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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	HCS12
Core Size	16-Bit
Speed	25MHz
Connectivity	CANbus, I²C, SCI, SPI
Peripherals	PWM, WDT
Number of I/O	91
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	2K x 8
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	2.35V ~ 5.25V
Data Converters	A/D 16x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	112-LQFP
Supplier Device Package	112-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mc9s12dt128vpve

Version Number	Revision Date	Effective Date	Author	Description of Changes
V02.07	29 Jan 2003	29 Jan 2003		Added 3L40K mask set in section 1.6 Corrected register entries in section 1.5.1 “Detailed Memory Map” Updated description for ROMCTL in section 2.3.31 Updated section 4.3.3 “Unsecuring the Microcontroller” Corrected and updated device-specific information for OSC (section 8.1) & Byteflight (section 15.1) Updated footnote in Table A-4 “Operating Conditions” Changed reference of VDDM to VDDR in section A.1.8 Removed footnote on input leakage current in Table A-6 “5V I/O Characteristics”
V02.08	26 Feb 2003	26 Feb 2003		Added part numbers MC9S12DT128E, MC9S12DG128E, and MC9S12DJ128E in “Preface” and related part number references Removed mask sets 0L40K and 2L40K from Table 1-3
V02.09	15 Oct 2003	15 Oct 2003		Replaced references to HCS12 Core Guide by the individual HCS12 Block guides in Table 0-2, section 1.5.1, and section 6; updated Fig.3-1 “Clock Connections” to show the individual HCS12 blocks Corrected PIM module name and document order number in Table 0-2 “Document References” Corrected ECT pulse accumulators description in section 1.2 “Features” Corrected KWP5 pin name in Fig 2-1 112LQFP pin assignments Corrected pull resistor CTRL/reset states for PE7 and PE4-PE0 in Table 2.1 “Signal Properties” Mentioned “S12LRAE” bootloader in Flash section 17 Corrected footnote on clamp of TEST pin under Table A-1 “Absolute Maximum Ratings” Corrected minimum bus frequency to 0.25MHz in Table A-4 “Operating Conditions” Replaced “burst programming” by “row programming” in A.3 “NVM, Flash and EEPROM” Corrected blank check time for EEPROM in Table A-11 “NVM Timing Characteristics” Corrected operating frequency in Table A-18 “SPI Master/Slave Mode Timing Characteristics
V02.10	6 Feb 2004	6 Feb 2004		Added A128 information in “Derivative Differences”, 2.1 “Device Pinout”, 2.2 “Signal Properties Summary”, Fig 23-2 & Fig 23-4 Added lead-free package option (PVE) in Table 0-2 “Derivative Differences for MC9S12DB128” and Fig 0-1 “Order Partnumber Example” Added an “AEC qualified” row in the “Derivative Differences” tables 0-1 & 0-2.
V02.11	3 May 2004	3 May 2004		Added part numbers SC515846, SC515847, SC515848, and SC515849 in “Derivative Differences” tables 0-1 & 0-2, section 2, and section 23. Corrected and added maskset 4L40K in tables 0-1 & 0-2 and section 1.6. Corrected BDLC module availability in DB128 80QFP part in “Derivative Differences” table 0-2.

List of Tables

1.4 Block Diagram

Figure 1-1 shows a block diagram of the MC9S12DT128 device.

$0080 - $009F ATD0 (Analog to Digital Converter 10 Bit 8 Channel)

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$0092	ATD0DR1H	Read:	Bit15	14	13	12	11	10	9	Bit8
		Write:								
$0093	ATD0DR1L	Read:	Bit7	Bit6	0	0	0	0	0	0
		Write:								
$0094	ATD0DR2H	Read:	Bit15	14	13	12	11	10	9	Bit8
		Write:								
$0095	ATD0DR2L	Read:	Bit7	Bit6	0	0	0	0	0	0
		Write:								
$0096	ATD0DR3H	Read:	Bit15	14	13	12	11	10	9	Bit8
		Write:								
$0097	ATD0DR3L	Read:	Bit7	Bit6	0	0	0	0	0	0
		Write:								
$0098	ATD0DR4H	Read:	Bit15	14	13	12	11	10	9	Bit8
		Write:								
$0099	ATD0DR4L	Read:	Bit7	Bit6	0	0	0	0	0	0
		Write:								
$009A	ATD0DR5H	Read:	Bit15	14	13	12	11	10	9	Bit8
		Write:								
$009B	ATD0DR5L	Read:	Bit7	Bit6	0	0	0	0	0	0
		Write:								
$009C	ATD0DR6H	Read:	Bit15	14	13	12	11	10	9	Bit8
		Write:								
$009D	ATD0DR6L	Read:	Bit7	Bit6	0	0	0	0	0	0
		Write:								
$009E	ATD0DR7H	Read:	Bit15	14	13	12	11	10	9	Bit8
		Write:								
$009F	ATD0DR7L	Read:	Bit7	Bit6	0	0	0	0	0	0
		Write:								

$00A0 - $00C7 PWM (Pulse Width Modulator 8 Bit 8 Channel)

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$00A0	PWME	Read:	PWME7	PWME6	PWME5	PWME4	PWME3	PWME2	PWME1	PWME0
		Write:								
$00A1	PWMPOL	Read:	PPOL7	PPOL6	PPOL5	PPOL4	PPOL3	PPOL2	PPOL1	PPOL0
		Write:								
$00A2	PWMCLK	Read:	PCLK7	PCLK6	PCLK5	PCLK4	PCLK3	PCLK2	PCLK1	PCLK0
		Write:								
$00A3	PWMPRCLK	Read:	0	PCKB2	PCKB1	PCKB0	0	PCKA2	PCKA1	PCKA0
		Write:								
$00A4	PWMCAE	Read:	CAE7	CAE6	CAE5	CAE4	CAE3	CAE2	CAE1	CAE0
		Write:								
$00A5	PWMCTL	Read:	CON67	CON45	CON23	CON01	PSWAI	PFRZ	0	0
		Write:								
$00A6	PWMTST Test Only	Read:	0	0	0	0	0	0	0	0
		Write:								
$00A7	PWMPRSC Test Only	Read:	0	0	0	0	0	0	0	0
		Write:								
$00A8	PWMSCLA	Read:	Bit 7	6	5	4	3	2	1	Bit 0
		Write:								

$0100 - $010F Flash Control Register (fts128k2)

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$0100	FCLKDIV	Read:	FDIVLD	PRDIV8	FDIV5	FDIV4	FDIV3	FDIV2	FDIV1	FDIV0
		Write:								
$0101	FSEC	Read:	KEYEN1	KEYEN0	NV5	NV4	NV3	NV2	SEC1	SEC0
		Write:								
$0102	FTSTMOD	Read:	0	0	0	WRALL	0	0	0	0
		Write:								
$0103	FCNFG	Read:	CBEIE	CCIE	KEYACC	0	0	0	BKSEL1	BKSEL0
		Write:								
$0104	FPROT	Read:	FPOPEN	NV6	FPHDIS	FPHS1	FPHS0	FPLDIS	FPLS1	FPLS0
		Write:								
$0105	FSTAT	Read:	CBEIF	CCIF	PVIOL	ACCERR	0	BLANK	0	0
		Write:								
$0106	FCMD	Read:	0	CMDB6	CMDB5	0	0	CMDB2	0	CMDB0
		Write:								
$0107	Reserved for Factory Test	Read:	0	0	0	0	0	0	0	0
		Write:								
$0108	FADDRHI	Read:	0	Bit 14	13	12	11	10	9	Bit 8
		Write:								
$0109	FADDRLO	Read:	Bit 7	6	5	4	3	2	1	Bit 0
		Write:								
$010A	FDATAHI	Read:	Bit 15	14	13	12	11	10	9	Bit 8
		Write:								
$010B	FDATALO	Read:	Bit 7	6	5	4	3	2	1	Bit 0
		Write:								
$010C - $010F	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								

$0110 - $011B EEPROM Control Register (eets2k)

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$0110	ECLKDIV	Read:	EDIVLD	PRDIV8	EDIV5	EDIV4	EDIV3	EDIV2	EDIV1	EDIV0
		Write:								
$0111	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
$0112	Reserved for Factory Test	Read:	0	0	0	0	0	0	0	0
		Write:								
$0113	ECNFG	Read:	CBEIE	CCIE	0	0	0	0	0	0
		Write:								
$0114	EPROT	Read:	EPOPEN	NV6	NV5	NV4	EPDIS	EP2	EP1	EP0
		Write:								
$0115	ESTAT	Read:	CBEIF	CCIF	PVIOL	ACCERR	0	BLANK	0	0
		Write:								
$0116	ECMD	Read:	0	CMDB6	CMDB5	0	0	CMDB2	0	CMDB0
		Write:								
$0117	Reserved for Factory Test	Read:	0	0	0	0	0	0	0	0
		Write:								
$0118	EADDRHI	Read:	0	0	0	0	0	0	Bit 9	Bit 8
		Write:								

$0180 - $01BF CAN1 (Motorola Scalable CAN - MSCAN)

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$0185	CAN1RIER	Read:	WUPIE	CSCIE	RSTATE1	RSTATE0	TSTATE1	TSTATE0	OVRIE	RXFIE
		Write:								
$0186	CAN1TFLG	Read:	0	0	0	0	0	TXE2	TXE1	TXE0
		Write:								
$0187	CAN1TIER	Read:	0	0	0	0	0	TXEIE2	TXEIE1	TXEIE0
		Write:								
$0188	CAN1TARQ	Read:	0	0	0	0	0	ABTRQ2	ABTRQ1	ABTRQ0
		Write:								
$0189	CAN1TAAK	Read:	0	0	0	0	0	ABTAK2	ABTAK1	ABTAK0
		Write:								
$018A	CAN1TBSEL	Read:	0	0	0	0	0	TX2	TX1	TX0
		Write:								
$018B	CAN1IDAC	Read:	0	0	IDAM1	IDAM0	0	IDHIT2	IDHIT1	IDHIT0
		Write:								
$018C	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
$018D	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
$018E	CAN1RXERR	Read:	RXERR7	RXERR6	RXERR5	RXERR4	RXERR3	RXERR2	RXERR1	RXERR0
		Write:								
$018F	CAN1TXERR	Read:	TXERR7	TXERR6	TXERR5	TXERR4	TXERR3	TXERR2	TXERR1	TXERR0
		Write:								
$0190 - $0193	CAN1IDAR0 - CAN1IDAR3	Read: Write:	AC7	AC6	AC5	AC4	AC3	AC2	AC1	AC0
$0194 - $0197	CAN1IDMR0 - CAN1IDMR3	Read: Write:	AM7	AM6	AM5	AM4	AM3	AM2	AM1	AM0
$0198 - $019B	CAN1IDAR4 - CAN1IDAR7	Read: Write:	AC7	AC6	AC5	AC4	AC3	AC2	AC1	AC0
$019C - $019F	CAN1IDMR4 - CAN1IDMR7	Read: Write:	AM7	AM6	AM5	AM4	AM3	AM2	AM1	AM0
$01A0 - $01AF	CAN0RXFG	Read:	FOREGROUND RECEIVE BUFFER see **(Table 1-2)**							
		Write:								
$01B0 - $01BF	CAN0TXFG	Read: Write:	FOREGROUND TRANSMIT BUFFER see **(Table 1-2)**							

$01C0 - $01FF Reserved

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$01C0 - $01FF	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								

$0200 - $023F Reserved

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$020C - $023F	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								

$02C0 - $02FF Reserved

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$02C0 - $02FF	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								

$0300 - $035F Byteflight

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$0300	BFMCR	Read:	INITRQ	MASTER	ALARM	SLPAK	SLPRQ	WPULSE	SSWAI	INITAK
		Write:								
$0301	BFFSIZR	Read:	0	0	0	FSIZ4	FSIZ3	FSIZ2	FSIZ1	FSIZ0
		Write:								
$0302	BFTCR1	Read:	TWX0T7	TWX0T6	TWX0T5	TWX0T4	TWX0T3	TWX0T2	TWX0T1	TWX0T0
		Write:								
$0303	BFTCR2	Read:	TWX0R7	TWX0R6	TWX0R5	TWX0R4	TWX0R3	TWX0R2	TWX0R1	TWX0R0
		Write:								
$0304	BFTCR3	Read:	TWX0D7	TWX0D6	TWX0D5	TWX0D4	TWX0D3	TWX0D2	TWX0D1	TWX0D0
		Write:								
$0305	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
$0306	BFRISR	Read:	RCVFIF	RXIF	SYNAIF	SYNNIF	SLMMIF	0	XSYNIF	OPTDF
		Write:								
$0307	BFGISR	Read:	TXIF	OVRNIF	ERRIF	SYNEIF	SYNLIF	ILLPIF	LOCKIF	WAKEIF
		Write:								
$0308	BFRIER	Read:	RCVFIE	RXIE	SYNAIE	SYNNIE	SLMMIE	0	XSYNIE	0
		Write:								
$0309	BFGIER	Read:	TXIE	OVRNIE	ERRIE	SYNEIE	SYNLIE	ILLPIE	LOCKIE	WAKEIE
		Write:								
$030A	BFRIVEC	Read:	0	0	0	0	RIVEC3	RIVEC2	RIVEC1	RIVEC0
		Write:								
$030B	BFTIVEC	Read:	0	0	0	0	TIVEC3	TIVEC2	TIVEC1	TIVEC0
		Write:								
$030C	BFFIDAC	Read:	FIDAC7	FIDAC6	FIDAC5	FIDAC4	FIDAC3	FIDAC2	FIDAC1	FIDAC0
		Write:								
$030D	BFFIDMR	Read:	FIDMR7	FIDMR6	FIDMR5	FIDMR4	FIDMR3	FIDMR2	FIDMR1	FIDMR0
		Write:								
$030E	BFMVR	Read:	MVR7	MVR6	MVR5	MVR4	MVR3	MVR2	MVR1	MVR0
		Write:								
$030F	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
$0310	BFPCTLBF	Read:	PMEREN	0	PSLMEN	PERREN	PROKEN	PSYNEN	0	BFEN
		Write:								
$0311	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
$0312	BFBUFLOCK	Read:	0	0	0	0	0	0	TXBUFLOCK	RXBUFLOCK
		Write:								
$0313	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
$0314	BFFIDRJ	Read:	FIDRJ7	FIDRJ6	FIDRJ5	FIDRJ4	FIDRJ3	FIDRJ2	FIDRJ1	FIDRJ0
		Write:								

Section 2 Signal Description

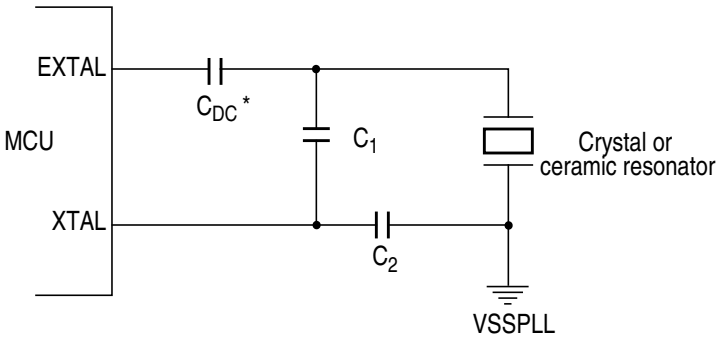
This section describes signals that connect off-chip. It includes a pinout diagram, a table of signal properties, and detailed discussion of signals. It is built from the signal description sections of the Block User Guides of the individual IP blocks on the device.

2.1 Device Pinout

The MC9S12DT128 and its derivatives are available in a 112-pin low profile quad flat pack (LQFP) and in a 80-pin quad flat pack (QFP). Most pins perform two or more functions, as described in the Signal Descriptions. **Figure 2-1**, **Figure 2-2**, and **Figure 2-3** show the pin assignments for different packages.

Pin Name Function 1	Pin Name Function 2	Pin Name Function 3	Pin Name Function 4	Pin Name Function 5	Powered by	Internal Pull Resistor		Description
						CTRL	Reset State	
PM1	*TXCAN0*	*TXB*	—	—	*VDDX*	*PERM/ PPSM*	*Disabled*	*Port M I/O, TX of CAN0, RX of BDLC*
PM0	*RXCAN0*	*RXB*	—	—	*VDDX*	*PERM/ PPSM*	*Disabled*	*Port M I/O, RX of CAN0, RX of BDLC*
PP7	KWP7	PWM7	—	—	VDDX	PERP/ PPSP	Disabled	Port P I/O, Interrupt, Channel 7 of PWM
PP6	**KWP6**	**PWM6**	**—**	**—**	**VDDX**	**PERP/ PPSP**	**Disabled**	**Port P I/O, Interrupt, Channel 6 of PWM**
PP5	KWP5	PWM5	—	—	VDDX	PERP/ PPSP	Disabled	Port P I/O, Interrupt, Channel 5 of PWM
PP4	KWP4	PWM4	—	—	VDDX	PERP/ PPSP	Disabled	Port P I/O, Interrupt, Channel 4 of PWM
PP3	KWP3	PWM3	$\overline{SS1}$	—	VDDX	PERP/ PPSP	Disabled	Port P I/O, Interrupt, Channel 3 of PWM, $\overline{SS}$ of SPI1
PP2	KWP2	PWM2	SCK1	—	VDDX	PERP/ PPSP	Disabled	Port P I/O, Interrupt, Channel 2 of PWM, SCK of SPI1
PP1	KWP1	PWM1	MOSI1	—	VDDX	PERP/ PPSP	Disabled	Port P I/O, Interrupt, Channel 1 of PWM, MOSI of SPI1
PP0	KWP0	PWM0	MISO1	—	VDDX	PERP/ PPSP	Disabled	Port P I/O, Interrupt, Channel 0 of PWM, MISO2 of SPI1
PS7	***$\overline{SS0}$***	**—**	**—**	**—**	***VDDX***	***PERS/ PPSS***	***Up***	***Port S I/O, $\overline{SS}$ of SPI0***
PS6	***SCK0***	**—**	**—**	**—**	***VDDX***	***PERS/ PPSS***	***Up***	***Port S I/O, SCK of SPI0***
PS5	***MOSI0***	**—**	**—**	**—**	***VDDX***	***PERS/ PPSS***	***Up***	***Port S I/O, MOSI of SPI0***
PS4	***MISO0***	**—**	**—**	**—**	***VDDX***	***PERS/ PPSS***	***Up***	***Port S I/O, MISO of SPI0***
PS3	*TXD1*	—	—	—	*VDDX*	*PERS/ PPSS*	*Up*	*Port S I/O, TXD of SCI1*
PS2	*RXD1*	—	—	—	*VDDX*	*PERS/ PPSS*	*Up*	*Port S I/O, RXD of SCI1*
PS1	TXD0	—	—	—	VDDX	PERS/ PPSS	Up	Port S I/O, TXD of SCI0
PS0	RXD0	—	—	—	VDDX	PERS/ PPSS	Up	Port S I/O, RXD of SCI0
PT[7:0]	IOC[7:0]	—	—	—	VDDX	PERT/ PPST	Disabled	Port T I/O, Timer channels

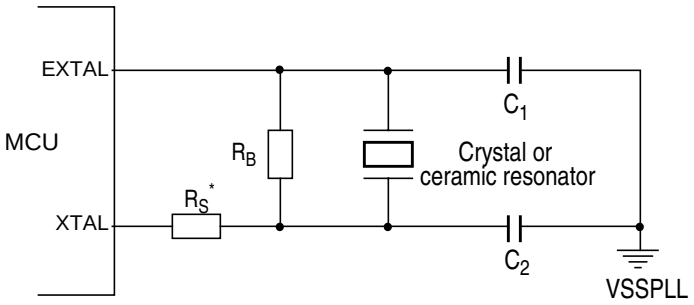
NOTES:
1. Refer to PEAR register description in HCS12 Multiplexed External Bus Interface (MEBI) Block Guide.



* Due to the nature of a translated ground Colpitts oscillator a DC voltage bias is applied to the crystal

Please contact the crystal manufacturer for crystal DC bias conditions and recommended capacitor value C_{DC}.

Figure 2-5 Colpitts Oscillator Connections (PE7=1)



* Rs can be zero (shorted) when used with higher frequency crystals. Refer to manufacturer's data.

Figure 2-6 Pierce Oscillator Connections (PE7=0)

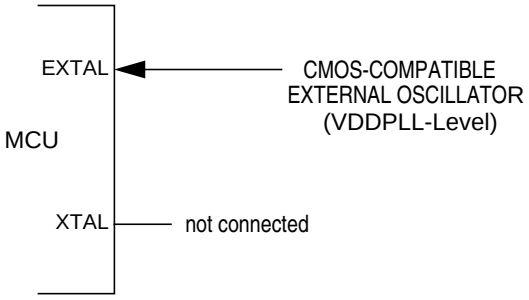


Figure 2-7 External Clock Connections (PE7=0)

2.3.51 PS5 / MOSI0 — Port S I/O Pin 5

PS5 is a general purpose input or output pin. It can be configured as master output (during master mode) or slave input pin (during slave mode) MOSI of the Serial Peripheral Interface 0 (SPI0).

2.3.52 PS4 / MISO0 — Port S I/O Pin 4

PS4 is a general purpose input or output pin. It can be configured as master input (during master mode) or slave output pin (during slave mode) MOSI of the Serial Peripheral Interface 0 (SPI0).

2.3.53 PS3 / TXD1 — Port S I/O Pin 3

PS3 is a general purpose input or output pin. It can be configured as the transmit pin TXD of Serial Communication Interface 1 (SCI1).

2.3.54 PS2 / RXD1 — Port S I/O Pin 2

PS2 is a general purpose input or output pin. It can be configured as the receive pin RXD of Serial Communication Interface 1 (SCI1).

2.3.55 PS1 / TXD0 — Port S I/O Pin 1

PS1 is a general purpose input or output pin. It can be configured as the transmit pin TXD of Serial Communication Interface 0 (SCI0).

2.3.56 PS0 / RXD0 — Port S I/O Pin 0

PS0 is a general purpose input or output pin. It can be configured as the receive pin RXD of Serial Communication Interface 0 (SCI0).

2.3.57 PT[7:0] / IOC[7:0] — Port T I/O Pins [7:0]

PT7-PT0 are general purpose input or output pins. They can be configured as input capture or output compare pins IOC7-IOC0 of the Enhanced Capture Timer (ECT).

2.4 Power Supply Pins

MC9S12DT128 power and ground pins are described below.

Table 2-2 MC9S12DT128 Power and Ground Connection Summary

Mnemonic	Pin Number	Nominal Voltage	Description
	112-pin QFP		
VDD1, 2	13, 65	2.5V	Internal power and ground generated by internal regulator
VSS1, 2	14, 66	0V	

Mnemonic	Pin Number 112-pin QFP	Nominal Voltage	Description
VDDR	41	5.0V	External power and ground, supply to pin drivers and internal voltage regulator.
VSSR	40	0V	
VDDX	107	5.0V	External power and ground, supply to pin drivers.
VSSX	106	0V	
VDDA	83	5.0V	Operating voltage and ground for the analog-to-digital converters and the reference for the internal voltage regulator, allows the supply voltage to the A/D to be bypassed independently.
VSSA	86	0V	
VRL	85	0V	Reference voltages for the analog-to-digital converter.
VRH	84	5.0V	
VDDPLL	43	2.5V	Provides operating voltage and ground for the Phased-Locked Loop. This allows the supply voltage to the PLL to be bypassed independently. Internal power and ground generated by internal regulator.
VSSPLL	45	0V	
VREGEN	97	5V	Internal Voltage Regulator enable/disable

NOTE: *All VSS pins must be connected together in the application.*

2.4.1 VDDX,VSSX — Power & Ground Pins for I/O Drivers

External power and ground for I/O drivers. Because fast signal transitions place high, short-duration current demands on the power supply, use bypass capacitors with high-frequency characteristics and place them as close to the MCU as possible. Bypass requirements depend on how heavily the MCU pins are loaded.

2.4.2 VDDR, VSSR — Power & Ground Pins for I/O Drivers & for Internal Voltage Regulator

External power and ground for I/O drivers and input to the internal voltage regulator. Because fast signal transitions place high, short-duration current demands on the power supply, use bypass capacitors with high-frequency characteristics and place them as close to the MCU as possible. Bypass requirements depend on how heavily the MCU pins are loaded.

2.4.3 VDD1, VDD2, VSS1, VSS2 — Internal Logic Power Supply Pins

Power is supplied to the MCU through VDD and VSS. Because fast signal transitions place high, short-duration current demands on the power supply, use bypass capacitors with high-frequency characteristics and place them as close to the MCU as possible. This 2.5V supply is derived from the internal voltage regulator. There is no static load on those pins allowed. The internal voltage regulator is turned off, if VREGEN is tied to ground.

NOTE: *No load allowed except for bypass capacitors.*

P_D = Total Chip Power Dissipation, [W]

Θ_{JA} = Package Thermal Resistance, [°C/W]

The total power dissipation can be calculated from:

$$P_D = P_{INT} + P_{IO}$$

P_{INT} = Chip Internal Power Dissipation, [W]

Two cases with internal voltage regulator enabled and disabled must be considered:

1. Internal Voltage Regulator disabled

$$P_{INT} = I_{DD} \cdot V_{DD} + I_{DDPLL} \cdot V_{DDPLL} + I_{DDA} \cdot V_{DDA}$$

$$P_{IO} = \sum_i R_{DSON} \cdot I_{IO_i}^2$$

Which is the sum of all output currents on I/O ports associated with VDDX and VDDR.

For R_{DSON} is valid:

$$R_{DSON} = \frac{V_{OL}}{I_{OL}}; \text{for outputs driven low}$$

respectively

$$R_{DSON} = \frac{V_{DD5} - V_{OH}}{I_{OH}}; \text{for outputs driven high}$$

2. Internal voltage regulator enabled

$$P_{INT} = I_{DDR} \cdot V_{DDR} + I_{DDA} \cdot V_{DDA}$$

I_{DDR} is the current shown in **(Table A-7)** and not the overall current flowing into VDDR, which additionally contains the current flowing into the external loads with output high.

$$P_{IO} = \sum_i R_{DSON} \cdot I_{IO_i}^2$$

Which is the sum of all output currents on I/O ports associated with VDDX and VDDR.

$$t_{era} \approx 4000 \cdot \frac{1}{f_{NVMOP}}$$

The setup time can be ignored for this operation.

A.3.1.4 Mass Erase

Erasing a NVM block takes:

$$t_{mass} \approx 20000 \cdot \frac{1}{f_{NVMOP}}$$

The setup time can be ignored for this operation.

A.3.1.5 Blank Check

The time it takes to perform a blank check on the Flash or EEPROM is dependant on the location of the first non-blank word starting at relative address zero. It takes one bus cycle per word to verify plus a setup of the command.

$$t_{check} \approx location \cdot t_{cyc} + 10 \cdot t_{cyc}$$

Table A-11 NVM Timing Characteristics

Conditions are shown in **(Table A-4)** unless otherwise noted							
Num	**C**	**Rating**	**Symbol**	**Min**	**Typ**	**Max**	**Unit**
1	D	External Oscillator Clock	f_{NVMOSC}	0.5		50 [1]	MHz
2	D	Bus frequency for Programming or Erase Operations	f_{NVMBUS}	1			MHz
3	D	Operating Frequency	f_{NVMOP}	150		200	kHz
4	P	Single Word Programming Time	t_{swpgm}	46 [2]		74.5 [3]	µs
5	D	Flash Row Programming consecutive word [4]	t_{bwpgm}	20.4 (2)		31 (3)	µs
6	D	Flash Row Programming Time for 32 Words (4)	t_{brpgm}	678.4 (2)		1035.5 (3)	µs
7	P	Sector Erase Time	t_{era}	20 [5]		26.7 (3)	ms
8	P	Mass Erase Time	t_{mass}	100 (5)		133 (3)	ms
9	D	Blank Check Time Flash per block	t_{check}	11 [6]		32778 [7]	t_{cyc}
10	D	Blank Check Time EEPROM per block	t_{check}	11 (6)		1034(7)	t_{cyc}

NOTES:
1. Restrictions for oscillator in crystal mode apply!
2. Minimum Programming times are achieved under maximum NVM operating frequency f_{NVMOP} and maximum bus frequency f_{bus}.
3. Maximum Erase and Programming times are achieved under particular combinations of f_{NVMOP} and bus frequency f_{bus}. Refer to formulae in Sections **Section A.3.1.1 Single Word Programming- Section A.3.1.4 Mass Erase**for guidance.
4. Row Programming operations are not applicable to EEPROM
5. Minimum Erase times are achieved under maximum NVM operating frequency f_{NVMOP}.
6. Minimum time, if first word in the array is not blank
7. Maximum time to complete check on an erased block

A.3.2 NVM Reliability

The reliability of the NVM blocks is guaranteed by stress test during qualification, constant process monitors and burn-in to screen early life failures.

The failure rates for data retention and program/erase cycling are specified at the operating conditions noted.

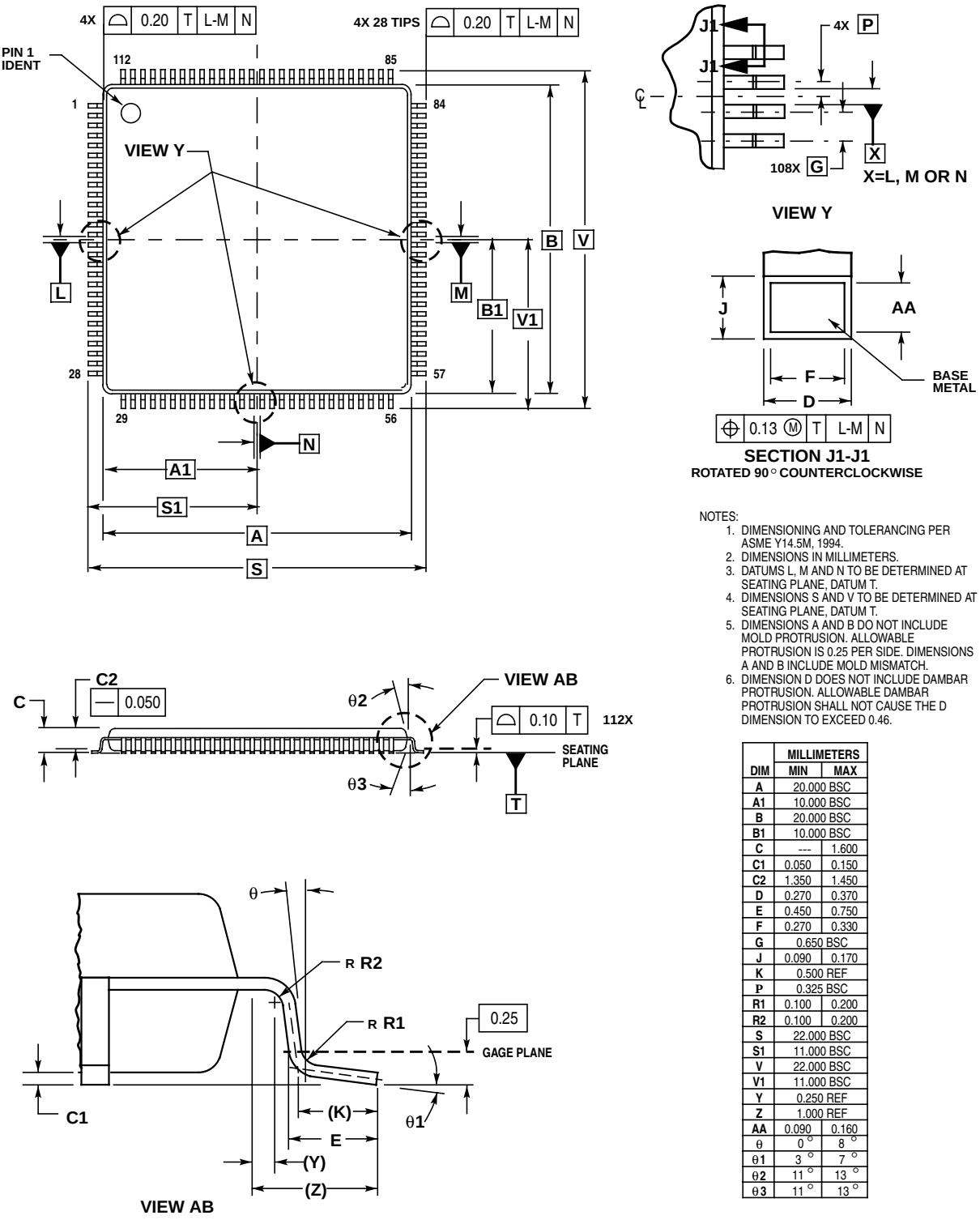
The program/erase cycle count on the sector is incremented every time a sector or mass erase event is executed.

Appendix B Package Information

B.1 General

This section provides the physical dimensions of the MC9S12DT128 packages.

B.2 112-pin LQFP package



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. DIMENSIONS IN MILLIMETERS.
3. DATUMS L, M AND N TO BE DETERMINED AT SEATING PLANE, DATUM T.
4. DIMENSIONS S AND V TO BE DETERMINED AT SEATING PLANE, DATUM T.
5. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 PER SIDE. DIMENSIONS A AND B INCLUDE MOLD MISMATCH.
6. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE D DIMENSION TO EXCEED 0.46.

	MILLIMETERS	
DIM	MIN	MAX
A	20.000 BSC	
A1	10.000 BSC	
B	20.000 BSC	
B1	10.000 BSC	
C	---	1.600
C1	0.050	0.150
C2	1.350	1.450
D	0.270	0.370
E	0.450	0.750
F	0.270	0.330
G	0.650 BSC	
J	0.090	0.170
K	0.500 REF	
P	0.325 BSC	
R1	0.100	0.200
R2	0.100	0.200
S	22.000 BSC	
S1	11.000 BSC	
V	22.000 BSC	
V1	11.000 BSC	
Y	0.250 REF	
Z	1.000 REF	
AA	0.090	0.160
θ	0°	8°
θ1	3°	7°
θ2	11°	13°
θ3	11°	13°

Figure 23-6 112-pin LQFP mechanical dimensions (case no. 987)