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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	ARM9®
Core Size	16/32-Bit
Speed	208MHz
Connectivity	EBI/EMI, I²C, Memory Card, SPI, UART/USART, USB OTG
Peripherals	DMA, PWM, WDT
Number of I/O	55
Program Memory Size	-
Program Memory Type	ROMless
EEPROM Size	-
RAM Size	64K x 8
Voltage - Supply (Vcc/Vdd)	1.1V ~ 3.3V
Data Converters	A/D 3x10b
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	320-LFBGA
Supplier Device Package	320-LFBGA (13x13)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/lpc3180fel320-01-5

- Up to 55 GPI, GPO, and GPIO pins. Includes 12 GPI pins, 24 GPO pins, and six GPIO pins.
- 10-bit ADC with input multiplexing from three pins.
- Real-Time Clock (RTC) with separate power supply and power domain, clocked by a dedicated 32 kHz oscillator. Includes a 128 byte scratch pad memory. The RTC may remain active when the rest of the chip is not powered.
- 32-bit general purpose high-speed timer with 16-bit pre-scaler with capture and compare capability.
- 32-bit millisecond timer driven from the RTC clock. Interrupts may be generated using two match registers.
- Watchdog timer.
- Two PWM blocks with an output rate up to 50 kHz.
- Keyboard scanner function provides automatic scanning of up to an 8×8 key matrix.
- Standard ARM test/debug interface for compatibility with existing tools.
- Emulation trace buffer with 2 k $\times$ 24-bit RAM allows trace via JTAG.
- On-chip crystal oscillator.
- Stop mode saves power, while allowing many peripheral functions to restart CPU activity.
- On-chip PLL allows CPU operation up to the maximum CPU rate without the need for a high frequency crystal.
- Boundary scan for simplified board testing.

3. Ordering information

Table 1. Ordering information

Type number	Package		
	Name	Description	Version
LPC3180FEL320[1]	LFBGA320	plastic low profile fine-pitch ball grid array package; 320 balls; body 13 $\times$ 13 $\times$ 0.9 mm	SOT824-1

[1] F = –40 °C to +85 °C temperature range.

4. Block diagram

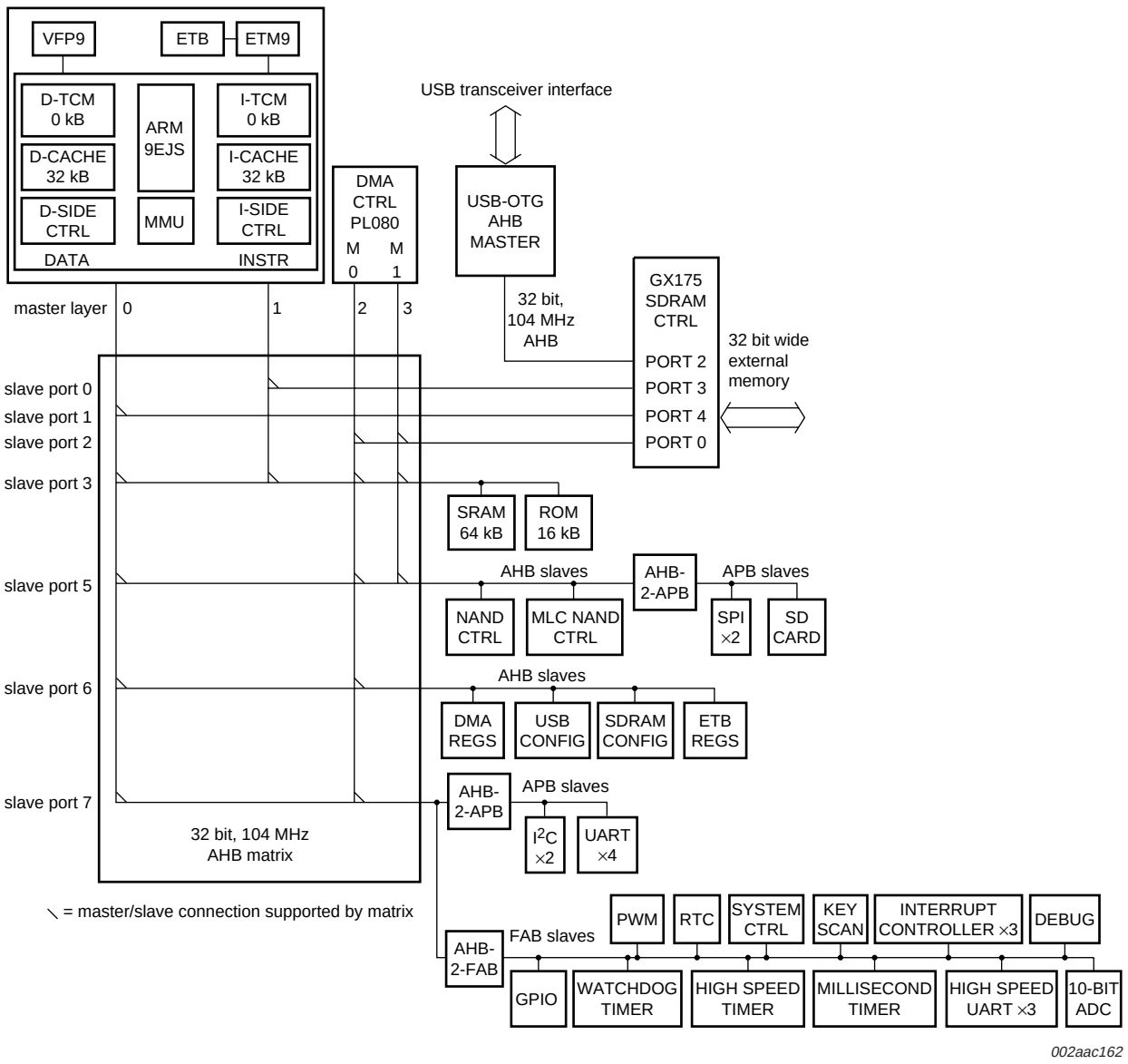


Fig 1. Block diagram

Table 2. Pin allocation table *…continued*

Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol
9	VSS	10	VDD_COREFXD12_01	11	VDD_RTCCORE12	12	VDD_RTC12
13	VSS_RTCOSC	14	VDD_RTCOSC12	15	i.c.[1]	16	VSS
17	VDD28	18	i.c.[1]	19	VSS	20	VSS_CORE_01
21	PLL397_LOOP	22	VDD_PLL397_12	23	VSS_PLL397	24	ADIN0
Row D							
1	KEY_ROW4	2	KEY_COL0	3	TEST	4	VSS_IO1828_01
5	U6_IRTX	6	VDD_CORE12_02	7	JTAG1_NTRST	8	VSS_CORE_02
9	U2_TX	10	GPI_11	11	VSS	12	ONSW
13	RESET_N	14	VDD28	15	VSS	16	VSS_CORE_03
17	VSS	18	VDD_COREFXD12_02	19	VSS_PLLHCLK	20	VDD_OSC12
21	i.c.[1]	22	VSS_AD	23	ADIN2	24	VDD_AD28
Row E							
1	KEY_ROW2	2	KEY_ROW5	3	VSS_IO28_01	4	KEY_COL4
21	VDD_AD28	22	ADIN1	23	RAM_D[30]/ PIO_SD[11]	24	RAM_D[31]/ PIO_SD[12]
Row F							
1	VSS_IO28_02	2	KEY_ROW1	3	KEY_ROW3	4	KEY_COL1
21	RAM_D[29]/ PIO_SD[10]	22	VDD_SDRAM18_02	23	VSS_SDRAM_01	24	RAM_D[28]/ PIO_SD[09]
Row G							
1	i.c.[1]	2	i.c.[1]	3	KEY_ROW0	4	VDD_IO28_02
21	VDD_SDRAM18_01	22	VSS_SDRAM_02	23	RAM_D[24]/ PIO_SD[05]	24	RAM_D[27]/ PIO_SD[08]
Row H							
1	GPI_00	2	i.c.[1]	3	PWM_OUT2	4	i.c.[1]
21	RAM_D[19]/ PIO_SD[00]	22	RAM_D[23]/ PIO_SD[04]	23	RAM_D[26]/ PIO_SD[07]	24	RAM_D[21]/ PIO_SD[02]
Row J							
1	GPI_07	2	PWM_OUT1	3	GPI_02	4	VSS_CORE_04
21	RAM_D[25]/ PIO_SD[06]	22	VDD_SDRAM18_03	23	VSS_SDRAM_03	24	RAM_D[20]/ PIO_SD[01]
Row K							
1	GPI_10/U4_RX	2	GPI_08/KEY_COL6/ SPI2_BUSY	3	GPI_01/SERVICE_N	4	GPI_04/SPI1_BUSY
21	VDD_CORE12_03	22	VDD_SDRAM18_04	23	RAM_D[22]/ PIO_SD[03]	24	RAM_D[18]/ DDR_NCLK
Row L							
1	GPO_03	2	GPI_09/KEY_COL7	3	VDD_CORE12_05	4	GPO_02
21	RAM_D[17]/ DDR_DQS1	22	RAM_D[13]	23	RAM_D[16]/ DDR_DQS0	24	RAM_D[15]

Table 2. Pin allocation table *…continued*

Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol
9	GPO_00/TST_CLK1	10	GPO_05	11	VDD_IO18_03	12	RESOUT_N
13	i.c.[1]	14	i.c.[1]	15	i.c.[1]	16	i.c.[1]
17	VSS_CORE_09	18	VDD_CORE12_08	19	FLASH_IO[04]	20	RAM_A[01]
21	VSS_SDRAM_09	22	RAM_A[07]	23	RAM_A[08]	24	RAM_A[11]
Row AC							
1	I2C1_SDA	2	VSS	3	VSS	4	VSS
5	VSS	6	VSS	7	VDD_IO18_04	8	USB_I2C_SCL
9	GPO_01	10	GPO_19	11	VSS	12	VSS_IO18_03
13	i.c.[1]	14	i.c.[1]	15	FLASH_CLE	16	VSS_IO18_01
17	FLASH_IO[06]	18	FLASH_RDY	19	FLASH_IO[02]	20	FLASH_IO[03]
21	FLASH_CE_N	22	RAM_A[04]	23	RAM_A[06]	24	VDD_SDRAM18_08
Row AD							
1	VSS	2	i.c.[1]	3	VSS	4	VDD1828
5	VSS	6	USB_OE_TP_N	7	USB_I2C_SDA	8	I2C2_SCL
9	GPO_14	10	GPO_20	11	VSS	12	i.c.[1]
13	i.c.[1]	14	i.c.[1]	15	VSS_IO18_02	16	i.c.[1]
17	FLASH_WR_N	18	FLASH_IO[07]	19	FLASH_IO[05]	20	FLASH_IO[01]
21	FLASH_IO[00]	22	RAM_A[00]	23	RAM_A[02]	24	RAM_A[03]

[1] These pins are connected internally and must be left unconnected in an application.

Table 3. Pin description *...continued*

Symbol	Pin	Type	Description
KEY_COL0 to KEY_COL5	D2, F4, C1, C2, E4, B1	I	keyboard scan column inputs
KEY_ROW0 to KEY_ROW5	G3, F2, E1, F3, D1, E2	O	keyboard scan row outputs 0 through 5
MS_BS	Y1	I/O	SD card command input/output (SD_CMD)
MS_DIO0 to MS_DIO3	W2, U2, Y2, V4	I/O	SD card data bus (SD_D0 to SD_D3)
MS_SCLK	AA1	O	SD card clock output (SD_CLK)
ONSW	D12	O	VCCon output signal
PLL397_LOOP	C21	I/O	loop filter pin for PLL397; requires external components if PLL397 is used
PWM_OUT1	J2	O	output of Pulse Width Modulator 1
PWM_OUT2	H3	O	output of Pulse Width Modulator 2
RAM_A[14:00]	W21, AA24, Y23, AB24, Y22, AA23, AB23, AB22, AC23, AA21, AC22, AD24, AD23, AB20, AD22	O	SDRAM address bus, pins 14 to 00
RAM_CAS_N	V23	O	SDRAM column address strobe output
RAM_CKE	U24	O	SDRAM clock enable output
RAM_CLK	U23	O	SDRAM clock output
RAM_CLKIN	T21	I	SDRAM clock return input
RAM_CS_N	V24	O	SDRAM chip select output
RAM_D[15:00]	L24, M23, L22, M24, N23, M22, N24, P23, N21, P24, R23, P21, R24, T24, T22, T23	I/O	SDRAM data bus, pins 15 to 00
RAM_D[16]/ DDR_DQS0	L23	I/O	**RAM_D[16] —** SDRAM data bus, pin 16
		O	**DDR_DQS0 —** SDRAM data strobe output for lower byte
RAM_D[17]/ DDR_DQS1	L21	I/O	**RAM_D[17] —** SDRAM data bus, pin 17
		O	**DDR_DQS1 —** SDRAM data strobe output for upper byte
RAM_D[18]/ DDR_NCLK	K24	I/O	**RAM_D[18] —** SDRAM data bus, pin 18
		O	**DDR_NCLK —** inverted SDRAM clock output for DDR
RAM_D[31:19]/ PIO_SD[12:00]	E24, E23, F21, F24, G24, H23, J21, G23, H22, K23, H24, J24, H21	I/O	**RAM_D[31:19] —** SDRAM data bus, pins 31 to 19
		I/O	**PIO_SD[12:00] —** general purpose input/output, pins 12 to 00; details may be found in Section 6.10 “General purpose parallel I/O” on page 18
RAM_DQM[3:0]	W24, V21, W23, Y24	O	SDRAM byte write mask outputs
RAM_RAS_N	U21	O	SDRAM row address strobe output
RAM_WR_N	V22	O	SDRAM write strobe output
RESET_N	D13	I	system reset input
RESOUT_N	AB12	O	reset output signal
RTCX_IN	A14	I	RTC oscillator input
RTCX_OUT	A13	O	RTC oscillator output

Table 3. Pin description *...continued*

Symbol	Pin	Type	Description
SPI1_CLK	W3	O	clock output for SPI1
SPI1_DATIN	V1	I	data input for SPI1
SPI1_DATIO	W1	I/O	data input/output for SPI1
SPI2_CLK	V3	O	clock output for SPI2
SPI2_DATIN	T4	I	data input for SPI2
SPI2_DATIO	V2	I/O	data input/output for SPI2
SYSCLKEN	C5	I/O	system clock request
SYSX_IN	A23	I	main oscillator input
SYSX_OUT	B23	O	main oscillator output
TEST	D3	I	test input; internally pulled down, should be left floating in an application
TST_CLK2	AB3	O	clock test output 2, controlled by the TEST_CLK
U1_RX/ PIO_INP[15]	B9	I	**U1_RX —** UART 1 receive data input
		I	**PIO_INP[15] —** general purpose input to PIO_INP_STATE register
U1_TX	B10	O	UART 1 transmit data output
U2_HCTS/ PIO_INP[16]	B8	I	**U2_HCTS —** UART 2 hardware flow control (CTS) input
		I	**PIO_INP[16] —** general purpose input to PIO_INP_STATE register
U2_RX/ PIO_INP[17]	C7	I	**U2_RX —** UART 2 receive data input
		I	**PIO_INP[17] —** general purpose input to PIO_INP_STATE register
U2_TX	D9	O	UART 2 transmit data output
U3_RX/ PIO_INP[18]	C6	I	**U3_RX —** UART 3 receive data input
		I	**PIO_INP[18] —** general purpose input to PIO_INP_STATE register
U3_TX	A7	O	UART 3 transmit data output
U5_RX/PIO_INP[20]	A2	I	**U5_RX —** UART 5 receive data input
		I	**PIO_INP[20] —** general purpose input to PIO_INP_STATE register
U5_TX	C4	O	UART 5 transmit data output
U6_IRRX/ PIO_INP[21]	A1	I/O	**U6_IRRX —** UART 6 receive data input; can be IrDA data
		I	**PIO_INP[21] —** general purpose input to PIO_INP_STATE register
U6_IRTX	D5	O	UART 6 transmit data output; can be IrDA data
U7_HCTS/ PIO_INP[22]	B2	I	**U7_HCTS —** UART 7 hardware flow control (CTS) input
		I	**PIO_INP[22] —** general purpose input to PIO_INP_STATE register
U7_RX/ PIO_INP[23]	C3	I	**U7_RX —** UART 7 receive data input
		I	**PIO_INP[23] —** general purpose input to PIO_INP_STATE register
U7_TX	B3	O	UART 7 transmit data output
USB_ATX_INT_N	AA7	I	USB interrupt from external transceiver

Table 3. Pin description *...continued*

Symbol	Pin	Type	Description
VSS_CORE_01 to VSS_CORE_09	C20, D8, D16, J4, R3, R21, AA5, AA10, AB17	I	ground for the core logic functions
VSS_IO1828_01 to VSS_IO1828_02	D4, A10	I	ground for I/O pins that may operate from either a 1.8 V range or a 3 V range
VSS_IO18_01 to VSS_IO18_04	AC16, AD15, AC12, AB8	I	ground for I/O pins that operate only from a 1.8 V range
VSS_IO28_01 to VSS_IO28_03	E3, F1, N3	I	ground for I/O pins that operate only from a 3 V range
VSS_OSC	B21	I	ground for the main oscillator
VSS_PLL397	C23	I	ground for the 397x PLL
VSS_PLLHCLK	D19	I	ground for the HCLK PLL
VSS_PLLUSB	B20	I	ground for the USB PLL
VSS_RTCCORE	B13	I	ground for the RTC block
VSS_RTCOSC	C13	I	ground for the 32 kHz RTC oscillator
VSS_SDRAM_01 to VSS_SDRAM_10	F23, G22, J23, M21, N22, R22, W22, AA22, AB21, AA18	I	ground for the SDRAM controller block
i.c.	A18, B17, B18, C18, U1, AD2, AA13, AD16, AB16, AA14, AC14, AB15, AD14, AC13, AB14, AD13, AB13, AD12, H2, G1, G2, H4, D21, B24, A24, C15		internally connected; leave open

6. Functional description

6.1 Architectural overview

The microcontroller is a general purpose 32-bit microprocessor, which offers high performance and very low power consumption. The ARM architecture is based on RISC principles, and the instruction set and related decode mechanism are much simpler than those of microprogrammed CISCs. This simplicity results in a high instruction throughput and impressive real-time interrupt response from a small and cost-effective processor core.

A 5-stage pipeline is employed so that all parts of the processing and memory systems can operate continuously. At any one point in time, several operations are typically in progress: subsequent instruction fetch, next instruction decode, instruction execution, memory access, and write-back. The combination of architectural enhancements gives the ARM9 about 30 % better performance than an ARM7 running at the same clock rate:

- Approximately 1.3 clocks per instruction (1.9 clocks per instruction for ARM7).
- Approximately 1.1 Dhrystone MIPS/MHz (0.9 Dhrystone MIPS/MHz for ARM7).

The ARM926EJ-S processor also employs a unique architectural strategy known as Thumb, which makes it ideally suited to high-volume applications with memory restrictions, or applications where code density is an issue.

The key idea behind Thumb is that of a super-reduced instruction set. Essentially, the ARM926EJ-S processor has two instruction sets:

1. The standard 32-bit ARM set.
2. A 16-bit Thumb set.

The Thumb set's 16-bit instruction length allows it to approach twice the density of standard ARM code while retaining most of the ARM's performance advantage over a traditional 16-bit processor using 16-bit registers. This is possible because Thumb code operates on the same 32-bit register set as ARM code.

Thumb code is able to provide up to 65 % of the code size of ARM, and 160 % of the performance of an equivalent ARM processor connected to a 16-bit memory system.

In addition, the ARM9 includes enhanced DSP instructions and multiplier, as well as an enhanced 32-bit MAC block.

6.2 Vector Floating Point (VFP) coprocessor

This CPU coprocessor provides full support for single-precision and double-precision add, subtract, multiply, divide, and multiply-accumulate operations at CPU clock speeds. It is compliant with the IEEE 754 standard, and enables advanced Motor control and DSP applications. The VFP has three separate pipelines for floating-point MAC operations, divide or square root operations, and load/store operations. These pipelines can operate in parallel and can complete execution out of order. All single-precision instructions, except divide and square root, take one cycle and double-precision multiply and multiply-accumulate instructions take two cycles. The VFP also provides format conversions between floating-point and integer word formats.

- Uses 32 kHz RTC clock

6.12 USB interface

The LPC3180 supports USB in either device, host, or OTG configuration.

6.12.1 USB device controller

The USB device controller enables 12 Mbit/s data exchange with a USB host controller. It consists of register interface, serial interface engine, endpoint buffer memory and DMA controller. The serial interface engine decodes the USB data stream and writes data to the appropriate end point buffer memory. The status of a completed USB transfer or error condition is indicated via status registers. An interrupt is also generated if enabled. The DMA controller when enabled transfers data between the endpoint buffer and the USB RAM.

6.12.1.1 Features

- Fully compliant with USB 2.0 full-speed specification.
- Supports 32 physical (16 logical) endpoints.
- Supports control, bulk, interrupt and isochronous endpoints.
- Scalable realization of endpoints at run time.
- Endpoint maximum packet size selection (up to USB maximum specification) by software at run time.
- RAM message buffer size based on endpoint realization and maximum packet size.
- Supports bus-powered capability with low suspend current.
- Supports DMA transfer on all non-control endpoints.
- One duplex DMA channel serves all endpoints.
- Allows dynamic switching between CPU controlled and DMA modes.
- Double buffer implementation for bulk and isochronous endpoints.

6.12.2 USB host controller

The host controller enables data exchange with various USB devices attached to the bus. It consists of register interface, serial interface engine and DMA controller. The register interface complies to the OHCI specification.

6.12.2.1 Features

- OHCI compliant.
- OHCI specifies the operation and interface of the USB host controller and SW driver.
- The host controller has four USB states visible to the SW driver:
  - USBOperational: Process lists and generate SOF tokens.
  - USBReset: Forces reset signaling on the bus, SOF disabled.
  - USBSuspend: Monitor USB for wake-up activity.
  - USBResume: Forces resume signaling on the bus.
- HCCA register points to interrupt and isochronous descriptors list.
- ControlHeadED and BulkHeadED registers point to control and bulk descriptors list.

6.12.3 USB OTG Controller

USB OTG (On-The-Go) is a supplement to the USB 2.0 specification that augments the capability of existing mobile devices and USB peripherals by adding host functionality for connection to USB peripherals.

6.12.3.1 Features

- Fully compliant with On-The-Go supplement to the USB Specification 2.0 Revision 1.0.
- Supports Host Negotiation Protocol (HNP) and Session Request Protocol (SRP) for dual-role devices under software control. HNP is partially implemented in hardware.
- Provides programmable timers required for HNP and SRP.
- Supports slave mode operation through AHB slave interface.
- Supports the OTG ATX from NXP (ISP 1301) or any external CEA-2011OTG specification compliant ATX.

6.13 UARTs

The LPC3180 contains seven UARTs. Four are standard UARTs, and three are special purpose high-speed UARTs.

6.13.1 Standard UARTs

The four standard UARTs are downwards compatible with the INS16Cx50. These UARTs support rates up to 460800 bit/s from a 13 MHz peripheral clock.

6.13.1.1 Features

- Each standard UART has 64 byte Receive and Transmit FIFOs.
- Receiver FIFO trigger points at 16 B, 32 B, 48 B, and 60 B.
- Transmitter FIFO trigger points at 0 B, 4 B, 8 B, and 16 B.
- Register locations conform to 16C550 industry standard.
- Each standard UART has a fractional rate pre-divider and an internal baud rate generator.
- The standard UARTs support three clocking modes: on, off, and auto-clock. The auto-clock mode shuts off the clock to the UART when it is idle.
- UART 6 includes an IrDA mode to support infrared communication.
- The standard UARTs are designed to support data rates of (2400, 4800, 9600, 19200, 38400, 57600, 115200, 230400, 460800) bit/s.
- Each UART includes an internal loopback mode.

6.13.2 High-speed UARTs

The three high-speed UARTs are designed to support rates up to 921600 bit/s from a 13 MHz peripheral clock, for on-board communication in low noise conditions. This is accomplished by changing the oversampling from 16× to 14×, and altering the rate generation logic.

6.13.2.1 Features

- Each high-speed UART has 64 byte Receive and Transmit FIFOs.
- Receiver FIFO trigger points at 1 B, 4 B, 8 B, 16 B, 32 B, and 48 B.
- Transmitter FIFO trigger points at 0 B, 4 B, and 8 B.
- Each high-speed UART has an internal baud rate generator.
- The high-speed UARTs are designed to support data rates of (2400, 4800, 9600, 19200, 38400, 57600, 115200, 230400, 460800, 921600) bit/s.
- Each UART includes an internal loopback mode.

6.14 I^2C-bus serial I/O controller

There are two I^2C-bus interfaces in the LPC3180. The blocks for the I^2C-bus are a master only implementation supporting the 400 kHz I^2C-bus mode and lower rates, with 7-bit slave addressing. Each has a four word FIFO for both transmit and receive. An interrupt signal is available from each block.

6.14.1 Features

- The two I^2C-bus blocks are standard I^2C-bus compliant interfaces that may be used in Single Master mode only.
- Programmable clock to allow adjustment of I^2C-bus transfer rates.
- Bidirectional data transfer.
- Serial clock synchronization allows devices with different bit rates to communicate via one serial bus.
- Serial clock synchronization can be used as a handshake mechanism to suspend and resume serial transfer.

6.15 SPI serial I/O controller

The LPC3180 has two Serial Peripheral Interfaces (SPI). The SPI is a 3-wire serial interface that is able to interface with a large range of serial peripheral or memory devices (SPI mode 0 to 3 compatible slave devices).

Only a single master and a single slave can communicate on the interface during a given data transfer. During a data transfer the master always sends a byte of data to the slave, and the slave always sends a byte of data to the master. The SPI implementation on the LPC3180 does not support operation as a slave.

6.15.1 Features

- Supports slaves compatible with SPI modes 0 to 3.
- Half duplex synchronous transfers.
- DMA support for data transmit and receive.
- 1-bit to 16-bit word length.
- Choice of LSB or MSB first data transmission.
- 64 $\times$ 16-bit input or output FIFO.
- Bit rates up to 52 Mbit/s.

6.23 Reset

Reset is accomplished by an active low signal on the RESET_N input pin. A reset pulse with a minimum width of 10 main oscillator clocks after the oscillator is stable is required to guarantee a valid chip reset. At power-up, 10 milliseconds should be allowed for the oscillator to start up and stabilize after V_{DD} reaches operational voltage. An internal reset with a minimum duration of 10 clock pulses will also be applied if the watchdog timer generates an internal device reset.

6.24 Clocking and power control

Clocking in the LPC3180 is designed to be versatile, so that system and peripheral requirements may be met, while allowing optimization of power consumption. Clocks to most functions may be turned off if not needed, some peripherals do this automatically.

The LPC3180 includes three operational modes that give control over processing speed and power consumption. In addition, clock rates to different functional blocks may be controlled by changing clock sources, reconfiguring PLL values, or altering clock divider configurations. This allows a trade-off of power versus processing speed based on application requirements.

6.24.1 Crystal oscillator

The main oscillator is the basis for the clocks most chip functions use by default. Optionally, many functions can be clocked instead by the output of a PLL (with a fixed 397x rate multiplication) which runs from the RTC oscillator. In this mode, the main oscillator may be turned off unless the USB interface is enabled. If a SYSCLK frequency other than 13 MHz is required in the application, or if the USB block is not used, the main oscillator may be used with a frequency of between 1 MHz and 20 MHz.

6.24.2 PLLs

The LPC3180 includes three PLLs: one allows boosting the RTC frequency to 13.008896 MHz for use as the primary system clock; one provides the 48 MHz clock required by the USB block; and one provides the basis for the CPU clock, the AHB bus clock, and the main peripheral clock.

The first PLL multiplies the 32768 Hz RTC clock by 397 to obtain a 13.008896 MHz clock. The 397x PLL is designed for low power operation and low jitter. This PLL requires an external RC loop filter for proper operation.

The other two PLLs accept an input clock from either the main oscillator or the output of the 397x PLL. The input frequency is multiplied up to a higher frequency, then divided down to provide the output clock.

The PLL input may initially be divided down by a pre-divider value ‘N’, which may have the values 1, 2, 3, or 4. This pre-divider can allow a greater number of possibilities for the output frequency.

Following the PLL input divider is the PLL multiplier. This can multiply the pre-divider output by a value ‘M’, in the range of 1 through 256. The resulting frequency must be in the range of 156 MHz to 320 MHz. The multiplier works by dividing the output of a Current Controlled Oscillator (CCO) by the value of M, then using a phase detector to compare the divided CCO output to the pre-divider output. The error value is used to adjust the CCO frequency.

At the PLL output, there is a post-divider that can be used to bring the CCO frequency down to the desired PLL output frequency. The post-divider value ‘P’, can divide the CCO output by 1, 2, 4, 8, or 16. The post-divider can also be bypassed, allowing the PLL CCO output to be used directly. The maximum PLL output frequency that is supported by the CPU is 208 MHz.

6.24.3 Power control and modes

The LPC3180 supports three operational modes, two of which are specifically designed to reduce power consumption. The modes are: Run mode, Direct Run mode, and Stop mode.

Run mode is the normal operating mode for applications that require the CPU, AHB bus, or any peripheral function other than the USB block to run faster than the main oscillator frequency. In Run mode, the CPU can run at up to 208 MHz and the AHB bus can run at up to 104 MHz.

Direct Run mode allows reducing the CPU and AHB bus rates in order to save power. Direct Run mode can also be the normal operating mode for applications that do not require the CPU, AHB bus, or any peripheral function other than the USB block to run faster than the main oscillator frequency. Direct Run mode is the default mode following chip reset.

Stop mode causes all CPU and AHB operation to cease, and stops clocks to peripherals other than the USB block.

6.24.4 APB bus

Many peripheral functions are accessed by on-chip APB busses that are attached to the higher speed AHB bus. The APB bus performs reads and writes to peripheral registers in three peripheral clocks.

6.24.5 FAB bus

Some peripherals are placed on a special bus called FAB that allows faster CPU access to those peripheral functions. Write access to FAB peripherals takes a single AHB clock. Read access to FAB peripherals takes two AHB clocks.

6.25 Emulation and debugging

The LPC3180 supports emulation and debugging via a dedicated JTAG serial port. An Embedded Trace Buffer allows tracing program execution. The dedicated JTAG port allows debugging of all chip features without impact to any pins that may be used in the application.

6.25.1 EmbeddedICE

Standard ARM EmbeddedICE logic provides on-chip debug support. The debugging of the target system requires a host computer running the debugger software and an EmbeddedICE protocol converter. The EmbeddedICE protocol converter converts the Remote Debug Protocol commands to the JTAG data needed to access the ARM core.

The ARM core has a Debug Communication Channel function built-in. The debug communication channel allows a program running on the target to communicate with the host debugger or another separate host without stopping the program flow or entering the debug state.

6.25.2 Embedded trace buffer

The Embedded Trace Module (ETM) is connected directly to the ARM core. It compresses the trace information and exports it through a narrow trace port. An internal Embedded Trace Buffer of 2 k $\times$ 24 bits captures the trace information under software debugger control. Data from the Embedded Trace Buffer is recovered by the debug software through the JTAG port.

The trace contains information about when the ARM core switches between states. Instruction trace (or PC trace) shows the flow of execution of the processor and provides a list of all the instructions that were executed. Instruction trace is significantly compressed by only broadcasting branch addresses as well as a set of status signals that indicate the pipeline status on a cycle by cycle basis. For data accesses either data or address or both can be traced.

8. Static characteristics

Table 5. Static characteristics

T_a = −40 °C to +85 °C, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
$V_{DD(1V2)}$	supply voltage (1.2 V)	core supply voltage for full performance; full frequency range	[2]	1.1	1.2	1.3	V
		core supply voltage for reduced power; up to 14 MHz CPU	[2]	0.9	-	1.3	V
		RTC supply voltage	[3]	0.9	-	1.3	V
		PLL and oscillator supply voltage	[4]	1.1	1.2	1.3	V
$V_{DD(1V8)}$	supply voltage (1.8 V)	external supply voltage	[5]	1.7	1.8	1.95	V
$V_{DD(3V0)}$	supply voltage (3.0 V)	external supply voltage	[6]	2.7	3	3.3	V
$V_{DDA(3V0)}$	analog supply voltage (3.0 V)	applies to VDD_AD28 pins		2.7	3	3.3	V
V_{DD}	supply voltage	in 1.8 V range	[7]	1.7	1.8	1.95	V
		in 3.0 V range		2.7	3	3.3	V
I_{IL}	LOW-state input current	V_I = 0 V; no pull-up		-	-	3	µA
I_{IH}	HIGH-state input current	$V_I = V_{DD}$; no pull-down	[8]	-	-	3	µA
I_{OZ}	OFF-state output current	V_O = 0 V; $V_O = V_{DD}$; no pull-up/down	[8]	-	-	3	µA
I_{latch}	I/O latch-up current	$-(1.5V_{DD}) < V_I < (1.5V_{DD})$	[8]	-	-	100	mA
V_I	input voltage		[8][9] [10][11]	0	-	V_{DD}	V
V_{IH}	HIGH-state input voltage	1.8 V inputs		1.6	-	-	V
		3.0 V inputs		2.0	-	-	V
V_{IL}	LOW-state input voltage	1.8 V inputs		-	-	0.6	V
		3.0 V inputs		-	-	0.8	V
V_{OH}	HIGH-state output voltage	1.8 V outputs; I_{OH} = −1 mA	[12]	V_{DD} − 0.4	-	-	V
		3.0 V outputs; I_{OH} = −4 mA	[12]	V_{DD} − 0.4	-	-	V
V_{OL}	LOW-state output voltage	1.8 V outputs; I_{OL} = 4 mA	[12]	-	-	0.4	V
		3.0 V outputs; I_{OL} = 4 mA	[12]	-	-	0.4	V
I_{OH}	HIGH-state output current	$V_{OH} = V_{DD}$ − 0.4 V	[8][12]	-	−4	-	mA
I_{OL}	LOW-state output current	V_{OL} = 0.4 V	[8][12]	-	4	-	mA
I_{OHS}	HIGH-state short-circuit output current	V_{OH} = 0 V	[13]	-	−45	-	mA
I_{OLS}	LOW-state short-circuit output current	$V_{OL} = V_{DD}$	[8][13]	-	45	-	mA

9. Dynamic characteristics

Table 6. Dynamic characteristics

T_a = −40 °C to +85 °C, unless otherwise specified.[1]

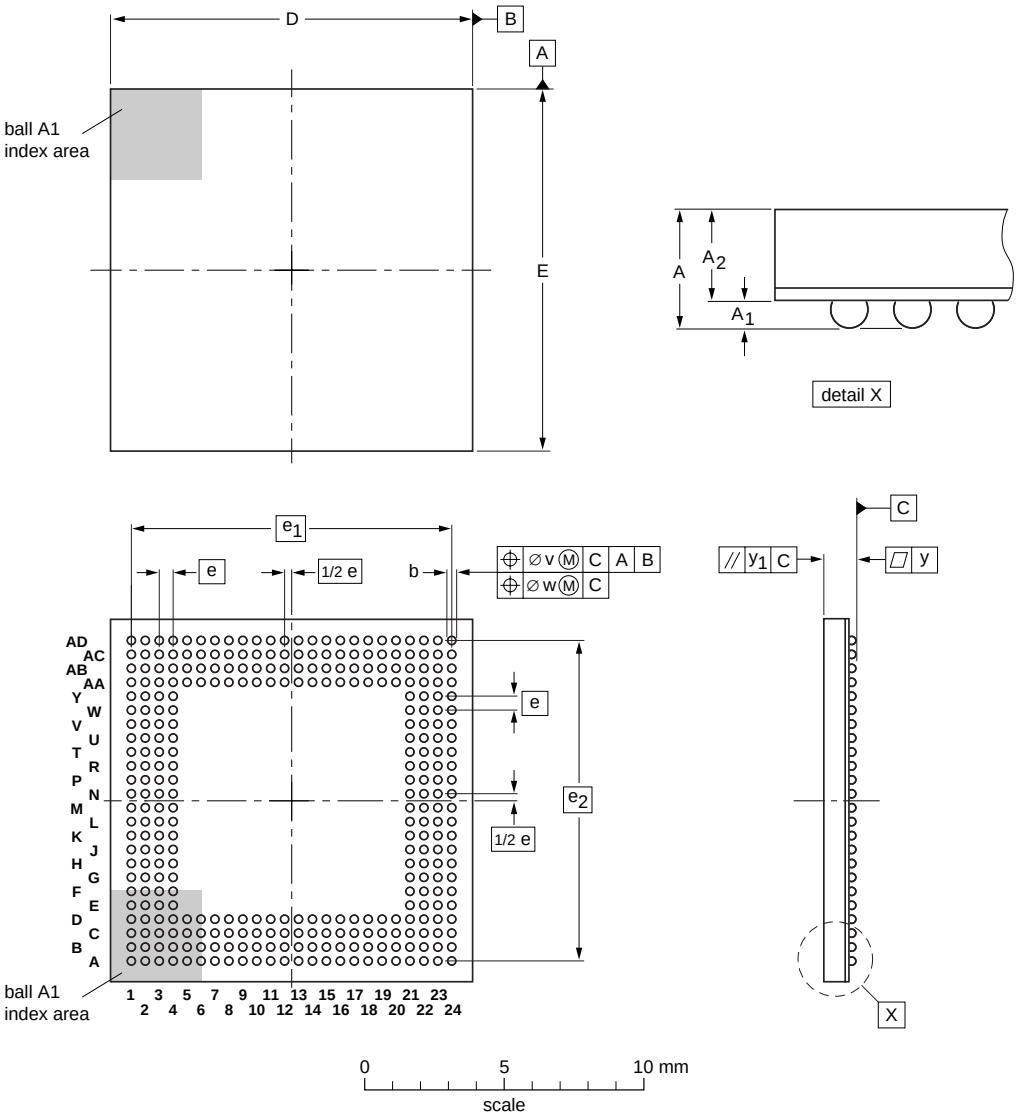
Symbol	Parameter	Conditions		Min	Typ	Max	Unit
External clock							
f_{ext}	external clock frequency		[2]	1	13	20	MHz
Port pins							
t_r	rise time			-	5	-	ns
t_f	fall time			-	5	-	ns

[1] Parameters are valid over operating temperature range unless otherwise specified.

[2] Supplied by an external crystal.

10. Package outline

LFBGA320: plastic low profile fine-pitch ball grid array package; 320 balls; body 13 x 13 x 0.9 mm SOT824-1



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	b	D	E	e	e_1	e_2	v	w	y	y_1
mm	1.3	0.3 0.2	1.0 0.8	0.35 0.25	13.1 12.9	13.1 12.9	0.5	11.5	11.5	0.15	0.05	0.08	0.1

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT824-1		- - -				03-07-09

Fig 4. Package outline SOT824-1 (LFBGA320)

11. Abbreviations

Table 7. Abbreviations

Acronym	Description
ADC	Analog-to-Digital Converter
AHB	Advanced High-performance Bus
APB	Advanced Peripheral Bus
CISC	Complex Instruction Set Computer
DDR	Double Data Rate
DMA	Direct Memory Access
DSP	Digital Signal Processing
FAB	Fast Access Bus
FIFO	First In, First Out
FIQ	Fast Interrupt Request
GPI	General Purpose Input
GPIO	General Purpose Input/Output
GPO	General Purpose Output
IRQ	Interrupt Request
MAC	Multiply-Accumulate
MMU	Memory Management Unit
OHCI	Open Host Controller Interface
OTG	On-The-Go
PLL	Phase-Locked Loop
PWM	Pulse Width Modulator
RC	Resistor-Capacitor
SDR	Single Data Rate
SPI	Serial Peripheral Interface
UART	Universal Asynchronous Receiver/Transmitter

12. Revision history

Table 8. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
LPC3180_2	20070215	Preliminary data sheet	-	LPC3180_1
Modifications:	• The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors. • Legal texts have been adapted to the new company name where appropriate. • Table 4 “Limiting values”; updated <tbd> values for V_{IA}, V_I, I_{DD}, and I_{SS}.			
LPC3180_1	20060602	Preliminary data sheet	-	-

15. Contents

For more information, please visit: http://www.nxp.com
For sales office addresses, please send an email to: salesaddresses@nxp.com

Date of release: 15 February 2007
Document identifier: LPC3180_2