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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	-
Core Size	8-Bit
Speed	12MHz
Connectivity	SIO, UART/USART
Peripherals	LVD, POR, PWM, WDT
Number of I/O	18
Program Memory Size	8KB (8K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	256 x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 7x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	24-LFSOP (0.173", 4.40mm Width)
Supplier Device Package	24-SSOP
Purchase URL	https://www.e-xfl.com/product-detail/onsemi/lc87f0g08auja-ah

Function Details

■Flash ROM
- Capable of on-board programming with a wide range of supply voltages : 2.2 to 5.5V
- Block-erasable in 128 byte units
- Writes data in 2-byte units
- 8192 × 8 bits

■RAM
- 256 × 9 bits

■Bus Cycle Time
- 83.3ns (12MHz, V_{DD}=2.7V to 5.5V, Ta=–40°C to 85°C)
- 125ns (8MHz, V_{DD}=2.0V to 5.5V, Ta=–40°C to 85°C)
- 250ns (4MHz, V_{DD}=1.8V to 5.5V, Ta=–40°C to 85°C)

Note : The bus cycle time here refers to the ROM read speed.

■Minimum Instruction Cycle Time (tCYC)
- 250ns (12MHz, V_{DD}=2.7V to 5.5V, Ta=–40°C to 85°C)
- 375ns (8MHz, V_{DD}=2.0V to 5.5V, Ta=–40°C to 85°C)
- 750ns (4MHz, V_{DD}=1,8V to 5.5V, Ta=–40°C to 85°C)

■Potrs
- Normal withstand voltage I/O ports whose I/O direction can be designated in 1-bit units 18($\overline{P0n}$, P1n, P70, CF1, CF2)
- Reset pins 1($\overline{RES}$)
- Power supply pins 3($V_{SS}1$, $V_{SS}2$,$V_{DD}1$)
- Reference voltage outputs 1(VREF)
- Dedicated debugger port 1(OWP0)

■Timers
- Timer 0 : 16-bit timer/counter with 2 capture registers.
  - Mode 0 : 8-bit timer with an 8-bit programmable prescaler (with two 8-bit capture registers) × 2 channels
  - Mode 1 : 8-bit timer with an 8-bit programmable prescaler (with two 8-bit capture registers) + 8-bit counter (with two 8-bit capture registers)
  - Mode 2 : 16-bit timer with an 8-bit programmable prescaler (with two 16-bit capture registers)
  - Mode 3 : 16-bit counter (with two 16-bit capture registers)
- Timer 1 : 16-bit timer/counter that supports PWM/toggle outputs
  - Mode 0 : 8-bit timer with an 8-bit prescaler (with toggle outputs) + 8-bit timer/counter with an 8-bit prescaler (with toggle outputs)
  - Mode 1 : 8-bit PWM with an 8-bit prescaler × 2 channels
  - Mode 2 : 16-bit timer/counter with an 8-bit prescaler (with toggle outputs) (toggle outputs also possible from lower-order 8 bits)
  - Mode 3 : 16-bit timer with an 8-bit prescaler (with toggle outputs) (lower-order 8 bits may be used as a PWM output)
- Base timer
  (1) The clock is selectable from the subclock (32.768kHz crystal oscillation), the low speed RC, system clock, and timer 0 prescaler output.
  (2) with an 8-bit programmable prescaler
  (3) Interrupts programmable in 5 different time schemes

■Standby Function

● HALT mode: Halts instruction execution while allowing the peripheral circuits to continue operation.
1) Oscillation is not halted automatically.
2) There are three ways of resetting the HALT mode.
(1) Setting the reset pin to the low level
(2) Having the watchdog timer or LVD function generate a reset
(3) Having an interrupt generated

● HOLD mode: Suspends instruction execution and the operation of the peripheral circuits.
1) The CF, RC and crystal oscillators automatically stop operation.
Note: The low-speed RC oscillator is controlled directly by the watchdog timer; its oscillation in the standby mode is also controlled by the watchdog timer.
2) There are four ways of resetting the HOLD mode:
(1) Setting the reset pin to the lower level
(2) Having the watchdog timer or LVD function generate a reset
(3) Having an interrupt source established at one of the INT0, INT1, INT2 and INT4 pins
* INT0 and INT1 can be used in the level sense mode only.
(4) Having an interrupt source established at port 0.

● X'tal HOLD mode: Suspends instruction execution and the operation of the peripheral circuits except the base timer. (when X'tal oscillation or low-speed RC oscillation is selected).
1) The CF, low-speed, and medium-speed RC oscillators automatically stop operation.
Note: The low-speed RC oscillator is controlled directly by the watchdog timer; its oscillation in the standby mode is also controlled by the watchdog timer.
Note: If the base timer is run with low-speed RC oscillation selected as the base timer input clock source and the X'tal HOLD mode is entered, the low-speed RC oscillator retains the state that is established when the X'tal HOLD mode is entered.
2) The state of crystal oscillation established when the X'tal HOLD mode is entered is retained.
3) There are five ways of resetting the X'tal HOLD mode.
(1) Setting the reset pin to the low level
(2) Having the watchdog timer or LVD function generate a reset
(3) Having an interrupt source established at one of the INT0, INT1, INT2, and INT4 pins
* INT0 and INT1 can be used in the level sense mode only.
(4) Having an interrupt source established at port 0
(5) Having an interrupt source established in the base timer circuit

■VCPWM: Frequency tunable 12-bit PWM × 2ch

■High speed PWM (HPWM2)

8-/10- bits PWM ×1ch
1) The PWM clock is selectable from system clock and Hi-speed RC2 (40MHz)
2) The PWM type is selectable from 8 bits(Normal mode) and 10 bits(additive puls mode).

■Temperature sensor

- Senseor voltage can be comapred by the AD converter.

■On-chip Debugger Function

- Supports software debugging with the IC mounted on the target board.
- Provides 1 channel of on-chip debugger pin.
  OWP0

■Data Security Function

- Protects the program data stored in flash memory from unauthorized read or copy.
  Note: This data security function does not necessarily provide absolute data security.

■Package Form

- SSOP24 (225mil): Lead-free and halogen-free type

■Development Tools

- On-chip debugger: TCB87 Type C (1-wire interface cable) + LC87F0G08A

■Programming Boards

Package	Programming boards
SSOP24(225mil)	W87F0GS

■Flash Programmer

Maker		Model	Supported version	Device
Flash Support Group, Inc. (FSG)	Single Programmer	AF9709C	Rev 03.28 or later	87F008SU
Flash Support Group, Inc. (FSG) + Our company (Note 1)	Onboard Single/Gang Programmer	AF9101/AF9103(Main unit) (FSG models)	(Note 2)	-
		SIB87 Type C(Inter Face Driver) (Our company model)		
Our company	Single/Gang Programmer	SKK Type B / SKK Type C	Application Version 1.08 or later Chip Data Version 2.46 or later	LC87F0G08
	Onboard Single/Gang Programmer	SKK-DBG Type C		

For information about AF-Series :
Flash Support Group, Inc.
TEL: +81-53-459-1050
E-mail: sales@j-fsg.co.jp

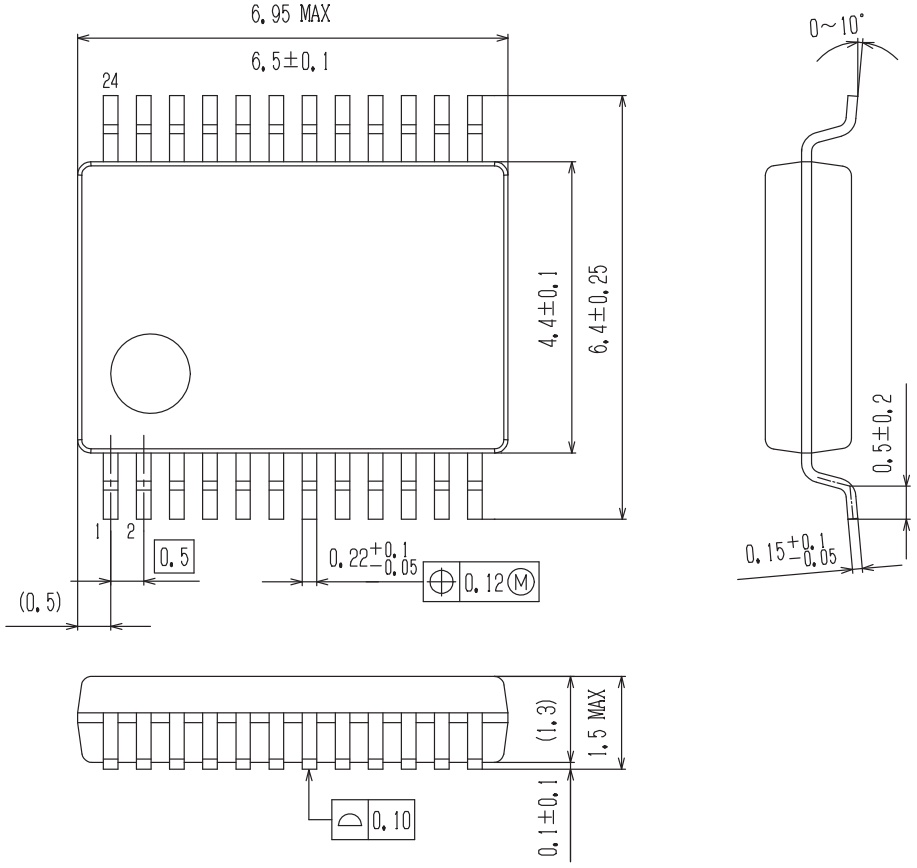
Note1: On-board-programmer from FSG (AF9101/AF9103) and serial interface driver from Our company (SIB87 Type C) together can give a PC-less, standalone on-board-programming capabilities.

Note2: It needs a special programming devices and applications depending on the use of programming environment. Please ask FSG or Our company for the information.

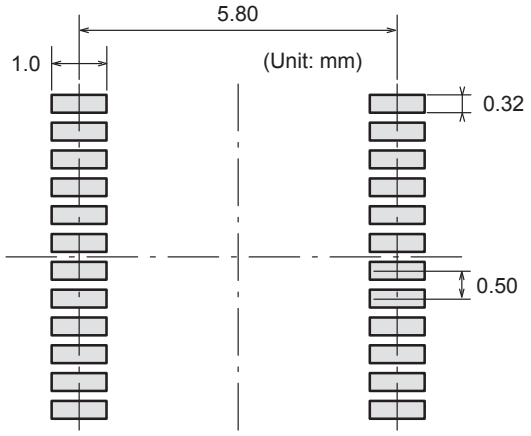
Package Dimensions

unit : mm

SSOP24 (225mil)
CASE 565AR
ISSUE A



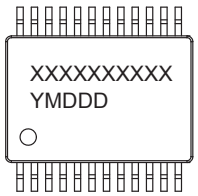
SOLDERING FOOTPRINT*



NOTE: The measurements are not to guarantee but for reference only.

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

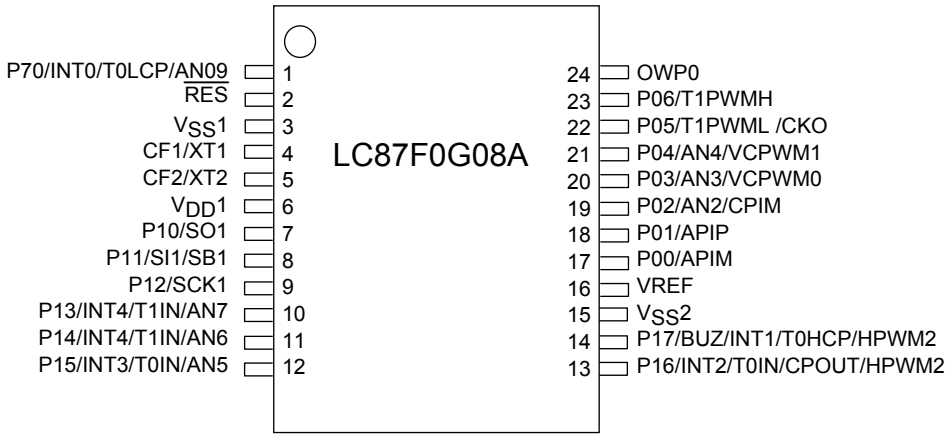
GENERIC MARKING DIAGRAM*



XXXXX = Specific Device Code
Y = Year
M = Month
DDD = Additional Traceability Data

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present.

Pin Assignment

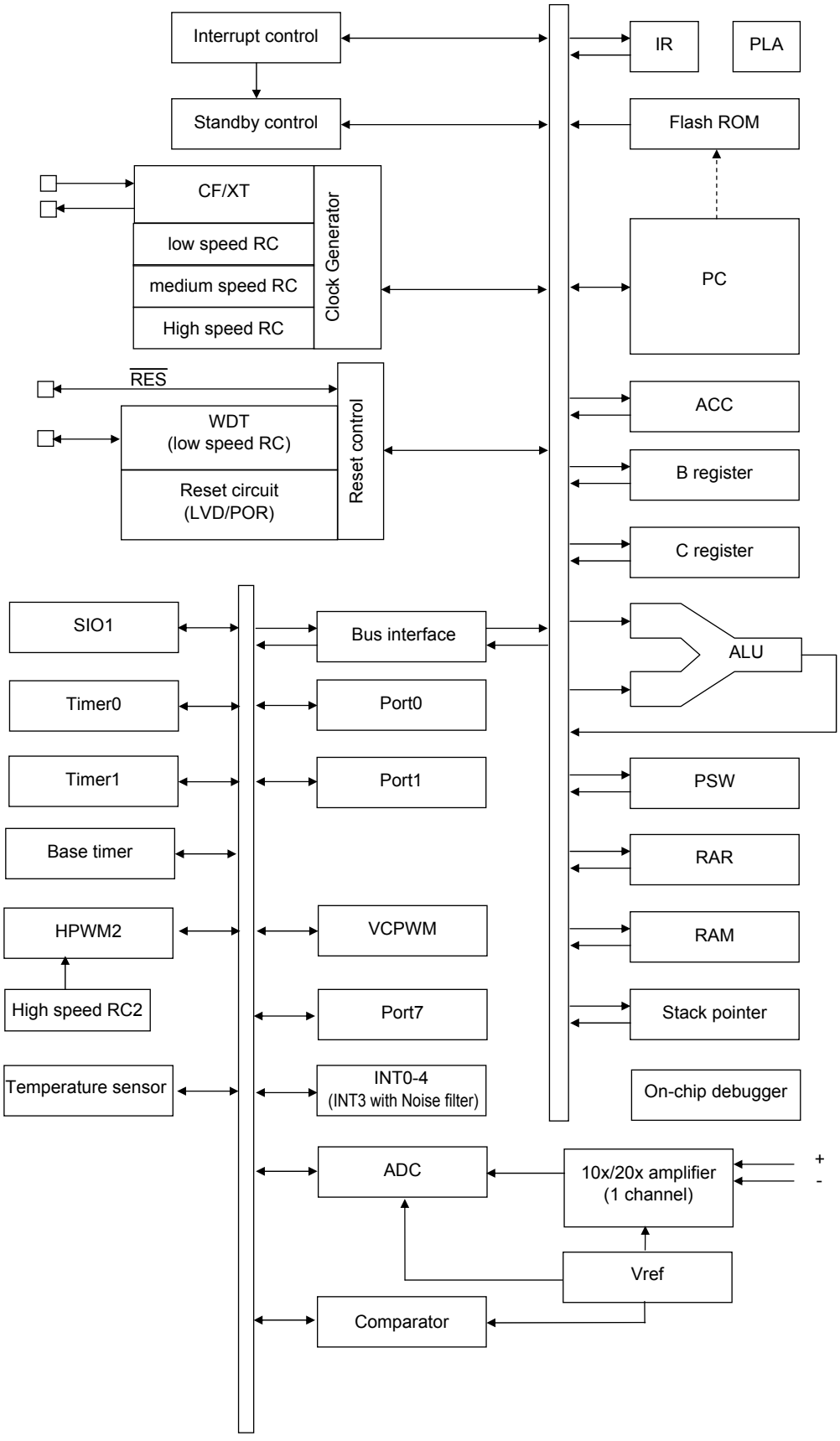


SSOP24(225mil) "Lead-/Halogen-free Type"

SSOP24	NAME
1	P70/INT0/T0LCP/AN09
2	$\overline{RES}$
3	$V_{SS}1$
4	CF1/XT1
5	CF2/XT2
6	$V_{DD}1$
7	P10/SO1
8	P11/SI1/SB1
9	P12/SCK1
10	P13/INT4/T1IN/AN7
11	P14/INT4/T1IN/AN6
12	P15/INT3/T0IN/AN5

SSOP24	NAME
13	P16/INT2/T0IN/CPOUT/HPWM2
14	P17/BUZ/INT1/T0HCP/HPWM2
15	$V_{SS}2$
16	VREF
17	P00/APIM
18	P01/APIP
19	P02/AN2/CPIM
20	P03/AN3/VCPWM0
21	P04/AN4/VCPWM1
22	P05/T1PWML/CKO
23	P06/T1PWMH
24	OWP0

System Block Diagram



Continued from preceding page.

<table>
<tr><th>Pin Name</th><th>I/O</th><th>Description</th><th>Option</th></tr>
<tr><td>Port 7
P70</td><td>I/O</td><td>• 1-bit I/O port
• I/O specifiable
• Pull-up resistors can be turned on and off.

• Pin functions
P70 : INT0 input/HOLD release input/timer 0L capture input/AD converter input port (AN9)

Interrupt acknowledge type
<table>
<tr><th></th><th>Rising</th><th>Falling</th><th>Rising & Falling</th><th>H level</th><th>L level</th></tr>
<tr><td>INT0</td><td>enable</td><td>enable</td><td>disable</td><td>enable</td><td>enable</td></tr>
</table></td><td>No</td></tr>
<tr><td>$\overline{\text{RES}}$</td><td>I</td><td>External reset input/internal reset output pin</td><td>Yes
Internal pullup ON/OFF</td></tr>
<tr><td>CF1/XT1</td><td>I/O</td><td>• Ceramic oscillator/32.768kHz crystal oscillator input pin

• Pin functions
• 1-bit I/O port
• I/O specifiable
(only Nch-open drain)</td><td>No</td></tr>
<tr><td>CF2/XT2</td><td>I/O</td><td>• Ceramic oscillator/32.768kHz crystal oscillator output pin

• Pin functions
• 1-bit I/O port
• I/O specifiable</td><td>No</td></tr>
<tr><td>OWP0</td><td>I/O</td><td>On-chip debugger pin</td><td>No</td></tr>
</table>

Port Output Types

The table below lists the types of port outputs and the presence/absence of a pull-up resistor.
Data can be read into any input port even if it is in the output mode.

Port Name	Option selected in units of	Option type	Output type	Pull-up resistor
P00 to P06	1 bit	1	CMOS	Programmable
		2	Nch-open drain	Programmable
P10 to P17	1 bit	1	CMOS	Programmable
		2	Nch-open drain	Programmable
CF1/XT1	-	No	Nch-open drain when general I/O port is selected.	No
CF2/XT2	-	No	CMOS / Nch-open drain when general I/O port is selected.(programmable)	No
P70	-	No	Nch-open drain	Programmable

User Option Table

Option Name	Option Type	Flash Version	Option Selected in Units of	Option Selection
Port output form	P00 to P06	enable	1 bit	CMOS
				Nch-open drain
	P10 to P17	enable	1 bit	CMOS
				Nch-open drain
Program start address	-	enable	-	00000h or 01E00h When protected area 1) is selected
				00000h When either of protected area 2), 3) or 4) is selected
Protected area (Note1)	-	enable	-	1) 1800h-1FFFh
				2) 0000h-1DFFh,1F00h-1FFFh
				3) 0000h-1CFFh,1F00h-1FFFh
				4) 0000h-1AFFh,1F00h-1FFFh
Reset pin	Internal pullup ON/OFF	enable	-	ON
				OFF
Low-voltage detection reset function	Detect function	enable	-	Enable: Use
				Disable: Not Used
	Detect level	enable	-	7-level
Power-on reset function	Power-On reset level	enable	-	1-level

Note1: onboard programming inhbited address

Recommended Unused Pin Connections

Port Name	Recommended Unused Pin Connections	
	Board	Software
P00 to P07	Open	Output low
P10 to P17	Open	Output low
P70	Open	Output low
CF1/XT1	Open	General I/O port output low
CF2/XT2	Open	General I/O port output low
OWP0	Pulled low with a 100kΩ resistor	-

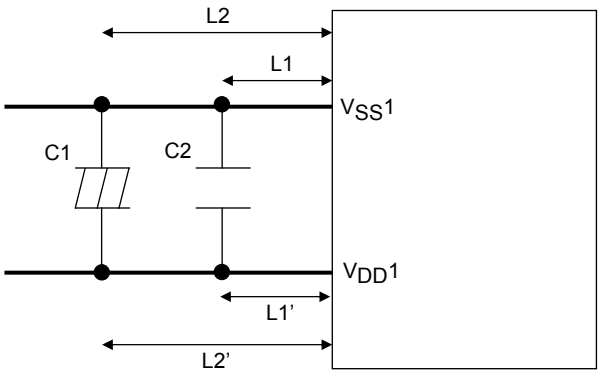
On-chip Debugger Pin Connection Requirements

For the treatment of the on-chip debugger pins, refer to the separately available documents entitled "Rd87 On-chip Debugger Installation Manual"

Power Pin Treatment Recommendations ($V_{DD}1$, $V_{SS}1$)

Connect bypass capacitors that meet the following conditions between the $V_{DD}1$ and $V_{SS}1$ pins:

- Connect among the $V_{DD}1$ and $V_{SS}1$ pins and bypass capacitors C1 and C2 with the shortest possible heavy lead wires, making sure that the impedances between the both pins and the bypass capacitors are as equal as possible (L1=L1', L2=L2').
- Connect a large-capacity capacitor C1 and a small-capacity capacitor C2 in parallel.
  The capacitance of C2 should be approximately 0.1μF.



Allowable Operating Conditions at Ta = -40°C to +85°C, $V_{SS}1 = V_{SS}2 = 0V$

Parameter	Symbol	Pin/Remarks	Conditions		Specification			
				V_{DD}[V]	min	typ	max	unit
Operating supply voltage (Note 2-1)	VDD(1)	VDD1	0.245μs ≤ tCYC ≤ 200μs		2.7		5.5	V
	VDD(2)		0.367μs ≤ tCYC ≤ 200μs		2.0		5.5	
	VDD(3)		0.735μs ≤ tCYC ≤ 200μs		1.8		5.5	
Memory sustaining supply voltage	VHD	VDD1	RAM and register contents sustained in HOLD mode.		1.6			
High level input voltage	VIH(1)	Port 0,1 P70		1.8 to 5.5	$0.3V_{DD}$ +0.7		V_{DD}	
	VIH(4)	CF1,CF2, $\overline{RES}$		1.8 to 5.5	$0.75V_{DD}$		V_{DD}	
Low level input voltage	VIL(1)	Port 0,1 P70		4.0 to 5.5	V_{SS}		$0.1V_{DD}+0.4$	
				1.8 to 4.0	V_{SS}		$0.2V_{DD}$	
	VIL(4)	CF1,CF2, $\overline{RES}$		1.8 to 5.5	V_{SS}		$0.25V_{DD}$	
Instruction cycle time (Note 2-2)	tCYC (Note 2-2)			2.7 to 5.5	0.245		200	μs
				2.0 to 5.5	0.367		200	
				1.8 to 5.5	0.735		200	
External system clock frequency	FEXCF	CF1	• CF2 pin open • System clock frequency division ratio=1/1 • External system clock duty=50 ± 5%	2.7 to 5.5	0.1		12	MHz
				2.2 to 5.5	0.1		8	
Oscillation frequency range (Note 2-3)	FmCF(1)	CF1,CF2	When 12MHz ceramic oscillation See Fig. 1.	2.7 to 5.5		12		MHz
	FmCF(2)	CF1,CF2	When 8MHz ceramic oscillation See Fig. 1.	2.2 to 5.5		8		
	FmCF(3)	CF1,CF2	When 4MHz ceramic oscillation See Fig. 1.	1.8 to 5.5		4		
	FmFRC(1)		Internal high-speed RC oscillation Ta=-10°C to +85°C (Note 2-4)	1.8 to 5.5	7.76	8.0	8.24	
	FmFRC(2)		Internal high-speed RC oscillation Ta=-40°C to +85°C (Note 2-4)	1.8 to 5.5	7.60	8.0	8.40	
	FmRC		Internal medium-speed RC oscillation	1.8 to 5.5	0.5	1.0	2.0	
	FmSRC		Internal low-speed RC oscillation (Note 2-5)	1.8 to 5.5	27	30	33	kHz
	FsX'tal	XT1,XT2	32.768kHz crystal oscillation See Fig. 2.	1.8 to 5.5		32.768		kHz
	FmPWMRC		Internal high-speed RC oscillation for HPWM2	2.7 to 5.5	38	40	42	MHz
Oscillation Stabilization Time	tmsCF	CF1,CF2	• When oscillation circuit is switched from "oscillation stopped" to "oscillation enabled" . • See Fig. 3.	See Table 1				μs
	tmsFRC (Note 2-4)			1.8 to 5.5			100	
	tmsPWMRC			1.8 to 5.5			100	
	tmsRC			1.8 to 5.5		0		
	tmsSRC (Note2-5)			1.8 to 5.5			1	ms
	tmsX'tal	XT1,XT2		See Table 2				

Note 2-1: V_{DD} must be held greater than or equal to 2.7V in the flash ROM onboard programming mode.

Note 2-2: Relationship between tCYC and oscillation frequency is 3/FmCF at a division ratio of 1/1 and 6/FmCF at a division ratio of 1/2.

Note 2-3: See Tables 1 and 2 for the oscillation constants.

Note 2-4: An oscillation stabilization time of 100μs or longer must be provided before switching the system clock source after the state of the high-speed RC oscillation circuit is switched from "oscillation stopped" to "oscillation enabled" .

Note 2-5: An oscillation stabilization time of 1ms or longer must be provided before switching the system clock source after the state of the low-speed RC oscillation circuit is switched from "oscillation stopped" to "oscillation enabled" .

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

Electrical Characteristics at Ta = -40°C to +85°C, $V_{SS}1 = V_{SS}2 = 0V$

Parameter	Symbol	Pin/Remarks	Conditions		Specification			
				V_{DD}[V]	min	typ	max	unit
High level input current	I_{IH}(1)	Port 0,1, Port 7, $\overline{RES}$	Output disabled Pull-up resistor off $V_{IN}=V_{DD}$ (Including output Tr's off leakage current)	1.8 to 5.5			1	μA
	I_{IH}(2)	CF1	$V_{IN}=V_{DD}$	1.8 to 5.5			15	
Low level input current	I_{IL}(1)	Port 0,1, Port 7, $\overline{RES}$	Output disabled Pull-up resistor off $V_{IN}=V_{SS}$ (Including output Tr's off leakage current)	1.8 to 5.5	-1			
	I_{IL}(2)	CF1	$V_{IN}=V_{SS}$	1.8 to 5.5	-15			
High level output voltage	V_{OH}(1)	Port 0,1, CF2	I_{OH}=-1mA	4.5 to 5.5	V_{DD}-1			V
	V_{OH}(2)		I_{OH}=-0.2mA	1.8 to 5.5	V_{DD}-0.4			
Low level output voltage	V_{OL}(1)	Port 0,1, P70,CF1,CF2	I_{OL}=10mA	4.5 to 5.5			1.5	
	V_{OL}(2)		I_{OL}=1.0mA	1.8 to 5.5			0.4	
Pull-up resistance	Rpu(1)	Port 0,1, P70	$V_{OH}=0.9V_{DD}$	4.5 to 5.5	15	35	80	kΩ
	Rpu(2)			1.8 to 4.5	18	50	230	
	Rpu(3)	$\overline{RES}$		1.8 to 5.5	300	400	500	
Hysteresis voltage	VHYS(1)	Port 0,1, P70 $\overline{RES}$		2.7 to 5.5		$0.1V_{DD}$		V
				1.8 to 5.5		$0.07V_{DD}$		
Pin capacitance	CP	All pins	For pins other than that under test: $V_{IN}=V_{SS}$ f=1MHz Ta=25°C	1.8 to 5.5		10		pF

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

AD Converter Characteristics at $V_{SS}1 = V_{SS}2 = 0V$

<12bits AD Converter Mode/Ta = -40°C to +85°C >

Parameter	Symbol	Pin/Remarks	Conditions	Specification				
				V_{DD}[V]	min	typ	max	unit
Resolution	N	AN2(P02) AN3(P03) AN4(P04) AN5(P15) AN6(P14) AN7(P13) AN9(P70) (Note 6-3)		1.8 to 5.5		12		bit
Absolute accuracy	ET		(Note 6-1)	1.8 to 5.5			±16	LSB
Conversion time	TCAD		• See conversion time calculation method. (Note 6-2)	2.7 to 5.5	32		115	μs
				2.2 to 5.5	134		215	
				1.8 to 5.5	400		430	
Analog input voltage range	VAIN(1)		When V_{DD} is selected	1.8 to 5.5	V_{SS}		V_{DD}	V
	VAIN(2)		When internal VREF=4V is selected. VREF≤V_{DD}	4.3 to 5.5	V_{SS}		VREF	
			When internal VREF=2V is selected VREF≤V_{DD}	2.3 to 3.6	V_{SS}		VREF	
Analog port input current	IAINH		VAIN=V_{DD}	1.8 to 5.5			1	μA
	IAINL		VAIN=V_{SS}	1.8 to 5.5	-1			

<8bits AD Converter Mode/Ta = -40°C to +85°C >

Parameter	Symbol	Pin/Remarks	Conditions	Specification				
				V_{DD}[V]	min	typ	max	unit
Resolution	N	AN2(P02) AN3(P03) AN4(P04) AN5(P15) AN6(P14) AN7(P13) AN9(P70) (Note 6-3)		1.8 to 5.5		8		bit
Absolute accuracy	ET		(Note 6-1)	1.8 to 5.5			±1.5	LSB
Conversion time	TCAD		• See conversion time calculation method. (Note 6-2)	2.7 to 5.5	20		90	μs
				2.2 to 5.5	80		135	
				1.8 to 5.5	245		265	
Analog input voltage range	VAIN(1)		When V_{DD} is selected	1.8 to 5.5	V_{SS}		V_{DD}	V
	VAIN(2)		When internal VREF=4V is selected. VREF≤V_{DD}	4.3 to 5.5	V_{SS}		VREF	
			When internal VREF=2V is selected. VREF≤V_{DD}	2.3 to 3.6	V_{SS}		VREF	
Analog port input current	IAINH		VAIN=V_{DD}	1.8 to 5.5			1	μA
	IAINL		VAIN=V_{SS}	1.8 to 5.5	-1			

<Conversion time calculation method>

12bits AD Converter Mode: TCAD(Conversion time) = ((52/(AD division ratio))+2)×(1/3)×tCYC

8bits AD Converter Mode: TCAD(Conversion time) = ((32/(AD division ratio))+2)× (1/3)×tCYC

10x/20x Amplifier Characteristics at Ta = -40°C to +85°C, $V_{SS}1 = V_{SS}2 = 0V$

Parameter	Symbol	Pin/Remarks	Conditions		V_{DD}[V]	Specification min	typ	max	unit
20x Amplifier gain	APGAIN20 See Fig7	P00/APIM P01/APIP	• Ta=-40 to +85°C 1)APDIR=0 & GAIN20=1. • P01=0V,P00≤0V or P00=0V,P01≥0V 2)APDIR=1 & GAIN20=1. • P01=0V,P00≥0V or P00=0V,P01≤0V		4.3 to 5.0		20		
20x Amplifier offset	VAPIO20					200		600	mV
20x Amplifier input voltage range	VAPIM20-1	P00/APIM	1)	P01/APIP=0V		-0.17		0	V
	VAPIP20-1	P01/APIP		P00/APIM=0V		0		0.17	
	VAPIM20-2	P00/APIM	2)	P01/APIP=0V		0		0.17	V
	VAPIP20-2	P01/APIP		P00/APIM=0V		-0.17		0	
10x Amplifier gain	APGAIN10 See Fig7	P00/APIM P01/APIP	• Ta=-40 to +85°C 3)APDIR=0 & GAIN20=0. • P01=0V,P00≤0V or P00=0V,P01≥0V 4)APDIR=1 & GAIN20=0. • P01=0V,P00≥0V or P00=0V,P01≤0V				10		
10x Amplifier offset	VAPIO10					100		300	mV
10x Amplifier input voltage range	VAPIM10-3	P00/APIM	3)	P01/APIP=0V		-0.24		0	V
	VAPIP10-3	P01/APIP		P00/APIM=0V		0		0.24	
	VAPIM10-4	P00/APIM	4)	P01/APIP=0V		0		0.24	V
	VAPIP10-4	P01/APIP		P00/APIM=0V		-0.24		0	
Amplifier input port input current	IAPINL	P00/APIM	P00/APIM=V_{SS}-0.2V			-1			μA
	IAPINH	P01/APIP	P01/APIP=V_{DD}					1	
Operation stabilization time (Note 8-1)	tAPW							20	μs

Note 8-1: Refers to the interval between the time APON is set to 1 and the time operation gets stabilized.

<Amplifier input vaoltage calculation method:See Fig7>

VAPFUL = (VREFAD - VAPIO) / APGAIN

(VREFAD can be selected from internal-VREF4V, internal-VREF2V and V_{DD}.)

Note: VAPFUL must not exceed VAPIP or VAPIM.

Consumption Current Characteristics at Ta = -40°C to +85°C, $V_{SS}1 = V_{SS}2 = 0V$

Parameter	Symbol	Pin / Remarks	Conditions	V_{DD}[V]	Specification min	typ	max	unit
Normal mode consumption current (Note 13-1) (Note 13-2)	IDDOP(1)	$V_{DD}1$	• FmCF=8MHz ceramic oscillation mode • System clock set to 8MHz mode • Internal low-/medium-speed RC oscillation stopped • Internal high-speed RC oscillation stopped • Frequency division ratio set to 1/1	2.2 to 5.5		3.8	5.2	mA
				2.2 to 3.6		2.2	2.9	
	IDDOP(2)		• FmCF=4MHz ceramic oscillation mode • System clock set to 4MHz mode • Internal low-/medium-speed RC oscillation stopped • Internal high-speed RC oscillation stopped • Frequency division ratio set to 1/1	1.8 to 5.5		2.1	3.5	
				1.8 to 3.6		1.1	1.7	
	IDDOP(3)		• FsX'tal=32.768kHz crystal oscillation mode • Internal low-speed RC oscillation stopped • System clock set to internal medium-speed RC oscillation mode • Internal high-speed RC oscillation stopped • Frequency division ratio set to 1/2	1.8 to 5.5		0.23	0.39	
				1.8 to 3.6		0.13	0.19	
	IDDOP(4)		• FsX'tal=32.768kHz crystal oscillation mode • Internal low-/medium-speed RC oscillation stopped • System clock set to internal high-speed RC oscillation mode • Frequency division ratio set to 1/1	1.8 to 5.5		2.7	3.6	
				1.8 to 3.6		1.7	2.3	
	IDDOP(5)		• External oscillation FsX'tal/FmCF stopped • System clock set to internal low-speed RC oscillation mode • Internal medium-speed RC oscillation stopped • Internal high-speed RC oscillation stopped • Frequency division ratio set to 1/1	1.8 to 5.5		10	42	μA
				1.8 to 3.6		6	21	
	IDDOP(6)		• FsX'tal=32.768kHz crystal oscillation mode • System clock set to 32.768kHz mode • Internal low-/medium-speed RC oscillation stopped • Internal high-speed RC oscillation stopped • Frequency division ratio set to 1/2	1.8 to 5.5		46	101	
				1.8 to 3.6		16	40	

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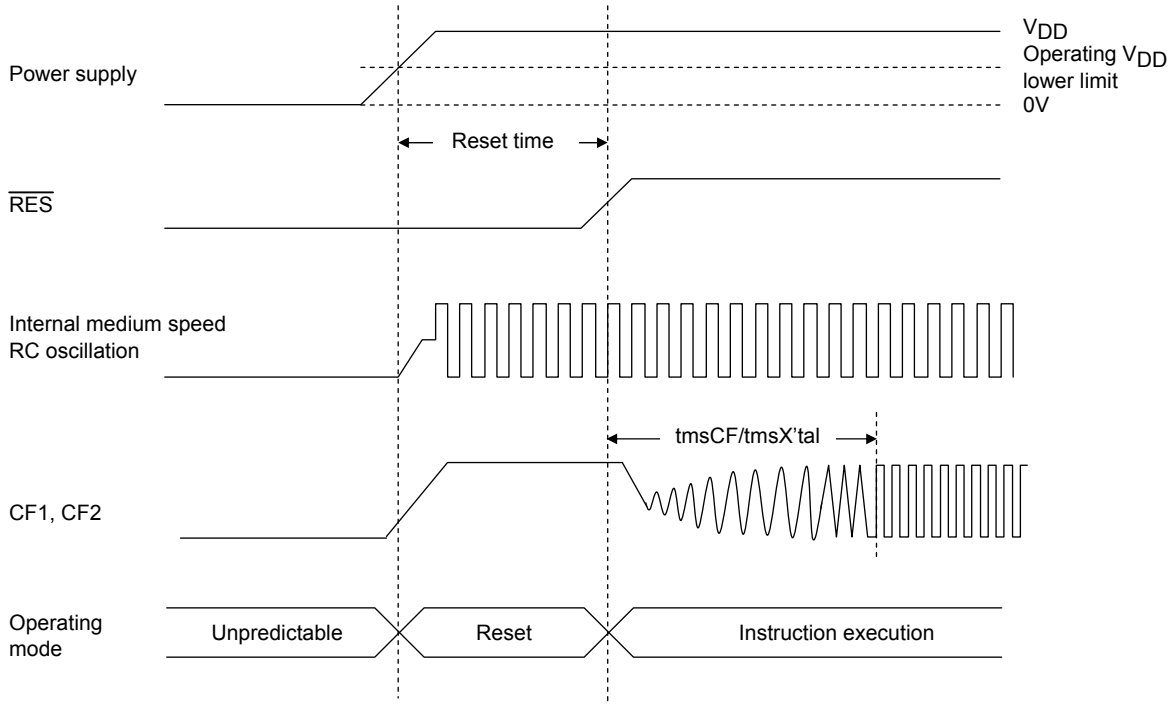
Parameter	Symbol	Pin / Remarks	Conditions	V_{DD}[V]	Specification min	Typ	max	unit
HALT mode consumption current (Note 13-1) (Note 13-2)	IDDHALT(1)	V_{DD}1	HALT mode • FmCF=8MHz ceramic oscillation mode • System clock set to 8MHz mode • Internal low-/medium-speed RC oscillation stopped • Internal high-speed RC oscillation stopped • Frequency division ratio set to 1/1	2.2 to 5.5		2.0	3.2	mA
				2.2 to 3.6		1.0	1.6	
	IDDHALT(2)		HALT mode • FmCF=4MHz ceramic oscillation mode • System clock set to 4MHz mode • Internal low-/medium-speed RC oscillation stopped • Internal high-speed RC oscillation stopped • Frequency division ratio set to 1/1	1.8 to 5.5		1.2	2.4	
				1.8 to 3.6		0.5	1.0	
	IDDHALT(3)		HALT mode • FsX'tal=32.768kHz crystal oscillation mode • Internal low-speed RC oscillation stopped • System clock set to internal medium-speed RC oscillation mode • Internal high-speed RC oscillation stopped • Frequency division ratio set to 1/2	1.8 to 5.5		0.12	0.25	
				1.8 to 3.6		0.06	0.11	
	IDDHALT(4)		HALT mode • FsX'tal=32.768kHz crystal oscillation mode • Internal low-/medium-speed RC oscillation stopped • System clock set to internal high-speed RC oscillation mode • Frequency division ratio set to 1/1	1.8 to 5.5		1.1	1.7	
				1.8 to 3.6		0.7	1.0	
	IDDHALT(5)		HALT mode • External oscillation FsX'tal/FmCF stopped • System clock set to internal low-speed RC oscillation mode • Internal medium-speed RC oscillation stopped • Internal high-speed RC oscillation stopped • Frequency division ratio set to 1/1	1.8 to 5.5		3.8	37	μA
				1.8 to 3.6		2.4	17	
	IDDHALT(6)		HALT mode • FsX'tal=32.768kHz crystal oscillation mode • System clock set to 32.768kHz mode • Internal low-/medium-speed RC oscillation stopped • Internal high-speed RC oscillation stopped • Frequency division ratio set to 1/2	1.8 to 5.5		42	97	
				1.8 to 3.6		13	38	
HOLD mode consumption current (Note 13-1) (Note 13-2)	IDDHOLD(1)	V_{DD}1	HOLD mode	1.8 to 5.5		0.023	33.2	μA
				1.8 to 3.6		0.012	14.2	
	IDDHOLD(2)		HOLD mode • LVD option selected	1.8 to 5.5		1.09	26.9	
				1.8 to 3.6		0.86	11.8	
Timer HOLD mode consumption current (Note 13-1) (Note 13-2)	IDDHOLD(3)	V_{DD}1	Timer HOLD mode • FsX'tal=32.768kHz crystal oscillation mode	1.8 to 5.5		39	94	
				1.8 to 3.6		12	36	
	IDDHOLD(4)		Timer HOLD mode • FmSRC=30kHz internal low-speed RC oscillation mode	1.8 to 5.5		0.63	34	
				1.8 to 3.6		0.53	15	

Note 13-1: The consumption current value includes none of the currents that flow into the output transistors and internal pull-up resistors.

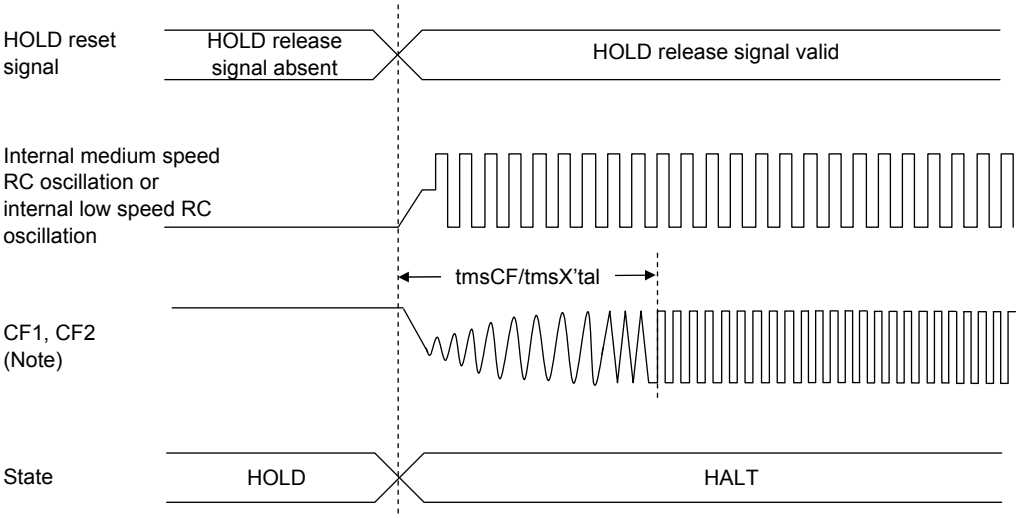
Note 13-2: Unless otherwise specified, the consumption current for the LVD circuit is not included.

F-ROM Programming Characteristics at Ta = +10°C to +55°C, $V_{SS}1 = V_{SS}2 = 0V$

Parameter	Symbol	Pin/Remarks	Conditions		Specification			
				V_{DD}[V]	min	typ	max	unit
Onboard programming current	IDDFW(1)	$V_{DD}1$	• Excluding power dissipation in the microcontroller block	2.2 to 5.5		5	10	mA
Programming time	tFW(1)		• Erasing time	2.2 to 5.5		20	30	ms
	tFW(2)		• Programming time			40	60	μs



Reset Time and Oscillation Stabilization Time



HOLD Release Signal and Oscillation Stabilization Time

Note: When an external oscillation circuit is selected.

Figure 3 Oscillation Stabilization Time

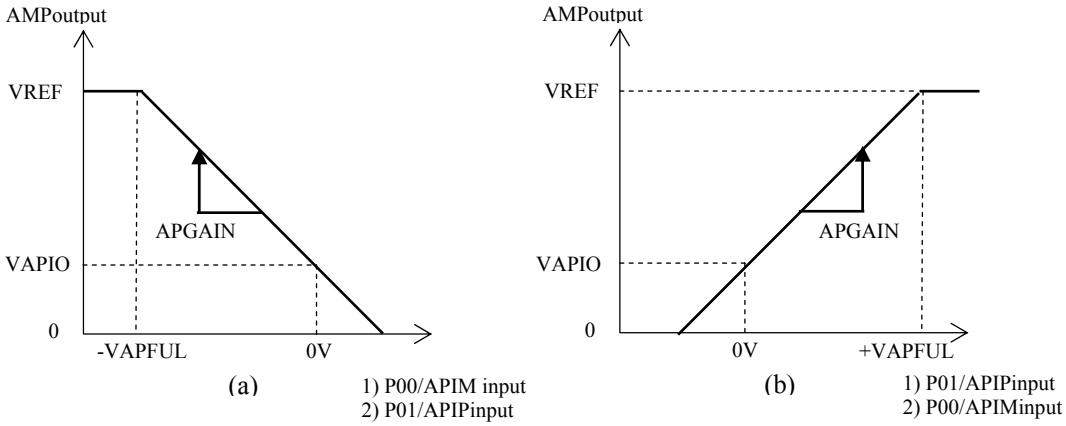


Figure 7 10×/20× Amplifier Characteristics

(a) 1) When P01/APIP is 0V, P00/APIM ≤ 0V.
2) When P00/APIM is 0V, P01/APIP ≤ 0V.

(b) 1) When P00/APIM is 0V, P01/APIP ≥ 0V.
2) When P01/APIP is 0V, P00/APIM ≥ 0V.

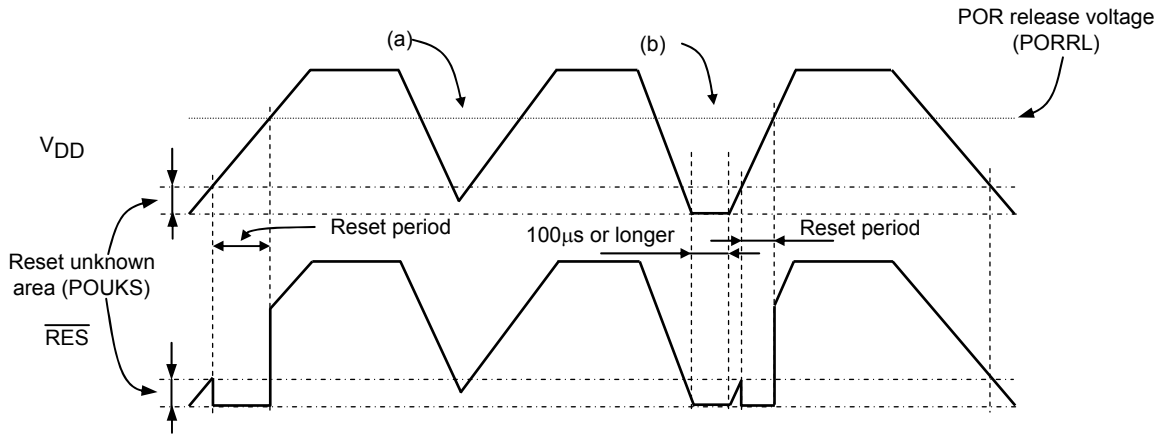


Figure 8 Example of POR Only (LVD Deselected) Mode Waveforms (at Reset Pin with R_{RES} Pull-up Resistor Only)

- The POR function generates a reset only when the power voltage goes up from the V_{SS} level.
- No stable reset will be generated if power is turned on again when the power level does not go down to the V_{SS} level as shown in (a). If such a case is anticipated, use the LVD function together with the POR function or implement an external reset circuit as shown below.
- A reset is generated only when the power level goes down to the V_{SS} level as shown in (b) and power is turned on again after this condition continues for 100µs or longer.

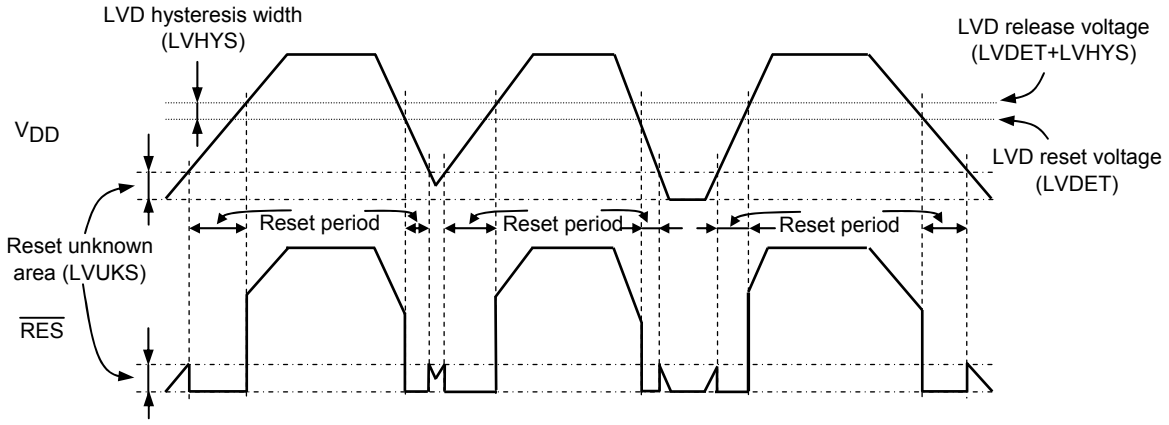


Figure 9 Example of POR + LVD Mode Waveforms (at Reset Pin with R_{RES} Pull-up Resistor Only)

- Resets are generated both when power is turned on and when the power level lowers.
- A hysteresis width (LVHYS) is provided to prevent the repetitions of reset release and entry cycles near the detection level.

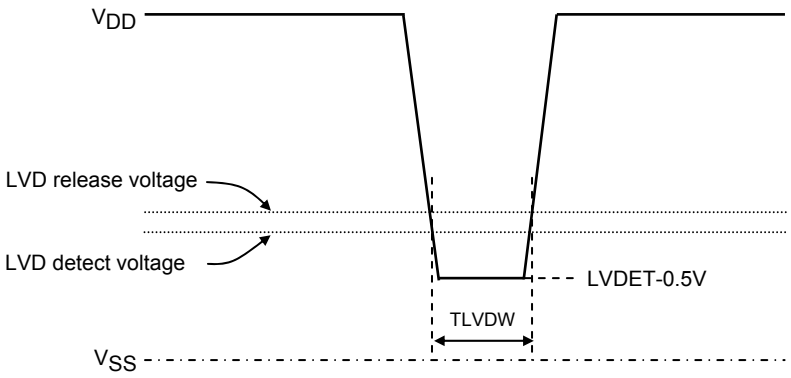


Figure 10 Minimum Low Voltage Detection Width (Example of Voltage Sag/Fluctuation Waveform)

ORDERING INFORMATION

Device	Package	Shipping (Qty / Packing)
LC87F0G08AUJA-AH	SSOP24(225mil) (Pb-Free / Halogen Free)	2000 / Tape & Reel
LC87F0G08AUJA-FH	SSOP24(225mil) (Pb-Free / Halogen Free)	2000 / Tape & Reel
LC87F0G08AUJA-ZH	SSOP24(225mil) (Pb-Free / Halogen Free)	1400 / Fan-Fold