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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Obsolete
Core Processor	R8C
Core Size	16-Bit
Speed	16MHz
Connectivity	SIO, UART/USART
Peripherals	LED, WDT
Number of I/O	22
Program Memory Size	8KB (8K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	512 x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	32-LQFP
Supplier Device Package	32-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f21122dfp-u0

1. Overview

This MCU is built using the high-performance silicon gate CMOS process using a R8C Tiny Series CPU core and is packaged in a 32-pin plastic molded LQFP. This MCU operates using sophisticated instructions featuring a high level of instruction efficiency. With 1M bytes of address space, it is capable of executing instructions at high speed.

The data flash ROM (2 KB X 2 blocks) is embedded.

1.1 Applications

Electric household appliance, office equipment, housing equipment (sensor, security), general industrial equipment, audio, etc.

1.3 Block Diagram

Figure 1.1. shows this MCU block diagram.

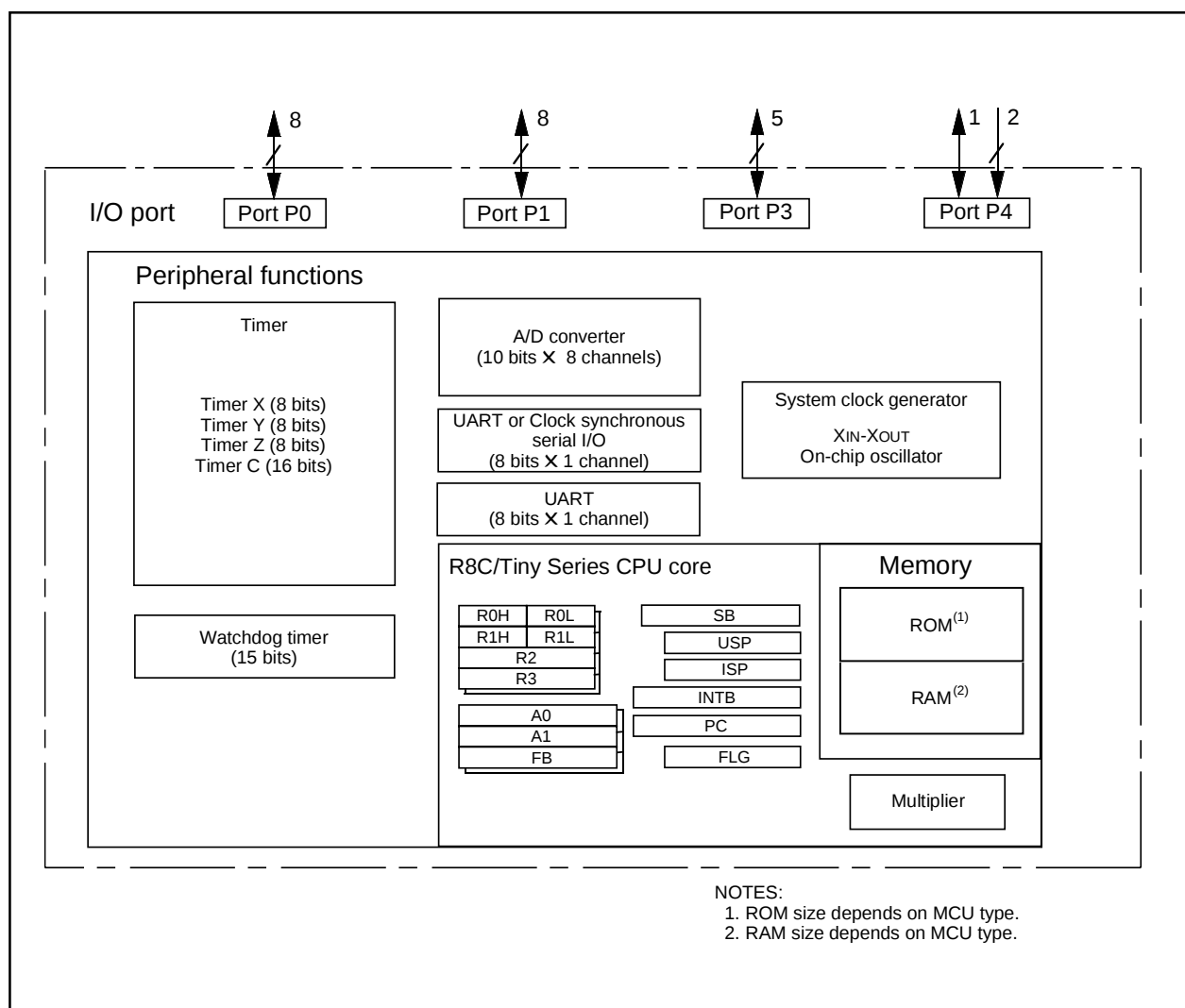


Figure 1.1 Block Diagram

1.4 Product Information

Table 1.2 lists the product information.

Table 1.2 Product Information

As of January 2006

Type No.	ROM capacity		RAM capacity	Package type	Remarks
	Program ROM	Data flash			
R5F21122FP	8K bytes	2K bytes x 2	512 bytes	PLQP0032GB-A	Flash memory version
R5F21123FP	12K bytes	2K bytes x 2	768 bytes	PLQP0032GB-A	
R5F21124FP	16K bytes	2K bytes x 2	1K bytes	PLQP0032GB-A	
R5F21122DFP	8K bytes	2K bytes x 2	512 bytes	PLQP0032GB-A	D version
R5F21123DFP	12K bytes	2K bytes x 2	768 bytes	PLQP0032GB-A	
R5F21124DFP	16K bytes	2K bytes x 2	1K bytes	PLQP0032GB-A	

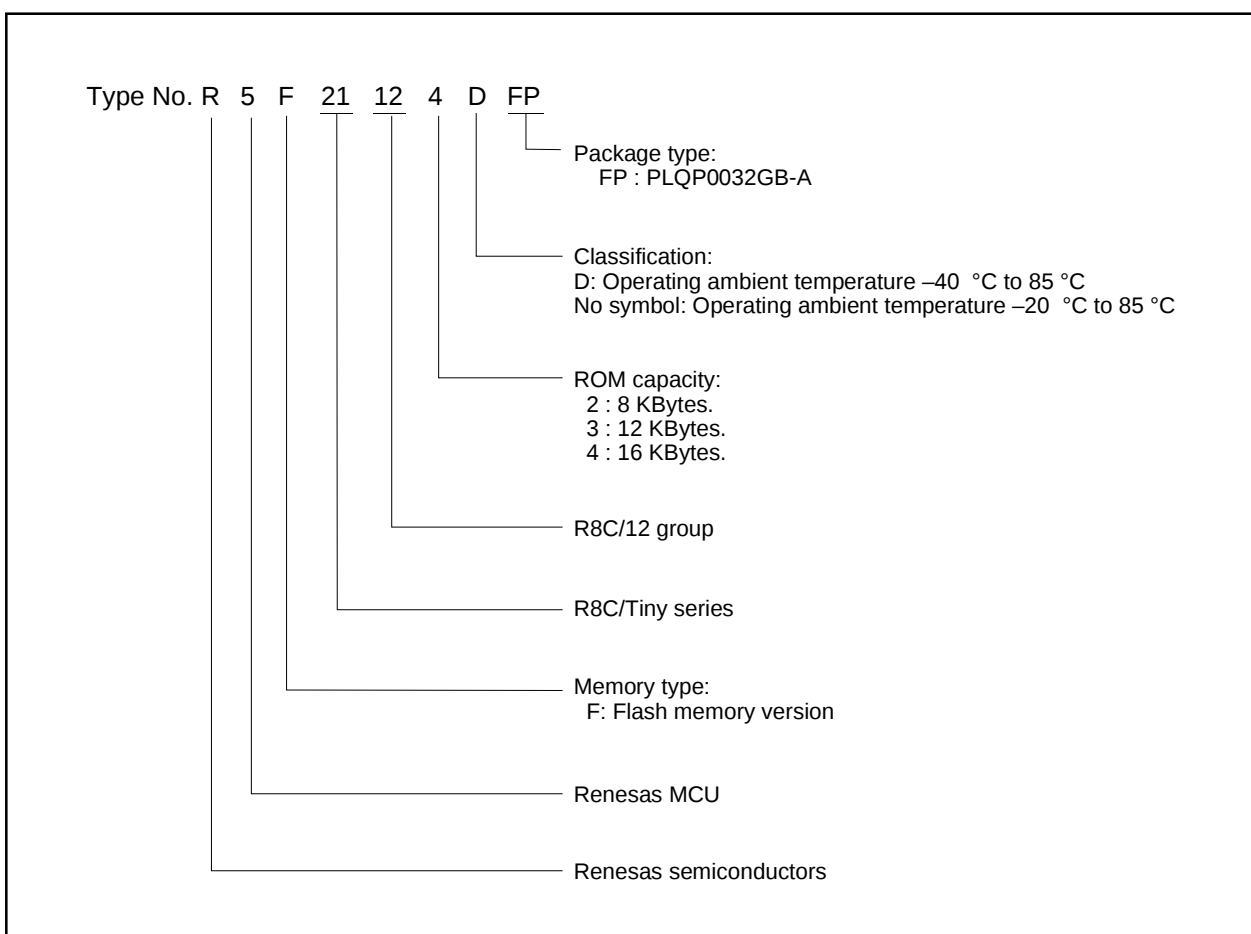


Figure 1.2 Type No., Memory Size, and Package

1.5 Pin Assignments

Figure 1.3 shows the pin configuration (top view).

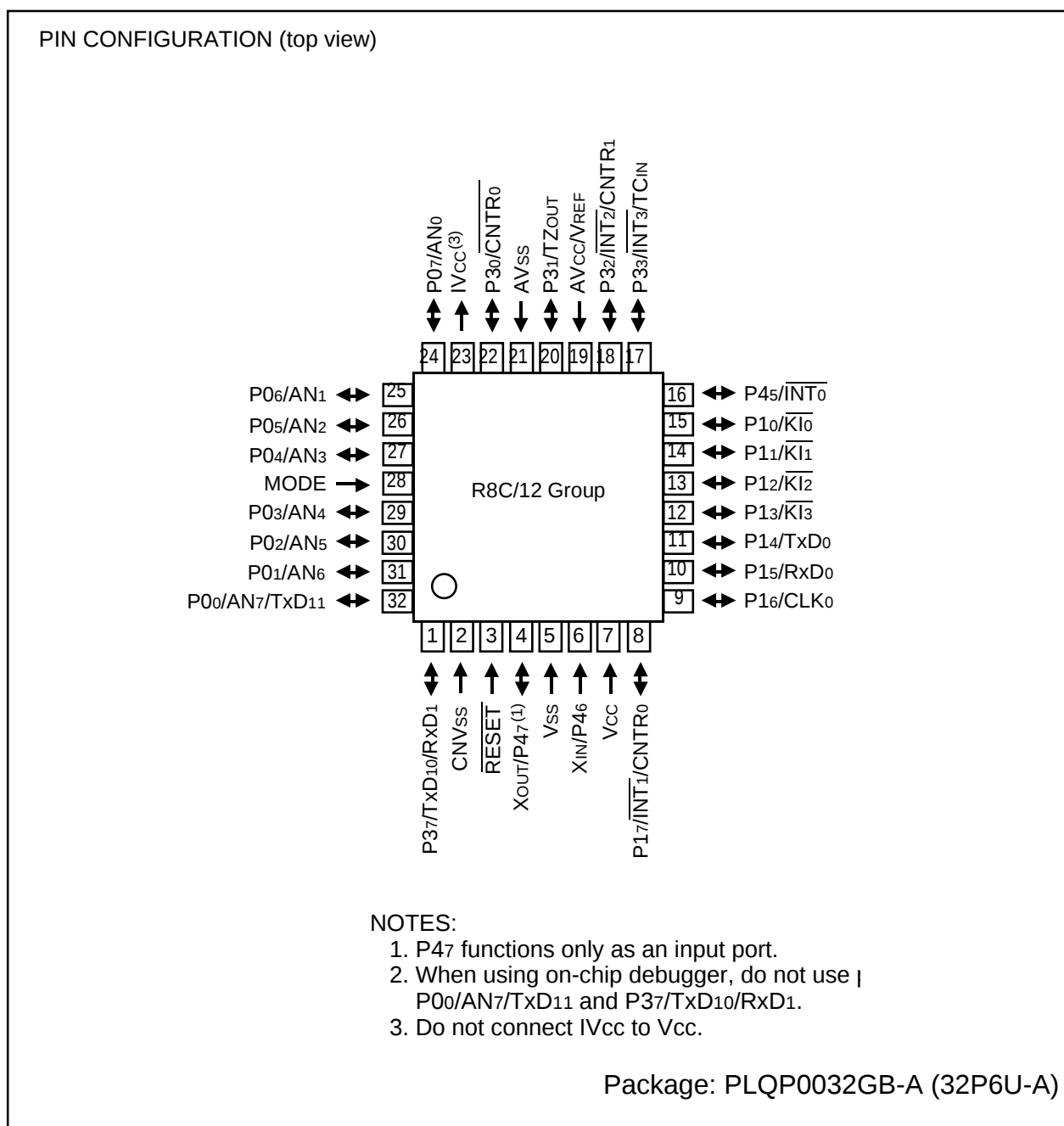


Figure 1.3 Pin Configuration (Top View)

1.6 Pin Description

Table 1.3 shows the pin description

Table 1.3 Pin description

Signal name	Pin name	I/O type	Function
Power supply input	Vcc, Vss	I	Apply 2.7 V to 5.5 V to the Vcc pin. Apply 0 V to the Vss pin.
IVcc	IVcc	O	This pin is to stabilize internal power supply. Connect this pin to Vss via a capacitor (0.1 μ F). Do not connect to Vcc.
Analog power supply input	AVcc, AVss	I	Power supply input pins for A/D converter. Connect the AVcc pin to Vcc. Connect the AVss pin to Vss. Connect a capacitor between pins AVcc and AVss.
Reset input	RESET	I	Input "L" on this pin resets the MCU.
CNVss	CNVss	I	Connect this pin to Vss via a resistor.
MODE	MODE	I	Connect this pin to Vcc via a resistor.
Main clock input	XIN	I	These pins are provided for the main clock generating circuit I/O. Connect a ceramic resonator or a crystal oscillator between the XIN and XOUT pins. To use an externally derived clock, input it to the XIN pin and leave the XOUT pin open.
Main clock output	XOUT	O	
INT interrupt input	INT0 to INT3	I	INT interrupt input pins.
Key input interrupt	KI0 to KI3	I	Key input interrupt pins.
Timer X	CNTR0	I/O	Timer X I/O pin
	CNTR0	O	Timer X output pin
Timer Y	CNTR1	I/O	Timer Y I/O pin
Timer Z	TZOUT	O	Timer Z output pin
Timer C	TCIN	I	Timer C input pin
Serial interface	CLK0	I/O	Transfer clock I/O pin.
	RxD0, RxD1	I	Serial data input pins.
	TxD0, TxD10, TxD11	O	Serial data output pins.
Reference voltage input	VREF	I	Reference voltage input pin for A/sD converter. Connect the VREF pin to Vcc.
A/D converter	AN0 to AN7	I	Analog input pins for A/D converter
I/O port	P00 to P07, P10 to P17, P30 to P33, P37, P45	I/O	These are 8-bit CMOS I/O ports. Each port has an input/output select direction register, allowing each pin in that port to be directed for input or output individually. Any port set to input can select whether to use a pull-up resistor or not by program. P10 to P17 also function as LED drive ports.
Input port	P46, P47	I	Port for input-only.

3. Memory

Figure 3.1 is a memory map of this MCU. This MCU provides 1-Mbyte address space from addresses 00000₁₆ to FFFFF₁₆.

The internal ROM (program ROM) is allocated lower addresses beginning with address 0FFFF₁₆. For example, a 16-Kbyte internal ROM is allocated addresses from 0C000₁₆ to 0FFFF₁₆.

The fixed interrupt vector table is allocated addresses 0FFDC₁₆ to 0FFFF₁₆. They store the starting address of each interrupt routine.

The internal ROM (data flash) is allocated addresses from 02000₁₆ to 02FFF₁₆.

The internal RAM is allocated higher addresses beginning with address 00400₁₆. For example, a 1-Kbyte internal RAM is allocated addresses 00400₁₆ to 007FF₁₆. The internal RAM is used not only for storing data, but for calling subroutines and stacks when interrupt request is acknowledged.

Special function registers (SFR) are allocated addresses 00000₁₆ to 002FF₁₆. The peripheral function control registers are located there. All addresses, which have nothing allocated within the SFR, are reserved area and cannot be accessed by users.

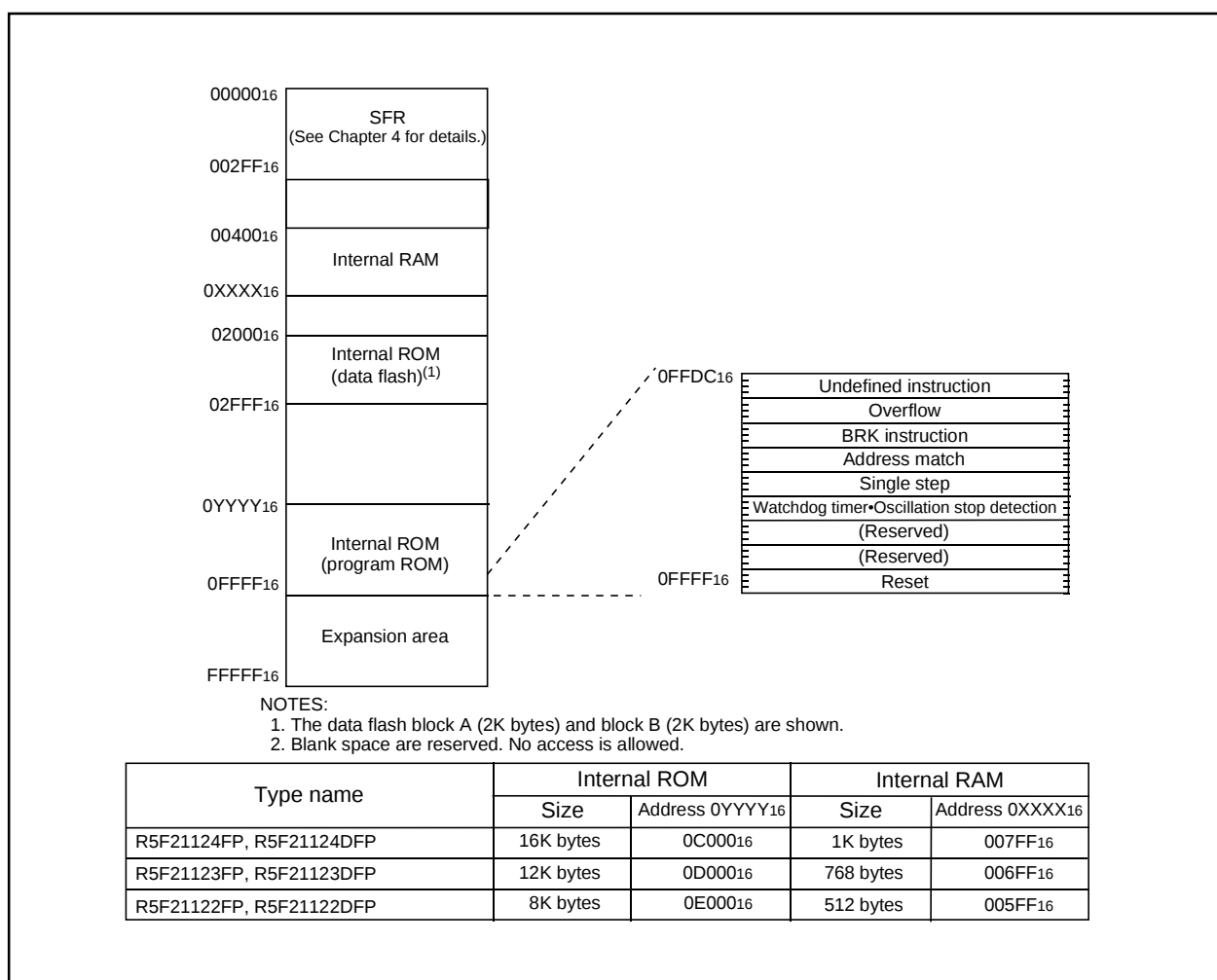


Figure 3.1 Memory Map

4. Special Function Register (SFR)

SFR(Special Function Register) is the control register of peripheral functions. Tables 4.1 to 4.4 list the SFR information

Table 4.1 SFR Information(1)(1)

Address	Register	Symbol	After reset
0000 ₁₆			
0001 ₁₆			
0002 ₁₆			
0003 ₁₆			
0004 ₁₆	Processor mode register 0	PM0	XXXX0X002
0005 ₁₆	Processor mode register 1	PM1	00XXX0X02
0006 ₁₆	System clock control register 0	CM0	011010002
0007 ₁₆	System clock control register 1	CM1	001000002
0008 ₁₆			
0009 ₁₆	Address match interrupt enable register	AIER	XXXXXX002
000A ₁₆	Protect register	PRCR	00XXX0002
000B ₁₆			
000C ₁₆	Oscillation stop detection register	OCD	000001002
000D ₁₆	Watchdog timer reset register	WDTR	XX16
000E ₁₆	Watchdog timer start register	WDTS	XX16
000F ₁₆	Watchdog timer control register	WDC	000111112
0010 ₁₆	Address match interrupt register 0	RMAD0	0016
0011 ₁₆			0016
0012 ₁₆			X016
0013 ₁₆			
0014 ₁₆	Address match interrupt register 1	RMAD1	0016
0015 ₁₆			0016
0016 ₁₆			X016
0017 ₁₆			
0018 ₁₆			
0019 ₁₆			
001A ₁₆			
001B ₁₆			
001C ₁₆			
001D ₁₆			
001E ₁₆	INT0 input filter select register	INT0F	XXXXX0002
001F ₁₆			
0020 ₁₆			
0021 ₁₆			
0022 ₁₆			
0023 ₁₆			
0024 ₁₆			
0025 ₁₆			
0026 ₁₆			
0027 ₁₆			
0028 ₁₆			
0029 ₁₆			
002A ₁₆			
002B ₁₆			
002C ₁₆			
002D ₁₆			
002E ₁₆			
002F ₁₆			
0030 ₁₆			
0031 ₁₆			
0032 ₁₆			
0033 ₁₆			
0034 ₁₆			
0035 ₁₆			
0036 ₁₆			
0037 ₁₆			
0038 ₁₆			
0039 ₁₆			
003A ₁₆			
003B ₁₆			
003C ₁₆			
003D ₁₆			
003E ₁₆			
003F ₁₆			

NOTES :

1. Blank spaces are reserved. No access is allowed.

X : Undefined

Table 4.2 SFR Information(2)⁽¹⁾

Address	Register	Symbol	After reset
0040 ₁₆			
0041 ₁₆			
0042 ₁₆			
0043 ₁₆			
0044 ₁₆			
0045 ₁₆			
0046 ₁₆			
0047 ₁₆			
0048 ₁₆			
0049 ₁₆			
004A ₁₆			
004B ₁₆			
004C ₁₆			
004D ₁₆	Key input interrupt control register	KUPIC	XXXXX0002
004E ₁₆	AD conversion interrupt control register	ADIC	XXXXX0002
004F ₁₆			
0050 ₁₆			
0051 ₁₆	UART0 transmit interrupt control register	S0TIC	XXXXX0002
0052 ₁₆	UART0 receive interrupt control register	S0RIC	XXXXX0002
0053 ₁₆	UART1 transmit interrupt control register	S1TIC	XXXXX0002
0054 ₁₆	UART1 receive interrupt control register	S1RIC	XXXXX0002
0055 ₁₆	INT2 interrupt control register	INT2IC	XXXXX0002
0056 ₁₆	Timer X interrupt control register	TXIC	XXXXX0002
0057 ₁₆	Timer Y interrupt control register	TYIC	XXXXX0002
0058 ₁₆	Timer Z interrupt control register	TZIC	XXXXX0002
0059 ₁₆	INT1 interrupt control register	INT1IC	XXXXX0002
005A ₁₆	INT3 interrupt control register	INT3IC	XXXXX0002
005B ₁₆	Timer C interrupt control register	TCIC	XXXXX0002
005C ₁₆			
005D ₁₆	INT0 interrupt control register	INT0IC	XX00X0002
005E ₁₆			
005F ₁₆			
0060 ₁₆			
0061 ₁₆			
0062 ₁₆			
0063 ₁₆			
0064 ₁₆			
0065 ₁₆			
0066 ₁₆			
0067 ₁₆			
0068 ₁₆			
0069 ₁₆			
006A ₁₆			
006B ₁₆			
006C ₁₆			
006D ₁₆			
006E ₁₆			
006F ₁₆			
0070 ₁₆			
0071 ₁₆			
0072 ₁₆			
0073 ₁₆			
0074 ₁₆			
0075 ₁₆			
0076 ₁₆			
0077 ₁₆			
0078 ₁₆			
0079 ₁₆			
007A ₁₆			
007B ₁₆			
007C ₁₆			
007D ₁₆			
007E ₁₆			
007F ₁₆			

NOTES :

1. Blank spaces are reserved. No access is allowed.

X : Undefined

Table 4.3 SFR Information(3)(4)

Address	Register	Symbol	After reset
0080 ₁₆	Timer Y, Z mode register	TYZMR	0016
0081 ₁₆	Prescaler Y register	PREY	FF16
0082 ₁₆	Timer Y secondary register	TYSC	FF16
0083 ₁₆	Timer Y primary register	TYPR	FF16
0084 ₁₆	Timer Y, Z waveform output control register	PUM	0016
0085 ₁₆	Prescaler Z register	PREZ	FF16
0086 ₁₆	Timer Z secondary register	TZSC	FF16
0087 ₁₆	Timer Z primary register	TZPR	FF16
0088 ₁₆			
0089 ₁₆			
008A ₁₆	Timer Y, Z output control register	TYZOC	0016
008B ₁₆	Timer X mode register	TXMR	0016
008C ₁₆	Prescaler X register	PREX	FF16
008D ₁₆	Timer X register	TX	FF16
008E ₁₆	Timer count source setting register	TCSS	0016
008F ₁₆			
0090 ₁₆	Timer C register	TC	0016
0091 ₁₆			0016
0092 ₁₆			
0093 ₁₆			
0094 ₁₆			
0095 ₁₆			
0096 ₁₆	External input enable register	INTEN	0016
0097 ₁₆			
0098 ₁₆	Key input enable register	KIEN	0016
0099 ₁₆			
009A ₁₆	Timer C control register 0	TCC0	0016
009B ₁₆	Timer C control register 1	TCC1	0016
009C ₁₆	Capture register	TM0	0016
009D ₁₆			0016
009E ₁₆			
009F ₁₆			
00A0 ₁₆	UART0 transmit/receive mode register	U0MR	0016
00A1 ₁₆	UART0 bit rate register	U0BRG	XX16
00A2 ₁₆	UART0 transmit buffer register	U0TB	XX16
00A3 ₁₆			XX16
00A4 ₁₆	UART0 transmit/receive control register 0	U0C0	000010002
00A5 ₁₆	UART0 transmit/receive control register 1	U0C1	000000102
00A6 ₁₆	UART0 receive buffer register	U0RB	XX16
00A7 ₁₆			XX16
00A8 ₁₆	UART1 transmit/receive mode register	U1MR	0016
00A9 ₁₆	UART1 bit rate generator	U1BRG	XX16
00AA ₁₆	UART1 transmit buffer register	U1TB	XX16
00AB ₁₆			XX16
00AC ₁₆	UART1 transmit/receive control register 0	U1C0	000010002
00AD ₁₆	UART1 transmit/receive control register 1	U1C1	000000102
00AE ₁₆	UART1 receive buffer register	U1RB	XX16
00AF ₁₆			XX16
00B0 ₁₆	UART transmit/receive control register 2	UCON	0016
00B1 ₁₆			
00B2 ₁₆			
00B3 ₁₆			
00B4 ₁₆			
00B5 ₁₆			
00B6 ₁₆			
00B7 ₁₆			
00B8 ₁₆			
00B9 ₁₆			
00BA ₁₆			
00BB ₁₆			
00BC ₁₆			
00BD ₁₆			
00BE ₁₆			
00BF ₁₆			

NOTES :

1. Blank spaces are reserved. No access is allowed.

X : Undefined

Table 5.3 A/D Conversion Characteristics

Symbol	Parameter		Measuring condition	Standard			Unit
				Min.	Typ.	Max.	
—	Resolution		$V_{ref} = V_{CC}$	—	—	10	Bit
—	Absolute accuracy	10 bit mode	$\phi_{AD} = 10 \text{ MHz}$, $V_{ref} = V_{CC} = 5.0 \text{ V}$	—	—	± 3	LSB
		8 bit mode	$\phi_{AD} = 10 \text{ MHz}$, $V_{ref} = V_{CC} = 5.0 \text{ V}$	—	—	± 2	LSB
		10 bit mode	$\phi_{AD} = 10 \text{ MHz}$, $V_{ref} = V_{CC} = 3.3 \text{ V}^{(3)}$	—	—	± 5	LSB
		8 bit mode	$\phi_{AD} = 10 \text{ MHz}$, $V_{ref} = V_{CC} = 3.3 \text{ V}^{(3)}$	—	—	± 2	LSB
R_{LADDER}	Ladder resistance		$V_{REF} = V_{CC}$	10	—	40	$k\Omega$
t_{CONV}	Conversion time	10 bit mode	$\phi_{AD} = 10 \text{ MHz}$, $V_{ref} = V_{CC} = 5.0 \text{ V}$	3.3	—	—	μs
		8 bit mode	$\phi_{AD} = 10 \text{ MHz}$, $V_{ref} = V_{CC} = 5.0 \text{ V}$	2.8	—	—	μs
V_{REF}	Reference voltage			—	$V_{CC}^{(4)}$	—	V
V_{IA}	Analog input voltage			0	—	V_{ref}	V
—	A/D operating clock frequency ⁽²⁾	Without sample & hold		0.25	—	10	MHz
		With sample & hold		1.0	—	10	MHz

NOTES:

1. $V_{CC} = AV_{CC} = 2.7$ to 5.5 V at $T_{opr} = -20$ to 85°C / -40 to 85°C , unless otherwise specified.
2. If f_{AD} exceeds 10 MHz , divide the f_{AD} and hold A/D operating clock frequency (ϕ_{AD}) 10 MHz or below.
3. If the AV_{CC} is less than 4.2 V , divide the f_{AD} and hold A/D operating clock frequency (ϕ_{AD}) $f_{AD}/2$ or below.
4. Hold $V_{CC} = V_{ref}$.

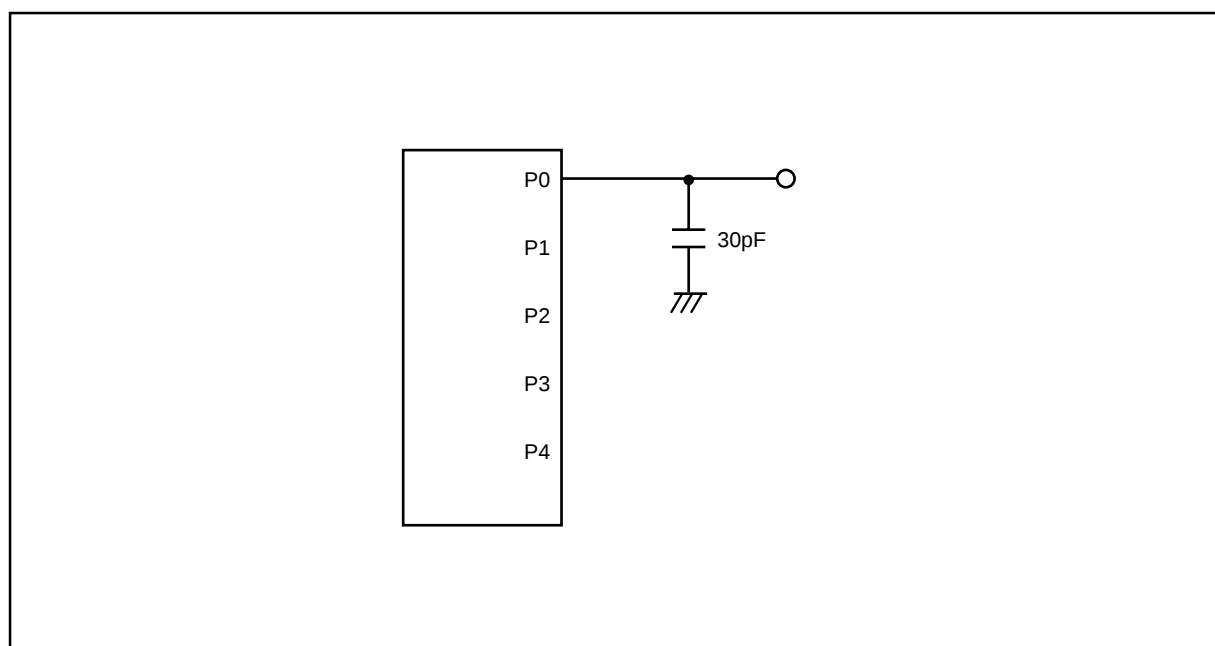
**Figure 5.1 Port P0 to P4 measurement circuit**

Table 5.4 Flash Memory (Program ROM) Electrical Characteristics

Symbol	Parameter	Measuring condition	Standard			Unit
			Min.	Typ.	Max	
—	Program/Erase endurance ⁽²⁾		1,000 ⁽³⁾	—	—	times
—	Byte program time		—	50	—	μs
—	Block erase time		—	0.4	—	s
t _d (SR-ES)	Time delay from Suspend Request until Erase Suspend		—	—	8	ms
—	Erase Suspend Request Interval		10	—	—	ms
—	Program, Erase Voltage		2.7	—	5.5	V
—	Read Voltage		2.7	—	5.5	V
—	Program, Erase Temperature		0	—	60	°C
—	Data hold time ⁽⁷⁾	Ambient temperature = 55 °C	20	—	—	year

NOTES:

1. V_{CC}=AV_{CC}=2.7 to 5.5V at T_{opr} = 0 to 60 °C, unless otherwise specified.

2. Definition of Program/Erase

The endurance of Program/Erase shows a time for each block.

If the program/erase number is "n" (n = 1,000, 10,000), "n" times erase can be performed for each block.

For example, if performing one-byte write to the distinct addresses on Block A of 2K-byte block 2048 times and then erasing that block, the number of Program/Erase cycles is one time.

However, performing multiple writes to the same address before an erase operation is prohibited (overwriting prohibited).

3. Numbers of Program/Erase cycles for which all electrical characteristics is guaranteed.

4. To reduce the number of Program/Erase cycles, a block erase should ideally be performed after writing in series as many distinct addresses (only one time each) as possible. If programming a set of 16 bytes, write up to 128 sets and then erase them one time. This will result in ideally reducing the number of Program/Erase cycles. Additionally, averaging the number of Program/Erase cycles for Block A and B will be more effective. It is important to track the total number of block erases and restrict the number.

5. If error occurs during block erase, attempt to execute the clear status register command, then the block erase command at least three times until the erase error disappears.

6. Customers desiring Program/Erase failure rate information should contact their Renesas technical support representative.

7. The data hold time includes time that the power supply is off or the clock is not supplied.

Table 5.7 Electrical Characteristics (1) [Vcc=5V]

Symbol	Parameter		Measuring condition		Standard			Unit
					Min.	Typ.	Max.	
V _{OH}	"H" output voltage	Except X _{OUT}	I _{OH} =-5mA		V _{CC} -2.0	—	V _{CC}	V
			I _{OH} =-200μA		V _{CC} -0.3	—	V _{CC}	V
	X _{OUT}		Drive capacity HIGH I _{OH} =-1 mA		V _{CC} -2.0	—	V _{CC}	V
			Drive capacity LOW I _{OH} =-500μA		V _{CC} -2.0	—	V _{CC}	V
V _{OL}	"L" output voltage	Except P10 to P17, X _{OUT}	I _{OL} = 5 mA		—	—	2.0	V
			I _{OL} = 200 μA		—	—	0.45	V
	P10 to P17		Drive capacity HIGH I _{OL} = 15 mA		—	—	2.0	V
			Drive capacity LOW I _{OL} = 5 mA		—	—	2.0	V
			Drive capacity LOW I _{OL} = 200 μA		—	—	0.45	V
	X _{OUT}		Drive capacity HIGH I _{OL} = 1 mA		—	—	2.0	V
			Drive capacity LOW I _{OL} =500 μA		—	—	2.0	V
V _{TH} -V _T	Hysteresis	INT0, INT1, INT2, INT3, K10, K11, K12, K13, CNTR0, CNTR1, TCIN, RxD0, RxD1, P45			0.2	—	1.0	V
		RESET			0.2	—	2.2	V
I _{IH}	"H" input current		V _I =5V		—	—	5.0	μA
I _{IL}	"L" input current		V _I =0V		—	—	-5.0	μA
R _{PULLUP}	Pull-up resistance		V _I =0V		30	50	167	kΩ
R _{XIN}	Feedback resistance	X _{IN}			—	1.0	—	MΩ
f _{RING-S}	Low-speed on-chip oscillator frequency				40	125	250	kHz
V _{RAM}	RAM retention voltage		At stop mode		2.0	—	—	V

NOTES:

1. Referenced to V_{CC} = AV_{CC} = 4.2 to 5.5V at T_{opr} = -20 to 85 °C / -40 to 85 °C, f(X_{IN})=20MHz unless otherwise specified.

Table 5.8 Electrical Characteristics (2) [Vcc=5V]

Symbol	Parameter		Measuring condition		Standard			Unit
					Min.	Typ.	Max.	
I _{CC}	Power supply current (V _{CC} =3.3 to 5.5V) In single-chip mode, the output pins are open and other pins are V _{SS}		High-speed mode	X _{IN} =16 MHz (square wave) On-chip oscillator on=125 kHz No division	—	8	14	mA
				X _{IN} =10 MHz (square wave) On-chip oscillator on=125 kHz No division	—	5	—	mA
			Medium-speed mode	X _{IN} =16 MHz (square wave) On-chip oscillator on=125 kHz Division by 8	—	3	—	mA
				X _{IN} =10 MHz (square wave) On-chip oscillator on=125 kHz Division by 8	—	2	—	mA
			On-chip oscillator mode	Main clock off On-chip oscillator on=125 kHz Division by 8	—	470	900	μA
			Wait mode	Main clock off On-chip oscillator on=125 kHz When a WAIT instruction is executed ⁽¹⁾ Peripheral clock operation	—	40	80	μA
			Wait mode	Main clock off On-chip oscillator on=125 kHz When a WAIT instruction is executed ⁽¹⁾ Peripheral clock off	—	38	76	μA
			Stop mode	Main clock off, T _{opr} = 25 °C On-chip oscillator off CM10="1" Peripheral clock off	—	0.8	3.0	μA

NOTES:

1. Timer Y is operated with timer mode.
2. Referenced to V_{CC} = AV_{CC} = 4.2 to 5.5V at T_{opr} = -20 to 85 °C / -40 to 85 °C, f(X_{IN})=20MHz unless otherwise specified.

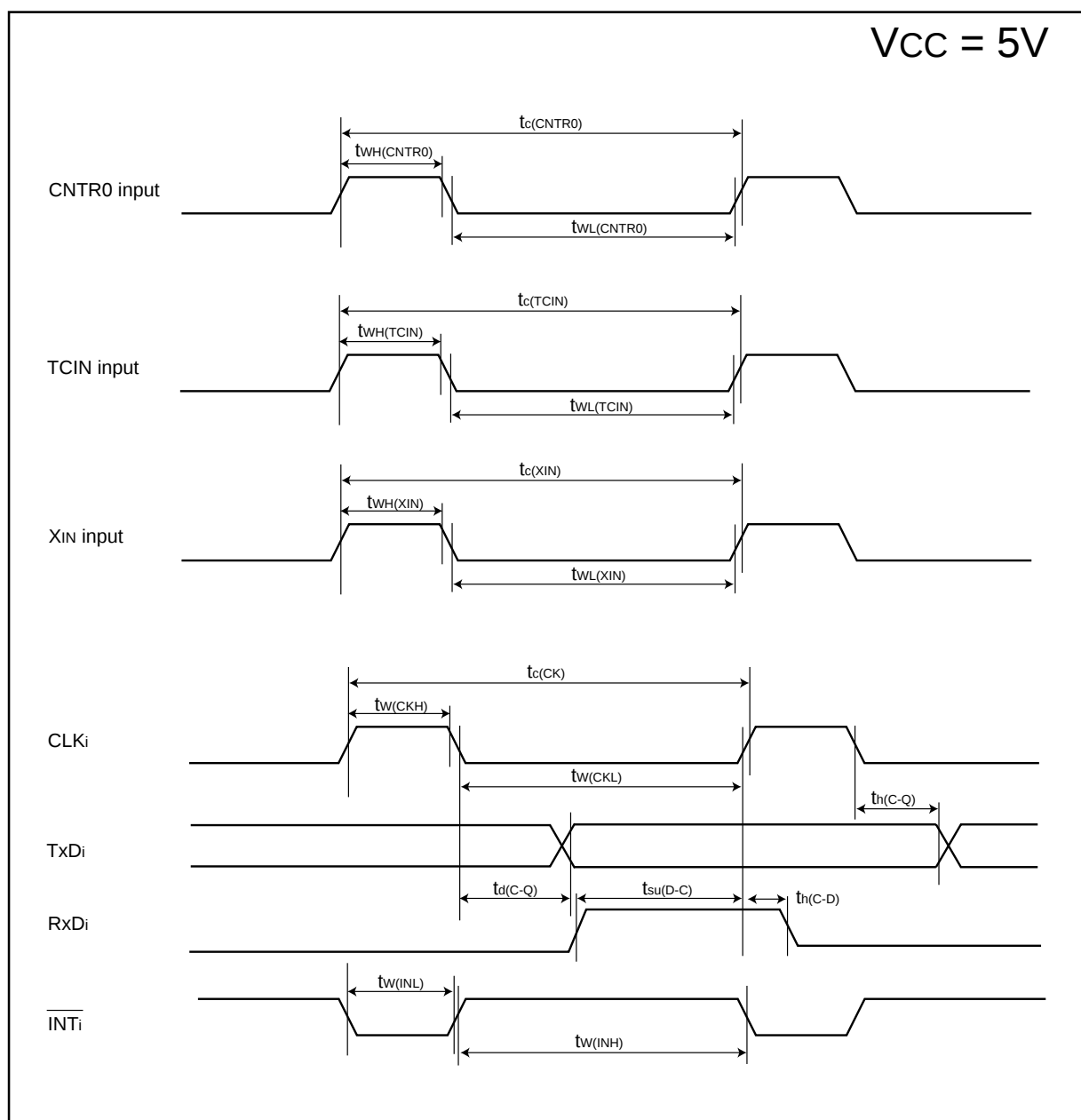
Figure 5.3 $V_{CC}=5V$ timing diagram

Table 5.14 Electrical Characteristics (3) [Vcc=3V]

Symbol	Parameter		Measuring condition		Standard			Unit
					Min.	Typ.	Max.	
VOH	"H" output voltage	Except XOUT	IOH=-1mA		Vcc-0.5	—	Vcc	V
		XOUT	Drive capacity HIGH	IOH=-0.1 mA	Vcc-0.5	—	Vcc	V
			Drive capacity LOW	IOH=-50 μA	Vcc-0.5	—	Vcc	V
VOL	"L" output voltage	Except P10 to P17, XOUT	IOL= 1 mA		—	—	0.5	V
		P10 to P17	Drive capacity HIGH	IOL= 2 mA	—	—	0.5	V
			Drive capacity LOW	IOL= 1 mA	—	—	0.5	V
		XOUT	Drive capacity HIGH	IOL= 0.1 mA	—	—	0.5	V
			Drive capacity LOW	IOL=50 μA	—	—	0.5	V
VT+-VT-	Hysteresis	INT0, INT1, INT2, INT3, KI0, KI1, KI2, KI3, CNTR0, CNTR1, TCIN, RxD0, RxD1, P45			0.2	—	0.8	V
		RESET			0.2	—	1.8	V
IiH	"H" input current		Vi=3V		—	—	4.0	μA
IiL	"L" input current		Vi=0V		—	—	-4.0	μA
RPULLUP	Pull-up resistance		Vi=0V		66	160	500	kΩ
RfXIN	Feedback resistance	XIN			—	3.0	—	MΩ
fRING	On-chip oscillator frequency				40	125	250	kHz
V _{RAM}	RAM retention voltage		At stop mode		2.0	—	—	V

NOTES:

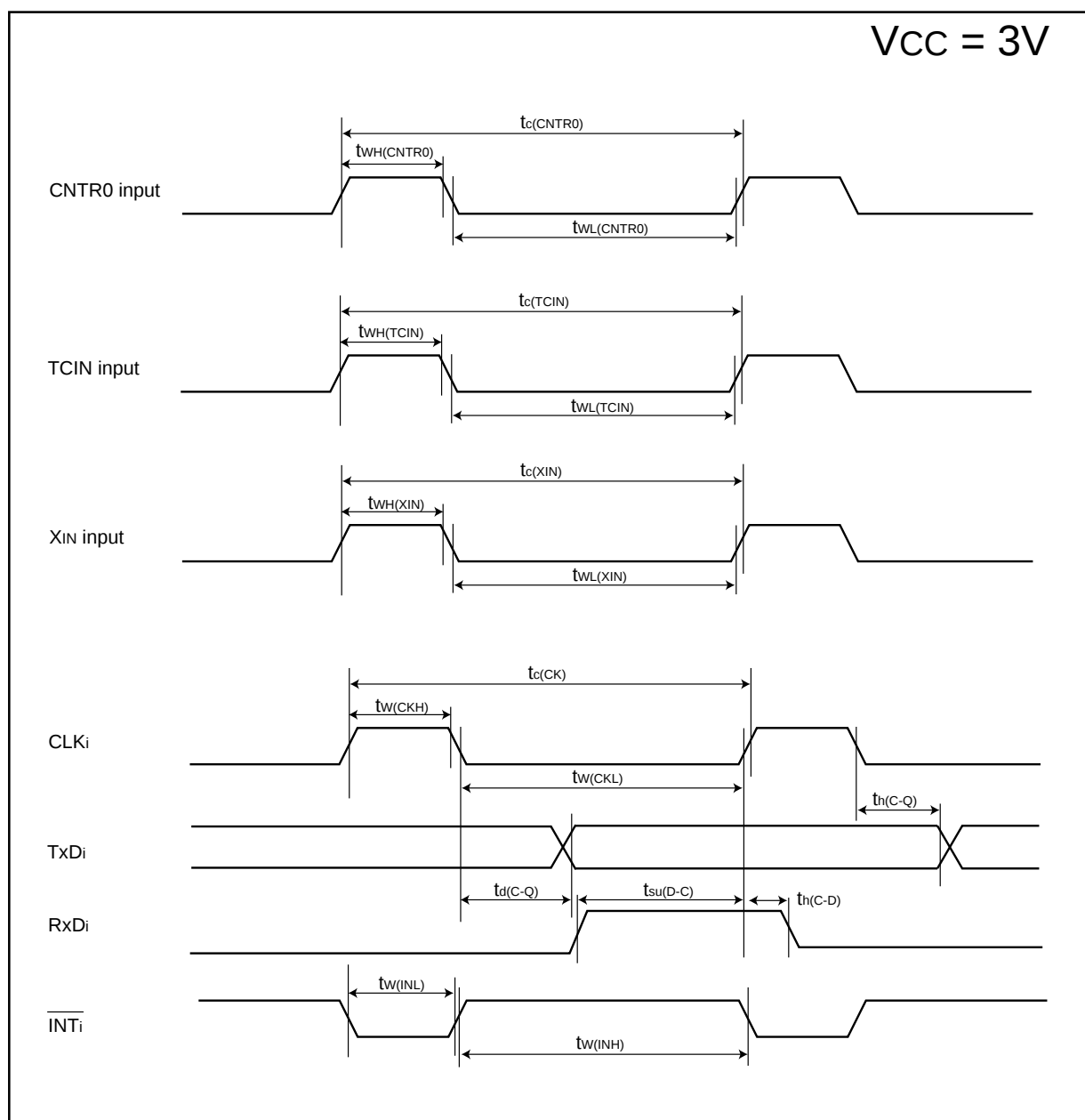
1. Referenced to Vcc=AVcc=2.7 to 3.3V at T_{opr} = -20 to 85 °C / -40 to 85 °C, f(XIN)=10MHz unless otherwise specified.

Table 5.15 Electrical Characteristics (4) [Vcc=3V]

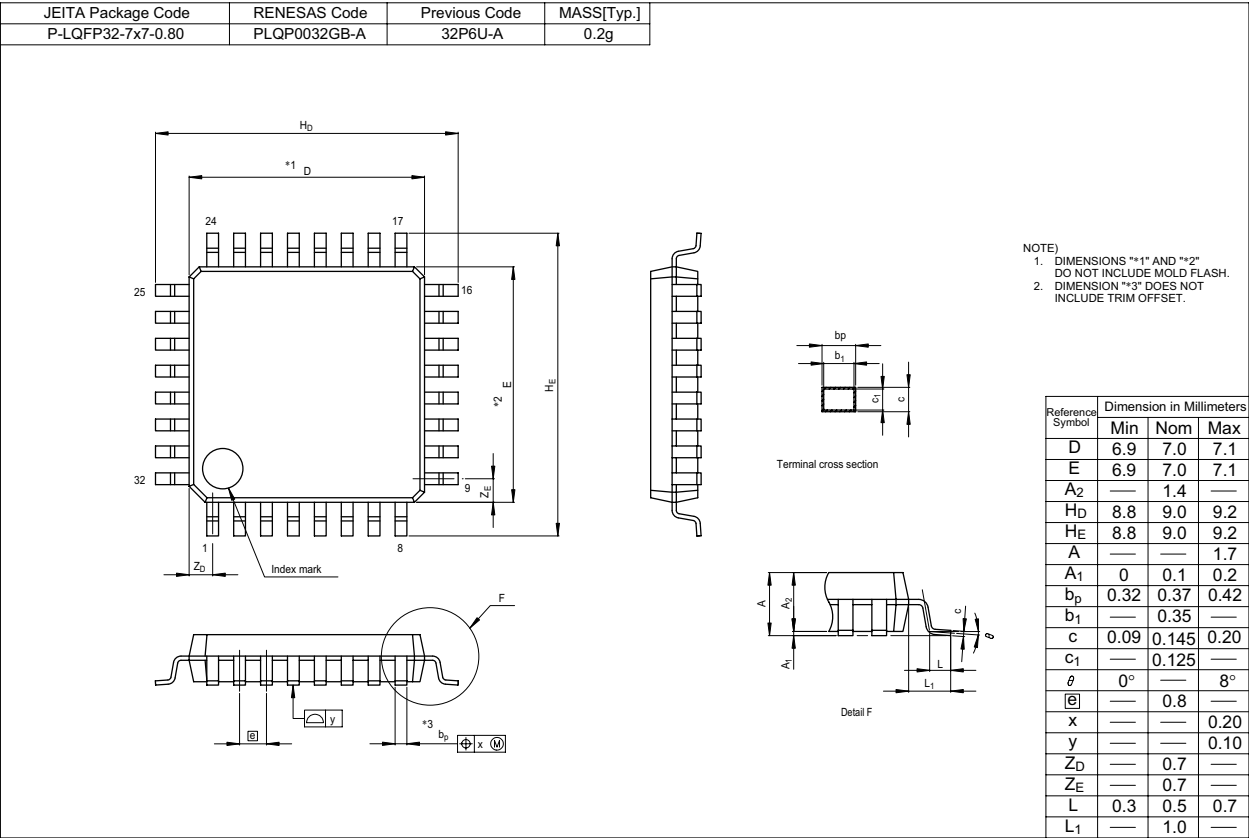
Symbol	Parameter	Measuring condition	Standard			Unit
			Min.	Typ.	Max.	
I _{cc}	Power supply current (V _{CC1} =2.7 to 3.3V) In single-chip mode, the output pins are open and other pins are V _{SS}	High-speed mode X _{IN} =16 MHz (square wave) On-chip oscillator on=125 kHz No division	—	7	12	mA
		X _{IN} =10 MHz (square wave) On-chip oscillator on=125 kHz No division	—	5	—	mA
		Medium-speed mode X _{IN} =16 MHz (square wave) On-chip oscillator on=125 kHz Division by 8	—	2.5	—	mA
		X _{IN} =10 MHz (square wave) On-chip oscillator on=125 kHz Division by 8	—	1.6	—	mA
		On-chip oscillator mode Main clock off On-chip oscillator on=125 kHz Division by 8	—	420	800	μA
		Wait mode Main clock off On-chip oscillator on=125 kHz When a WAIT instruction is executed ⁽¹⁾ Peripheral clock operation	—	37	74	μA
		Wait mode Main clock off On-chip oscillator on=125 kHz When a WAIT instruction is executed ⁽¹⁾ Peripheral clock off	—	35	70	μA
		Stop mode Main clock off, T _{opr} = 25 °C On-chip oscillator off CM10="1" Peripheral clock off	—	0.7	3.0	μA

NOTES:

1. Timer Y is operated with timer mode.
2. Referenced to V_{CC}=AV_{CC}=2.7 to 3.3V at T_{opr} = -20 to 85 °C / -40 to 85 °C, f(X_{IN})=10MHz unless otherwise specified.

Figure 5.4 V_{CC}=3V timing diagram

Package Dimensions



REVISION HISTORY	R8C/12 Group Datasheet
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Rev.	Date	Description	
		Page	Summary
0.10	Oct 28, 2003		First edition issued
0.20	Dec05, 2003	16	Table 16.5 revised
1.00	Sep30, 2004	All pages	Words standardized (on-chip oscillator, serial interface, A/D)
		2	Table 1.1 revised
		5	Figure 1.3, NOTES 3 added
		6	Table 1.3 revised
		9	Figure 3.1, NOTES added
		10-13	One body sentence in chapter 4 added ; Titles of Table 4.1 to 4.4 added
		12	Table 4.3 revised ; Table 4.4 revised
		14	Table 5.2 revised
		15	Table 5.3 revised
		16	Table 5.4 and 5.5 revised
		17	Table 5.7 revised
		18	Table 5.8 revised
		19	Table 5.13 revised
		21	Table 5.14 revised
		22	Table 5.15 revised
		23	Table 5.17 revised
1.10	Apr.27.2005	4	Table 1.2, Figure 1.2 package name revised
		5	Figure 1.3 package name revised
		10	Table 4.1 revised
		12	Table 4.3 revised
		15	Table 5.3 partly revised
		16	Table 5.4, Table 5.5 partly added
		17	Table 5.6, Table 5.7 partly revised
		21	Table 5.14 partly revised
		26	Package Dimensions revised
1.20	Jan.27.2006	2	Table 1.1 Performance outline revised
		3	Figure 1.1 Block diagram partly revised
		4	1.4 Product Information, title of Table 1.2
			“Product List” → “Product Informaton” revised
			ROM capacity; “Program area” → “Program ROM”,
			“Data area” → “Data flash” revised
			Figure 1.2 Type No., Memory Size, and Package partly revised
		6	Table 1.3 Pin description revised
		7-8	2 Central Processing Unit (CPU) revised
			Figure 2.1 CPU register revised
		9	3 Memory, Figure 3.1 Memory Map;
			“Program area” → “Program ROM”, “Data area” → “Data flash” revised
		10	Table 4.1 SFR Information(1) NOTES:1 revised

REVISION HISTORY	R8C/12 Group Datasheet
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Rev.	Date	Description	
		Page	Summary
1.20	Jan.27.2006	11	Table 4.2 SFR Information(2) NOTES:1 revised
		12	Table 4.3 SFR Information(3); 0081 ₁₆ : "Prescaler Y" → "Prescaler Y Register" 0082 ₁₆ : "Timer Y Secondary" → "Timer Y Secondary Register" 0083 ₁₆ : "Timer Y Primary" → "Timer Y Primary Register" 0085 ₁₆ : "Prescaler Z" → "Prescaler Z Register" 0086 ₁₆ : "Timer Z Secondary" → "Timer Z Secondary Register" 0087 ₁₆ : "Timer Z Primary" → "Timer Z Primary Register" 008C ₁₆ : "Prescaler X" → "Prescaler X Register" revised NOTES:1 revised
		13	Table 4.4 SFR Information(4) NOTES:1 revised
		14	Table 5.2 Recommended Operating Conditions; NOTES: 1, 2, 3 revised
		15	Table 5.3 A/D Conversion Characteristics; "A/D operation clock frequency" → "A/D operating clock frequency" revised NOTES: 1, 2, 3, 4 revised
		16	Table 5.4 Flash Memory (Program ROM) Electrical Characteristics; "Data retention duration" → "Data hold time" revised "Topr" → "Ambient temperature" NOTES: 1 to 7 added Measuring condition of byte program time and block erase time deleted
		17	Table 5.5 Flash Memory (Data flash Block A, Block B) Electrical characteristics "Data retention duration" → "Data hold time" revised "Topr" → "Ambient temperature" NOTES: 1, 3 revised, NOTES: 9 added Measuring condition of byte program time and block erase time deleted
		18	Table 5.7 Electrical Characteristics (1) [V _{CC} =5V]; "P1 ₀ to P1 ₇ Except X _{OUT} " → "Except P1 ₀ to P1 ₇ , X _{OUT} " revised Table 5.8 Electrical Characteristics (2) [V _{CC} =5V]; Measuring condition Stop mode: "Topr = 25 °C" added NOTES: 1, 2 revised
		21	Table 5.14 Electrical Characteristics (3) [V _{CC} =3V] "P1 ₀ to P1 ₇ Except X _{OUT} " → "Except P1 ₀ to P1 ₇ , X _{OUT} " revised
		22	Table 5.15 Electrical Characteristics (4) [V _{CC} =3V]; Measuring condition Stop mode: "Topr = 25 °C" added NOTES: 1, 2 revised

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