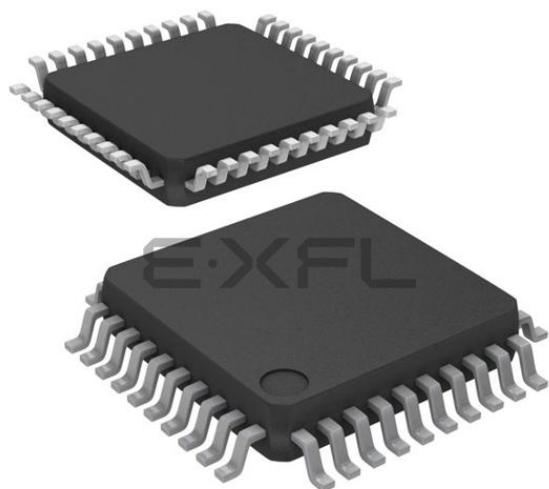




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Details

Product Status	Not For New Designs
Core Processor	R8C
Core Size	16-Bit
Speed	16MHz
Connectivity	SIO, UART/USART
Peripherals	LED, WDT
Number of I/O	22
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-20°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	32-LQFP
Supplier Device Package	32-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f21124fp-u0

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1. Overview

This MCU is built using the high-performance silicon gate CMOS process using a R8C Tiny Series CPU core and is packaged in a 32-pin plastic molded LQFP. This MCU operates using sophisticated instructions featuring a high level of instruction efficiency. With 1M bytes of address space, it is capable of executing instructions at high speed.

The data flash ROM (2 KB X 2 blocks) is embedded.

1.1 Applications

Electric household appliance, office equipment, housing equipment (sensor, security), general industrial equipment, audio, etc.

1.2 Performance Overview

Table 1.1. lists the performance outline of this MCU.

Table 1.1 Performance outline

Item		Performance
CPU	Number of basic instructions	89 instructions
	Minimum instruction execution time	62.5 ns (f(XIN) = 16 MHz, VCC = 3.0 to 5.5 V) 100 ns (f(XIN) = 10 MHz, VCC = 2.7 to 5.5 V)
	Operating mode	Single-chip
	Address space	1M bytes
	Memory capacity	See Table 1.2 “Product List”
Peripheral function	Port	Input/Output: 22 (including LED drive port), Input: 2
	LED drive port	I/O port: 8
	Timer	Timer X: 8 bits x 1 channel, Timer Y: 8 bits x 1 channel, Timer Z: 8 bits x 1 channel (Each timer equipped with 8-bit prescaler) Timer C: 16 bits x 1 channel (Input capture circuit)
	Serial Interface	•1 channel Clock synchronous, UART •1 channel UART
	A/D converter	10-bit A/D converter: 1 circuit, 8 channels
	Watchdog timer	15 bits x 1 (with prescaler) Reset start function selectable
	Interrupt	Internal: 9 factors, External: 5 factors, Software: 4 factors, Priority level: 7 levels
	Clock generation circuit	2 circuits •Main clock generation circuit (Equipped with a built-in feedback resistor) •On-chip oscillator
	Oscillation stop detection function	Main clock oscillation stop detection function
Electrical characteristics	Supply voltage	VCC = 3.0 to 5.5 V (f(XIN) = 16 MHz) VCC = 2.7 to 5.5 V (f(XIN) = 10 MHz)
	Power consumption	Typ.8mA (VCC = 5.0 V (f(XIN) = 16 MHz) Typ.5mA (VCC = 3.0 V, (f(XIN) = 10 MHz) Typ.35μA (VCC = 3.0 V, Wait mode, peripheral clock stops) Typ.0.7μA (VCC = 3.0 V, Stop mode)
Flash memory	Program/erase supply voltage	VCC = 2.7 to 5.5 V
	Program/erase endurance	10,000 times (Data flash) 1,000 times (Program ROM)
		Operating ambient temperature
		-20 to 85 °C -40 to 85 °C (D-version)
Package		32-pin plastic mold LQFP

1.3 Block Diagram

Figure 1.1. shows this MCU block diagram.

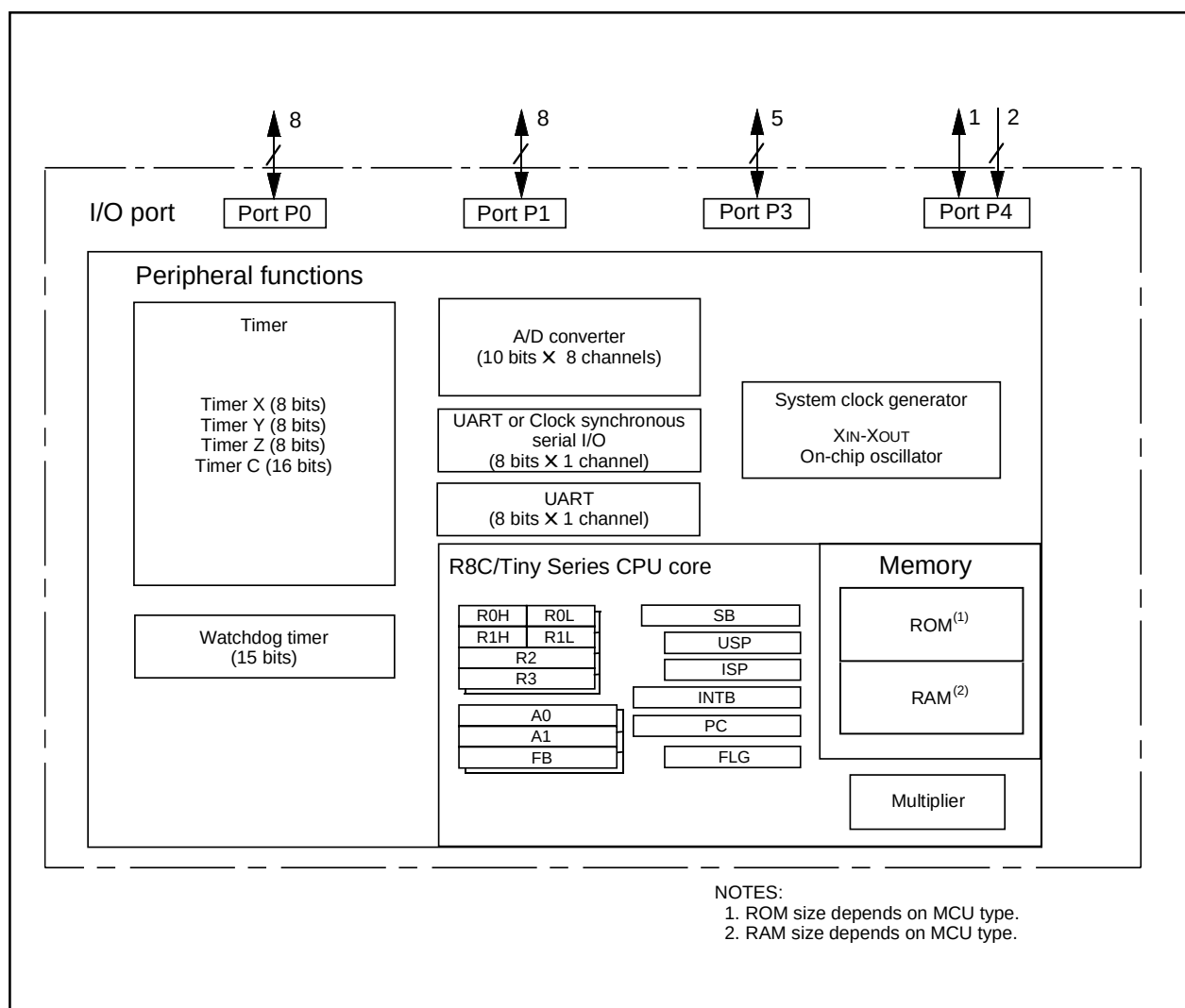


Figure 1.1 Block Diagram

1.6 Pin Description

Table 1.3 shows the pin description

Table 1.3 Pin description

Signal name	Pin name	I/O type	Function
Power supply input	Vcc, Vss	I	Apply 2.7 V to 5.5 V to the Vcc pin. Apply 0 V to the Vss pin.
IVcc	IVcc	O	This pin is to stabilize internal power supply. Connect this pin to Vss via a capacitor (0.1 μ F). Do not connect to Vcc.
Analog power supply input	AVcc, AVss	I	Power supply input pins for A/D converter. Connect the AVcc pin to Vcc. Connect the AVss pin to Vss. Connect a capacitor between pins AVcc and AVss.
Reset input	$\overline{\text{RESET}}$	I	Input "L" on this pin resets the MCU.
CNVss	CNVss	I	Connect this pin to Vss via a resistor.
MODE	MODE	I	Connect this pin to Vcc via a resistor.
Main clock input	XIN	I	These pins are provided for the main clock generating circuit I/O. Connect a ceramic resonator or a crystal oscillator between the XIN and XOUT pins. To use an externally derived clock, input it to the XIN pin and leave the XOUT pin open.
Main clock output	XOUT	O	
INT interrupt input	INT0 to INT3	I	INT interrupt input pins.
Key input interrupt	KI0 to KI3	I	Key input interrupt pins.
Timer X	CNTR0	I/O	Timer X I/O pin
	CNTR0	O	Timer X output pin
Timer Y	CNTR1	I/O	Timer Y I/O pin
Timer Z	TZOUT	O	Timer Z output pin
Timer C	TCIN	I	Timer C input pin
Serial interface	CLK0	I/O	Transfer clock I/O pin.
	RxD0, RxD1	I	Serial data input pins.
	TxD0, TxD10, TxD11	O	Serial data output pins.
Reference voltage input	VREF	I	Reference voltage input pin for A/sD converter. Connect the VREF pin to Vcc.
A/D converter	AN0 to AN7	I	Analog input pins for A/D converter
I/O port	P00 to P07, P10 to P17, P30 to P33, P37, P45	I/O	These are 8-bit CMOS I/O ports. Each port has an input/output select direction register, allowing each pin in that port to be directed for input or output individually. Any port set to input can select whether to use a pull-up resistor or not by program. P10 to P17 also function as LED drive ports.
Input port	P46, P47	I	Port for input-only.

2. Central Processing Unit (CPU)

Figure 2.1 shows the CPU registers. The CPU has 13 registers. Of these, R0, R1, R2, R3, A0, A1 and FB comprise a register bank. Two sets of register banks are provided.

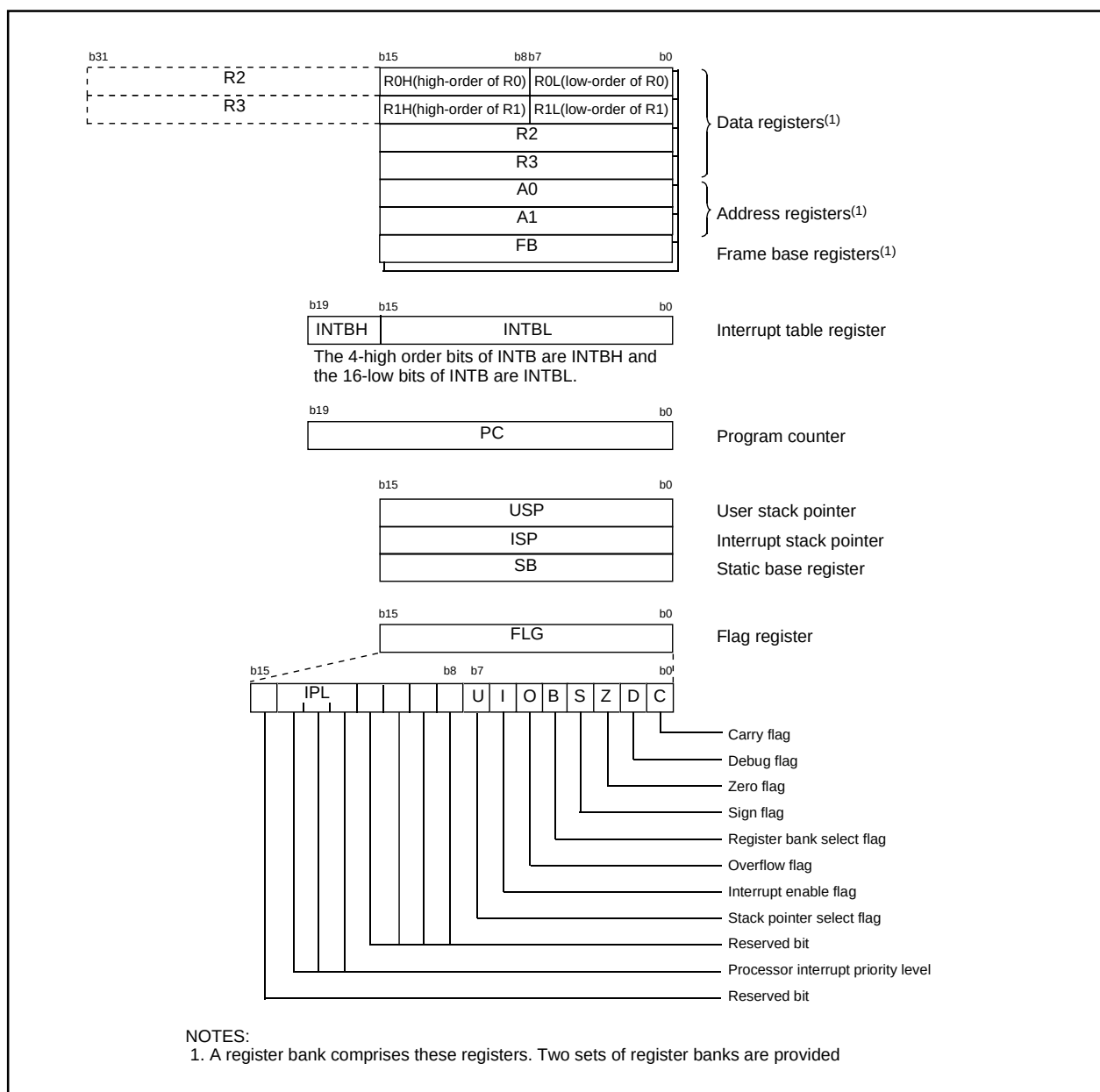


Figure 2.1 CPU Register

2.1 Data Registers (R0, R1, R2 and R3)

R0 is a 16-bit register for transfer, arithmetic and logic operations. The same applies to R1 to R3. The R0 can be split into high-order bit (R0H) and low-order bit (R0L) to be used separately as 8-bit data registers. The same applies to R1H and R1L as R0H and R0L. R2 can be combined with R0 to be used as a 32-bit data register (R2R0). The same applies to R3R1 as R2R0.

3. Memory

Figure 3.1 is a memory map of this MCU. This MCU provides 1-Mbyte address space from addresses 00000₁₆ to FFFFF₁₆.

The internal ROM (program ROM) is allocated lower addresses beginning with address 0FFFF₁₆. For example, a 16-Kbyte internal ROM is allocated addresses from 0C000₁₆ to 0FFFF₁₆.

The fixed interrupt vector table is allocated addresses 0FFDC₁₆ to 0FFFF₁₆. They store the starting address of each interrupt routine.

The internal ROM (data flash) is allocated addresses from 02000₁₆ to 02FFF₁₆.

The internal RAM is allocated higher addresses beginning with address 00400₁₆. For example, a 1-Kbyte internal RAM is allocated addresses 00400₁₆ to 007FF₁₆. The internal RAM is used not only for storing data, but for calling subroutines and stacks when interrupt request is acknowledged.

Special function registers (SFR) are allocated addresses 00000₁₆ to 002FF₁₆. The peripheral function control registers are located there. All addresses, which have nothing allocated within the SFR, are reserved area and cannot be accessed by users.

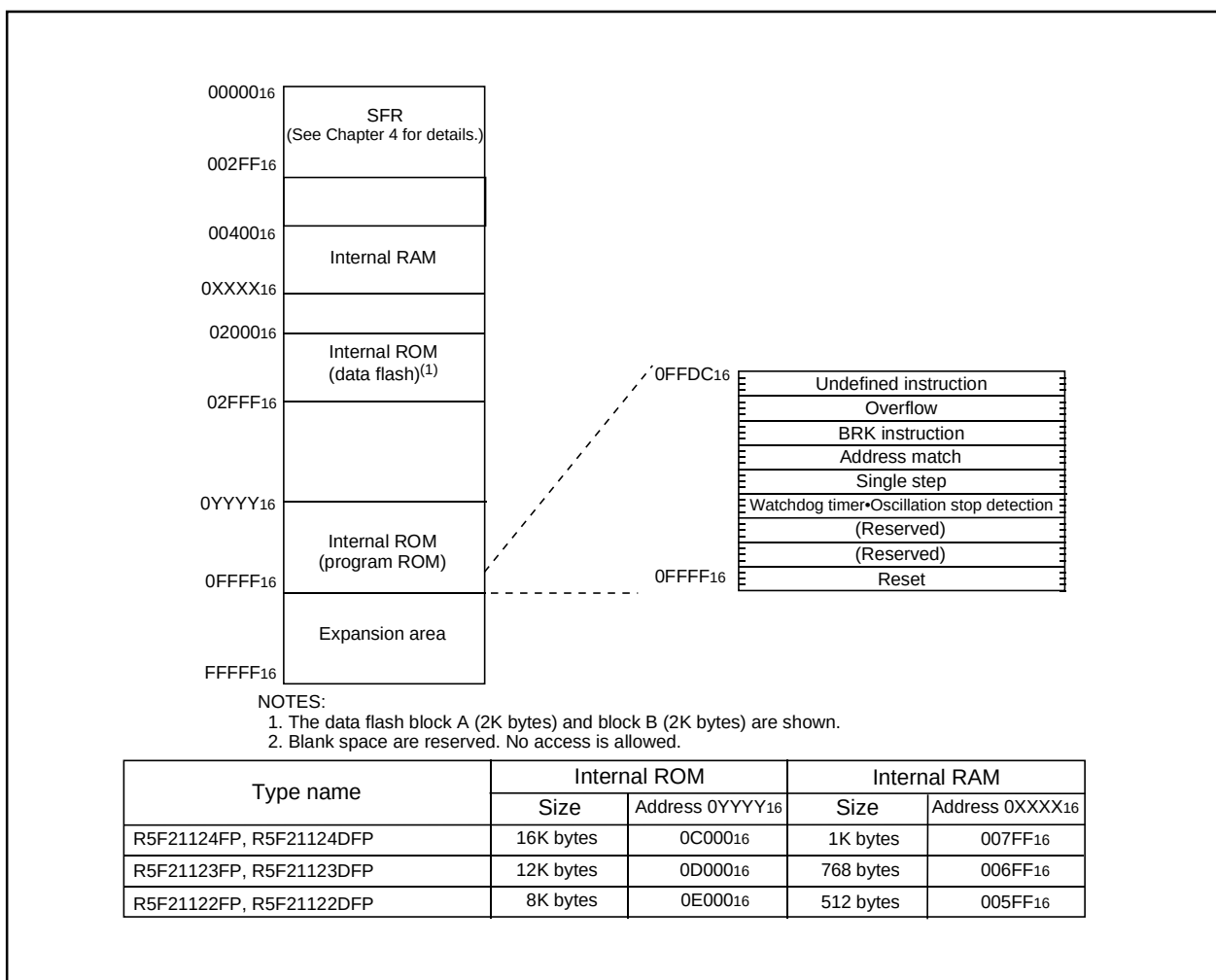


Figure 3.1 Memory Map

4. Special Function Register (SFR)

SFR(Special Function Register) is the control register of peripheral functions. Tables 4.1 to 4.4 list the SFR information

Table 4.1 SFR Information(1)(1)

Address	Register	Symbol	After reset
0000 ₁₆			
0001 ₁₆			
0002 ₁₆			
0003 ₁₆			
0004 ₁₆	Processor mode register 0	PM0	XXXX0X002
0005 ₁₆	Processor mode register 1	PM1	00XXX0X02
0006 ₁₆	System clock control register 0	CM0	011010002
0007 ₁₆	System clock control register 1	CM1	001000002
0008 ₁₆			
0009 ₁₆	Address match interrupt enable register	AIER	XXXXXX002
000A ₁₆	Protect register	PRCR	00XXX0002
000B ₁₆			
000C ₁₆	Oscillation stop detection register	OCD	000001002
000D ₁₆	Watchdog timer reset register	WDTR	XX16
000E ₁₆	Watchdog timer start register	WDTS	XX16
000F ₁₆	Watchdog timer control register	WDC	000111112
0010 ₁₆	Address match interrupt register 0	RMAD0	0016
0011 ₁₆			0016
0012 ₁₆			X016
0013 ₁₆			
0014 ₁₆	Address match interrupt register 1	RMAD1	0016
0015 ₁₆			0016
0016 ₁₆			X016
0017 ₁₆			
0018 ₁₆			
0019 ₁₆			
001A ₁₆			
001B ₁₆			
001C ₁₆			
001D ₁₆			
001E ₁₆	INT0 input filter select register	INT0F	XXXXX0002
001F ₁₆			
0020 ₁₆			
0021 ₁₆			
0022 ₁₆			
0023 ₁₆			
0024 ₁₆			
0025 ₁₆			
0026 ₁₆			
0027 ₁₆			
0028 ₁₆			
0029 ₁₆			
002A ₁₆			
002B ₁₆			
002C ₁₆			
002D ₁₆			
002E ₁₆			
002F ₁₆			
0030 ₁₆			
0031 ₁₆			
0032 ₁₆			
0033 ₁₆			
0034 ₁₆			
0035 ₁₆			
0036 ₁₆			
0037 ₁₆			
0038 ₁₆			
0039 ₁₆			
003A ₁₆			
003B ₁₆			
003C ₁₆			
003D ₁₆			
003E ₁₆			
003F ₁₆			

NOTES :

1. Blank spaces are reserved. No access is allowed.

X : Undefined

Table 4.3 SFR Information(3)(1)

Address	Register	Symbol	After reset
0080 ₁₆	Timer Y, Z mode register	TYZMR	0016
0081 ₁₆	Prescaler Y register	PREY	FF16
0082 ₁₆	Timer Y secondary register	TYSC	FF16
0083 ₁₆	Timer Y primary register	TYPR	FF16
0084 ₁₆	Timer Y, Z waveform output control register	PUM	0016
0085 ₁₆	Prescaler Z register	PREZ	FF16
0086 ₁₆	Timer Z secondary register	TZSC	FF16
0087 ₁₆	Timer Z primary register	TZPR	FF16
0088 ₁₆			
0089 ₁₆			
008A ₁₆	Timer Y, Z output control register	TYZOC	0016
008B ₁₆	Timer X mode register	TXMR	0016
008C ₁₆	Prescaler X register	PREX	FF16
008D ₁₆	Timer X register	TX	FF16
008E ₁₆	Timer count source setting register	TCSS	0016
008F ₁₆			
0090 ₁₆	Timer C register	TC	0016
0091 ₁₆			0016
0092 ₁₆			
0093 ₁₆			
0094 ₁₆			
0095 ₁₆			
0096 ₁₆	External input enable register	INTEN	0016
0097 ₁₆			
0098 ₁₆	Key input enable register	KIEN	0016
0099 ₁₆			
009A ₁₆	Timer C control register 0	TCC0	0016
009B ₁₆	Timer C control register 1	TCC1	0016
009C ₁₆	Capture register	TM0	0016
009D ₁₆			0016
009E ₁₆			
009F ₁₆			
00A0 ₁₆	UART0 transmit/receive mode register	U0MR	0016
00A1 ₁₆	UART0 bit rate register	U0BRG	XX16
00A2 ₁₆	UART0 transmit buffer register	U0TB	XX16
00A3 ₁₆			XX16
00A4 ₁₆	UART0 transmit/receive control register 0	U0C0	000010002
00A5 ₁₆	UART0 transmit/receive control register 1	U0C1	000000102
00A6 ₁₆	UART0 receive buffer register	U0RB	XX16
00A7 ₁₆			XX16
00A8 ₁₆	UART1 transmit/receive mode register	U1MR	0016
00A9 ₁₆	UART1 bit rate generator	U1BRG	XX16
00AA ₁₆	UART1 transmit buffer register	U1TB	XX16
00AB ₁₆			XX16
00AC ₁₆	UART1 transmit/receive control register 0	U1C0	000010002
00AD ₁₆	UART1 transmit/receive control register 1	U1C1	000000102
00AE ₁₆	UART1 receive buffer register	U1RB	XX16
00AF ₁₆			XX16
00B0 ₁₆	UART transmit/receive control register 2	UCON	0016
00B1 ₁₆			
00B2 ₁₆			
00B3 ₁₆			
00B4 ₁₆			
00B5 ₁₆			
00B6 ₁₆			
00B7 ₁₆			
00B8 ₁₆			
00B9 ₁₆			
00BA ₁₆			
00BB ₁₆			
00BC ₁₆			
00BD ₁₆			
00BE ₁₆			
00BF ₁₆			

NOTES :

1. Blank spaces are reserved. No access is allowed.

X : Undefined

Table 4.4 SFR Information(4)(1)

Address	Register	Symbol	After reset
00C0 ₁₆	AD register	AD	XXXXXXXX ₂
00C1 ₁₆			XXXXXXXX ₂
00C2 ₁₆			
00C3 ₁₆			
00C4 ₁₆			
00C5 ₁₆			
00C6 ₁₆			
00C7 ₁₆			
00C8 ₁₆			
00C9 ₁₆			
00CA ₁₆			
00CB ₁₆			
00CC ₁₆			
00CD ₁₆			
00CE ₁₆			
00CF ₁₆			
00D0 ₁₆			
00D1 ₁₆			
00D2 ₁₆			
00D3 ₁₆			
00D4 ₁₆	AD control register 2	ADCON2	00 ₁₆
00D5 ₁₆			
00D6 ₁₆	AD control register 0	ADCON0	00000XXX ₂
00D7 ₁₆	AD control register 1	ADCON1	00 ₁₆
00D8 ₁₆			
00D9 ₁₆			
00DA ₁₆			
00DB ₁₆			
00DC ₁₆			
00DD ₁₆			
00DE ₁₆			
00DF ₁₆			
00E0 ₁₆	Port P0 register	P0	XX ₁₆
00E1 ₁₆	Port P1 register	P1	XX ₁₆
00E2 ₁₆	Port P0 direction register	PD0	00 ₁₆
00E3 ₁₆	Port P1 direction register	PD1	00 ₁₆
00E4 ₁₆			
00E5 ₁₆	Port P3 register	P3	XX ₁₆
00E6 ₁₆			
00E7 ₁₆	Port P3 direction register	PD3	00 ₁₆
00E8 ₁₆	Port P4 register	P4	XX ₁₆
00E9 ₁₆			
00EA ₁₆	Port P4 direction register	PD4	00 ₁₆
00EB ₁₆			
00EC ₁₆			
00ED ₁₆			
00EE ₁₆			
00EF ₁₆			
00F0 ₁₆			
00F1 ₁₆			
00F2 ₁₆			
00F3 ₁₆			
00F4 ₁₆			
00F5 ₁₆			
00F6 ₁₆			
00F7 ₁₆			
00F8 ₁₆			
00F9 ₁₆			
03FA ₁₆			
00FB ₁₆			
00FC ₁₆	Pull-up control register 0	PUR0	00XX0000 ₂
00FD ₁₆	Pull-up control register 1	PUR1	XXXXXXXX ₂
00FE ₁₆	Port P1 drive capacity control register	DRR	00 ₁₆
00FF ₁₆			
01B3 ₁₆	Flash memory control register 4	FMR4	01000000 ₂
01B4 ₁₆			
01B5 ₁₆	Flash memory control register 1	FMR1	1000000X ₂
01B6 ₁₆			
01B7 ₁₆	Flash memory control register 0	FMR0	00000001 ₂
0FFF ₁₆	Option function select register ⁽²⁾	OFS	(Note 2)

NOTES :

1. Blank columns, 0100₁₆ to 01B2₁₆ and 01B8₁₆ to 02FF₁₆ are all reserved. No access is allowed.

2. The watchdog timer control bit is assigned. Refer to "Figure11.2 OFS, WDC, WDTR and WDTS registers" for the OFS register details

X : Undefined

Table 5.3 A/D Conversion Characteristics

Symbol	Parameter		Measuring condition	Standard			Unit
				Min.	Typ.	Max.	
—	Resolution		$V_{ref} = V_{CC}$	—	—	10	Bit
—	Absolute accuracy	10 bit mode	$\phi_{AD} = 10 \text{ MHz}$, $V_{ref} = V_{CC} = 5.0 \text{ V}$	—	—	± 3	LSB
		8 bit mode	$\phi_{AD} = 10 \text{ MHz}$, $V_{ref} = V_{CC} = 5.0 \text{ V}$	—	—	± 2	LSB
		10 bit mode	$\phi_{AD} = 10 \text{ MHz}$, $V_{ref} = V_{CC} = 3.3 \text{ V}^{(3)}$	—	—	± 5	LSB
		8 bit mode	$\phi_{AD} = 10 \text{ MHz}$, $V_{ref} = V_{CC} = 3.3 \text{ V}^{(3)}$	—	—	± 2	LSB
R_{LADDER}	Ladder resistance		$V_{REF} = V_{CC}$	10	—	40	$k\Omega$
t_{CONV}	Conversion time	10 bit mode	$\phi_{AD} = 10 \text{ MHz}$, $V_{ref} = V_{CC} = 5.0 \text{ V}$	3.3	—	—	μs
		8 bit mode	$\phi_{AD} = 10 \text{ MHz}$, $V_{ref} = V_{CC} = 5.0 \text{ V}$	2.8	—	—	μs
V_{REF}	Reference voltage			—	$V_{CC}^{(4)}$	—	V
V_{IA}	Analog input voltage			0	—	V_{ref}	V
—	A/D operating clock frequency ⁽²⁾	Without sample & hold		0.25	—	10	MHz
		With sample & hold		1.0	—	10	MHz

NOTES:

1. $V_{CC} = AV_{CC} = 2.7$ to 5.5 V at $T_{opr} = -20$ to 85°C / -40 to 85°C , unless otherwise specified.
2. If f_{AD} exceeds 10 MHz , divide the f_{AD} and hold A/D operating clock frequency (ϕ_{AD}) 10 MHz or below.
3. If the AV_{CC} is less than 4.2 V , divide the f_{AD} and hold A/D operating clock frequency (ϕ_{AD}) $f_{AD}/2$ or below.
4. Hold $V_{CC} = V_{ref}$.

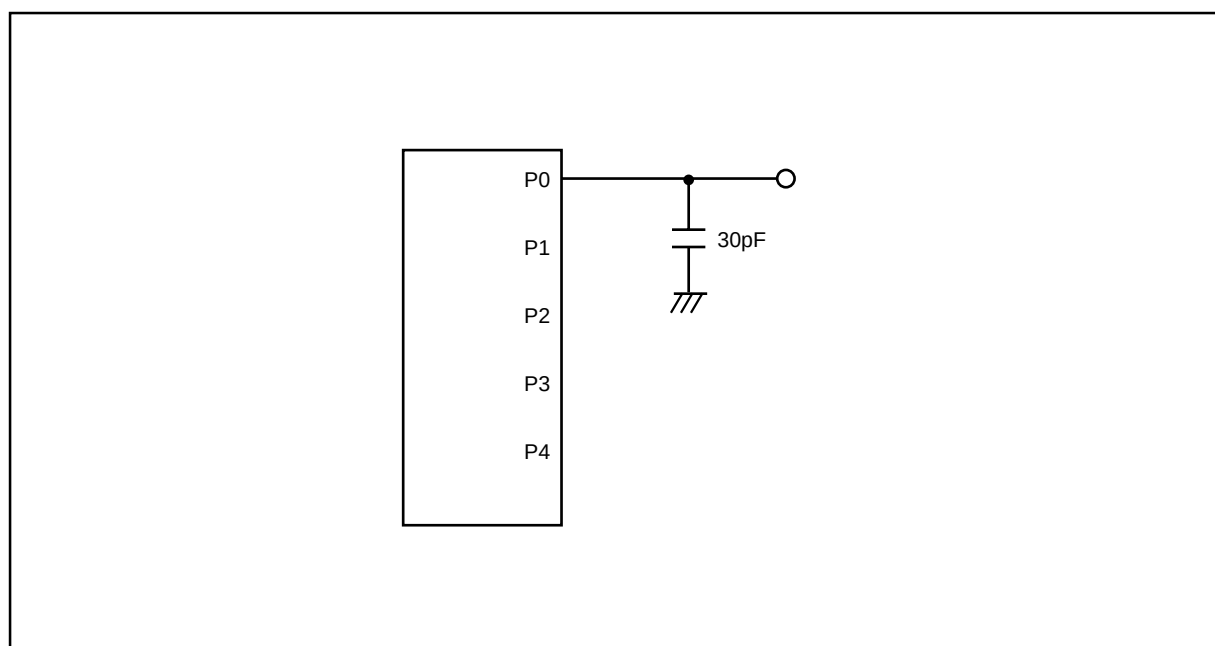
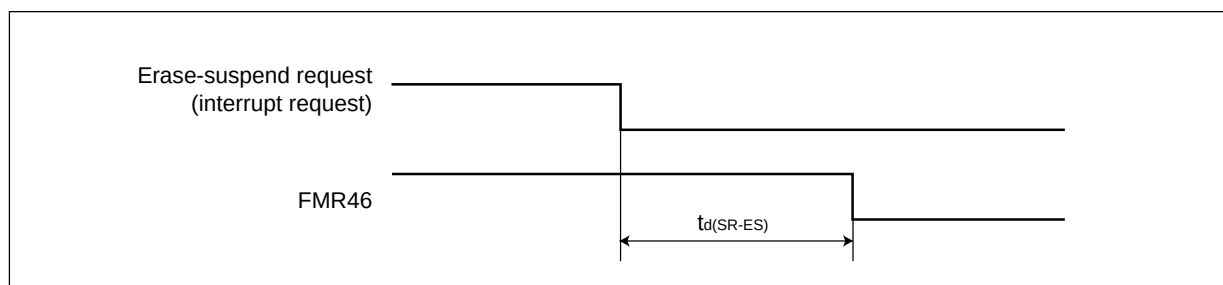
**Figure 5.1 Port P0 to P4 measurement circuit**

Table 5.5 Flash Memory (Data flash Block A, Block B) Electrical Characteristics⁽⁴⁾

Symbol	Parameter	Measuring condition	Standard			Unit
			Min.	Typ.	Max	
—	Program/Erase endurance ⁽²⁾		10000 ⁽³⁾	—	—	times
—	Byte program time(program/erase endurance ≤1000 times)		—	50	400	μs
—	Byte program time(program/erase endurance >1000 times)		—	65	—	μs
—	Block erase time(program/erase endurance ≤1000 times)		—	0.2	9	s
—	Block erase time(program/erase endurance >1000 times)		—	0.3	—	s
t _d (SR-ES)	Time delay from Suspend Request until Erase Suspend		—	—	8	ms
—	Erase Suspend Request Interval		10	—	—	ms
—	Program, Erase Voltage		2.7	—	5.5	V
—	Read Voltage		2.7	—	5.5	V
—	Program/Erase Temperature		-20(-40) ⁽⁸⁾	—	85	°C
—	Data hold time ⁽⁹⁾	Ambient temperature = 55 °C	20	—	—	year

NOTES:

1. Referenced to V_{cc}=AV_{cc}=2.7 to 5.5V at T_{opr} = -20 to 85 °C / -40 to 85 °C unless otherwise specified.
2. Definition of Program/Erase
The endurance of Program/Erase shows a time for each block.
If the program/erase number is "n" (n = 1,000, 10,000), "n" times erase can be performed for each block.
For example, if performing one-byte write to the distinct addresses on Block A of 2K-byte block 2048 times and then erasing that block, the number of Program/Erase cycles is one time.
However, performing multiple writes to the same address before an erase operation is prohibited (overwriting prohibited).
3. Numbers of Program/Erase cycles for which all electrical characteristics is guaranteed.
4. Table 16.5 applies for Block A or B when the Program/Erase cycles are more than 1000. The byte program time up to 1000 cycles are the same as that of the program area (see Table 5.4).
5. To reduce the number of Program/Erase cycles, a block erase should ideally be performed after writing in series as many distinct addresses (only one time each) as possible. If programming a set of 16 bytes, write up to 128 sets and then erase them one time. This will result in ideally reducing the number of Program/Erase cycles. Additionally, averaging the number of Program/Erase cycles for Block A and B will be more effective. It is important to track the total number of block erases and restrict the number.
6. If error occurs during block erase, attempt to execute the clear status register command, then the block erase command at least three times until the erase error disappears.
7. Customers desiring Program/Erase failure rate information should contact their Renesas technical support representative.
8. -40 °C for D version.
9. The data hold time includes time that the power supply is off or the clock is not supplied.

**Figure 5.2 Time delay from Suspend Request until Erase Suspend****Table 5.6 Power Circuit Timing Characteristics**

Symbol	Parameter	Measuring condition	Standard			Unit
			Min.	Typ.	Max.	
t _d (P-R)	Time for internal power supply stabilization during powering-on ⁽²⁾		1	—	2000	μs
t _d (R-S)	STOP release time ⁽³⁾		—	—	150	μs

NOTES:

1. The measuring condition is V_{cc}=AV_{cc}=2.7 to 5.5 V and T_{opr}=25 °C.
2. This shows the waiting time until the internal power supply generating circuit is stabilized during powering-on.
3. This shows the time until BCLK starts from the interrupt acknowledgement to cancel stop mode.

Table 5.7 Electrical Characteristics (1) [Vcc=5V]

Symbol	Parameter		Measuring condition		Standard			Unit
					Min.	Typ.	Max.	
V _{OH}	"H" output voltage	Except X _{OUT}	I _{OH} =-5mA		V _{CC} -2.0	—	V _{CC}	V
			I _{OH} =-200μA		V _{CC} -0.3	—	V _{CC}	V
	X _{OUT}		Drive capacity HIGH	I _{OH} =-1 mA	V _{CC} -2.0	—	V _{CC}	V
			Drive capacity LOW	I _{OH} =-500μA	V _{CC} -2.0	—	V _{CC}	V
V _{OL}	"L" output voltage	Except P10 to P17, X _{OUT}	I _{OL} = 5 mA		—	—	2.0	V
			I _{OL} = 200 μA		—	—	0.45	V
	P10 to P17		Drive capacity HIGH	I _{OL} = 15 mA	—	—	2.0	V
			Drive capacity LOW	I _{OL} = 5 mA	—	—	2.0	V
			Drive capacity LOW	I _{OL} = 200 μA	—	—	0.45	V
	X _{OUT}		Drive capacity HIGH	I _{OL} = 1 mA	—	—	2.0	V
			Drive capacity LOW	I _{OL} =500 μA	—	—	2.0	V
V _{TH} -V _T	Hysteresis	INT0, INT1, INT2, INT3, K10, K11, K12, K13, CNTR0, CNTR1, TCIN, RxD0, RxD1, P45			0.2	—	1.0	V
		RESET			0.2	—	2.2	V
I _{IH}	"H" input current		V _I =5V		—	—	5.0	μA
I _{IL}	"L" input current		V _I =0V		—	—	-5.0	μA
R _{PULLUP}	Pull-up resistance		V _I =0V		30	50	167	kΩ
R _{XIN}	Feedback resistance	X _{IN}			—	1.0	—	MΩ
f _{RING-S}	Low-speed on-chip oscillator frequency				40	125	250	kHz
V _{RAM}	RAM retention voltage		At stop mode		2.0	—	—	V

NOTES:

1. Referenced to V_{CC} = AV_{CC} = 4.2 to 5.5V at T_{opr} = -20 to 85 °C / -40 to 85 °C, f(X_{IN})=20MHz unless otherwise specified.

Table 5.8 Electrical Characteristics (2) [Vcc=5V]

Symbol	Parameter		Measuring condition		Standard			Unit
					Min.	Typ.	Max.	
I _{CC}	Power supply current (V _{CC} =3.3 to 5.5V) In single-chip mode, the output pins are open and other pins are V _{SS}		High-speed mode	X _{IN} =16 MHz (square wave) On-chip oscillator on=125 kHz No division	—	8	14	mA
				X _{IN} =10 MHz (square wave) On-chip oscillator on=125 kHz No division	—	5	—	mA
			Medium-speed mode	X _{IN} =16 MHz (square wave) On-chip oscillator on=125 kHz Division by 8	—	3	—	mA
				X _{IN} =10 MHz (square wave) On-chip oscillator on=125 kHz Division by 8	—	2	—	mA
			On-chip oscillator mode	Main clock off On-chip oscillator on=125 kHz Division by 8	—	470	900	μA
			Wait mode	Main clock off On-chip oscillator on=125 kHz When a WAIT instruction is executed ⁽¹⁾ Peripheral clock operation	—	40	80	μA
			Wait mode	Main clock off On-chip oscillator on=125 kHz When a WAIT instruction is executed ⁽¹⁾ Peripheral clock off	—	38	76	μA
			Stop mode	Main clock off, T _{opr} = 25 °C On-chip oscillator off CM10="1" Peripheral clock off	—	0.8	3.0	μA

NOTES:

1. Timer Y is operated with timer mode.
2. Referenced to V_{CC} = AV_{CC} = 4.2 to 5.5V at T_{opr} = -20 to 85 °C / -40 to 85 °C, f(X_{IN})=20MHz unless otherwise specified.

Timing requirements (Unless otherwise noted: $V_{CC} = 5V$, $V_{SS} = 0V$ at $T_{opr} = 25\text{ }^{\circ}C$) [$V_{CC}=5V$]**Table 5.9 X_{IN} input**

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_C(X_{IN})$	X_{IN} input cycle time	62.5	—	ns
$t_{WH}(X_{IN})$	X_{IN} input HIGH pulse width	30	—	ns
$t_{WL}(X_{IN})$	X_{IN} input LOW pulse width	30	—	ns

Table 5.10 $CNTR0$ input, $CNTR1$ input, $\overline{INT2}$ input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_C(CNTR0)$	$CNTR0$ input cycle time	100	—	ns
$t_{WH}(CNTR0)$	$CNTR0$ input HIGH pulse width	40	—	ns
$t_{WL}(CNTR0)$	$CNTR0$ input LOW pulse width	40	—	ns

Table 5.11 $TCIN$ input, $\overline{INT3}$ input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_C(TCIN)$	$TCIN$ input cycle time	400 ⁽¹⁾	—	ns
$t_{WH}(TCIN)$	$TCIN$ input HIGH pulse width	200 ⁽²⁾	—	ns
$t_{WL}(TCIN)$	$TCIN$ input LOW pulse width	200 ⁽²⁾	—	ns

NOTES:

1. When using the Timer C capture function, adjust the cycle time above (1/ Timer C count source frequency x 3).
2. When using the Timer C capture function, adjust the pulse width above (1/ Timer C count source frequency x 1.5).

Table 5.12 Serial Interface

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_C(CLK_i)$	CLK_i input cycle time	200	—	ns
$t_{W(CLK_H)}$	CLK_i input HIGH pulse width	100	—	ns
$t_{W(CLK_L)}$	CLK_i input LOW pulse width	100	—	ns
$t_d(C-Q)$	TxD_i output delay time	—	80	ns
$t_h(C-Q)$	TxD_i hold time	0	—	ns
$t_{su}(D-C)$	RxD_i input setup time	35	—	ns
$t_h(C-D)$	RxD_i input hold time	90	—	ns

Table 5.13 External interrupt $\overline{INT0}$ input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{W(INH)}$	$\overline{INT0}$ input HIGH pulse width	250 ⁽¹⁾	—	ns
$t_{W(INL)}$	$\overline{INT0}$ input LOW pulse width	250 ⁽²⁾	—	ns

NOTES:

1. When selecting the digital filter by the $\overline{INT0}$ input filter select bit, use the $\overline{INT0}$ input HIGH pulse width to the greater value, either (1/ digital filter clock frequency x 3) or the minimum value of standard.
2. When selecting the digital filter by the $\overline{INT0}$ input filter select bit, use the $\overline{INT0}$ input LOW pulse width to the greater value, either (1/ digital filter clock frequency x 3) or the minimum value of standard.

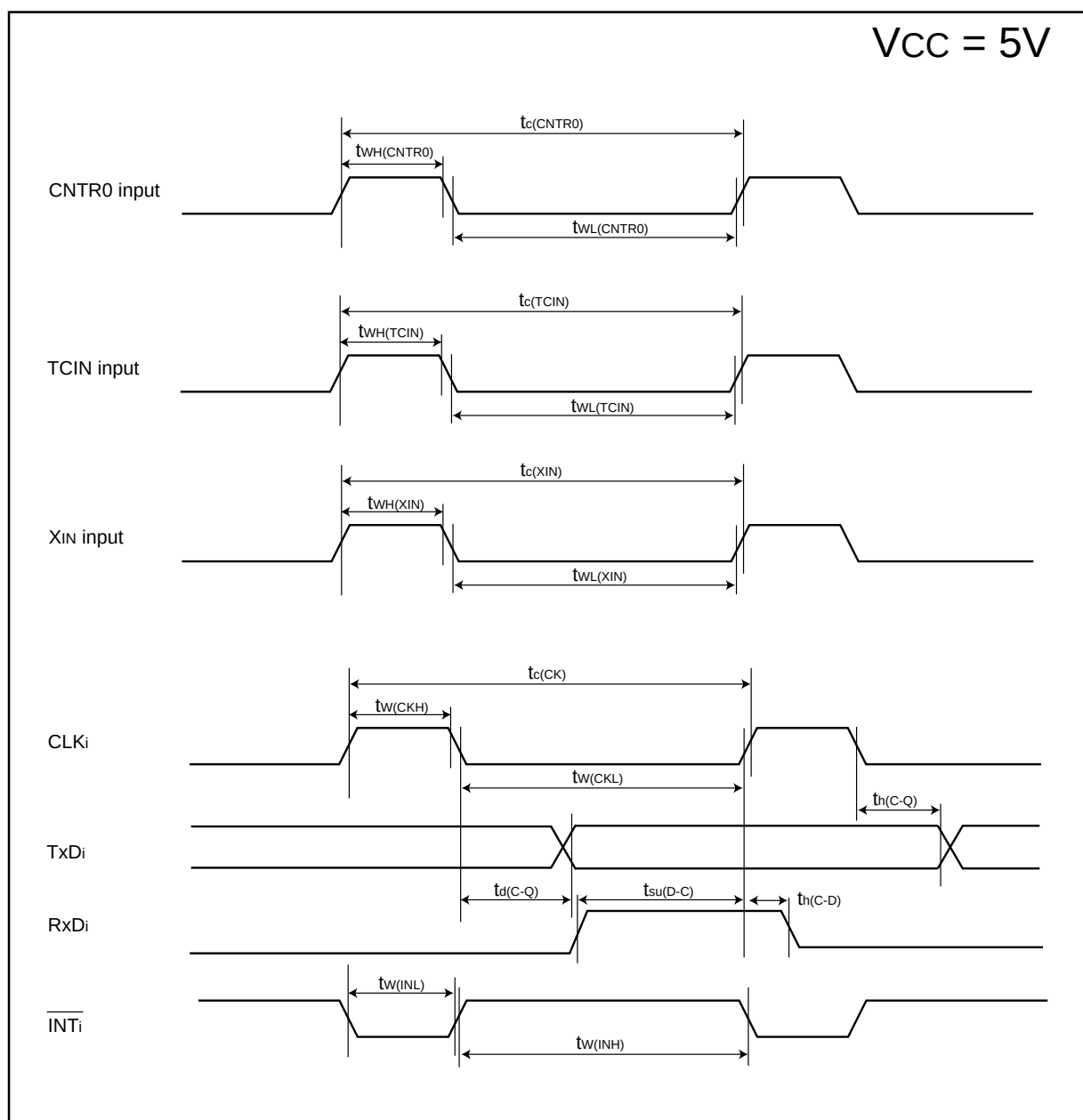
Figure 5.3 $V_{CC}=5V$ timing diagram

Table 5.14 Electrical Characteristics (3) [Vcc=3V]

Symbol	Parameter		Measuring condition		Standard			Unit
					Min.	Typ.	Max.	
V _{OH}	"H" output voltage	Except X _{OUT}	I _{OH} =-1mA		V _{CC} -0.5	—	V _{CC}	V
		X _{OUT}	Drive capacity HIGH	I _{OH} =-0.1 mA	V _{CC} -0.5	—	V _{CC}	V
			Drive capacity LOW	I _{OH} =-50 μA	V _{CC} -0.5	—	V _{CC}	V
V _{OL}	"L" output voltage	Except P10 to P17, X _{OUT}	I _{OL} = 1 mA		—	—	0.5	V
		P10 to P17	Drive capacity HIGH	I _{OL} = 2 mA	—	—	0.5	V
			Drive capacity LOW	I _{OL} = 1 mA	—	—	0.5	V
		X _{OUT}	Drive capacity HIGH	I _{OL} = 0.1 mA	—	—	0.5	V
			Drive capacity LOW	I _{OL} =50 μA	—	—	0.5	V
V _{T+} -V _{T-}	Hysteresis	INT0, INT1, INT2, INT3, KI0, KI1, KI2, KI3, CNTR0, CNTR1, TCIN, RxD0, RxD1, P45			0.2	—	0.8	V
		RESET			0.2	—	1.8	V
I _{IH}	"H" input current		V _I =3V		—	—	4.0	μA
I _{IL}	"L" input current		V _I =0V		—	—	-4.0	μA
R _{PULLUP}	Pull-up resistance		V _I =0V		66	160	500	kΩ
R _{FXIN}	Feedback resistance	X _{IN}			—	3.0	—	MΩ
f _{RING}	On-chip oscillator frequency				40	125	250	kHz
V _{RAM}	RAM retention voltage		At stop mode		2.0	—	—	V

NOTES:

1. Referenced to V_{CC}=AV_{CC}=2.7 to 3.3V at T_{OP} = -20 to 85 °C / -40 to 85 °C, f(X_{IN})=10MHz unless otherwise specified.

Timing requirements (Unless otherwise noted: $V_{CC} = 3V$, $V_{SS} = 0V$ at $T_{opr} = 25\text{ }^{\circ}C$) [$V_{CC}=3V$]**Table 5.16 X_{IN} input**

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_C(X_{IN})$	X_{IN} input cycle time	100	—	ns
$t_{WH}(X_{IN})$	X_{IN} input HIGH pulse width	40	—	ns
$t_{WL}(X_{IN})$	X_{IN} input LOW pulse width	40	—	ns

Table 5.17 CNTR0 input, CNTR1 input, $\overline{INT2}$ input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_C(CNTR0)$	CNTR0 input cycle time	300	—	ns
$t_{WH}(CNTR0)$	CNTR0 input HIGH pulse width	120	—	ns
$t_{WL}(CNTR0)$	CNTR0 input LOW pulse width	120	—	ns

Table 5.18 TCIN input, $\overline{INT3}$ input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_C(TCIN)$	TCIN input cycle time	1200 ⁽¹⁾	—	ns
$t_{WH}(TCIN)$	TCIN input HIGH pulse width	600 ⁽²⁾	—	ns
$t_{WL}(TCIN)$	TCIN input LOW pulse width	600 ⁽²⁾	—	ns

NOTES:

1. When using the Timer C capture function, adjust the cycle time above (1/ Timer C count source frequency x 3).
2. When using the Timer C capture function, adjust the pulse width above (1/ Timer C count source frequency x 1.5).

Table 5.19 Serial Interface

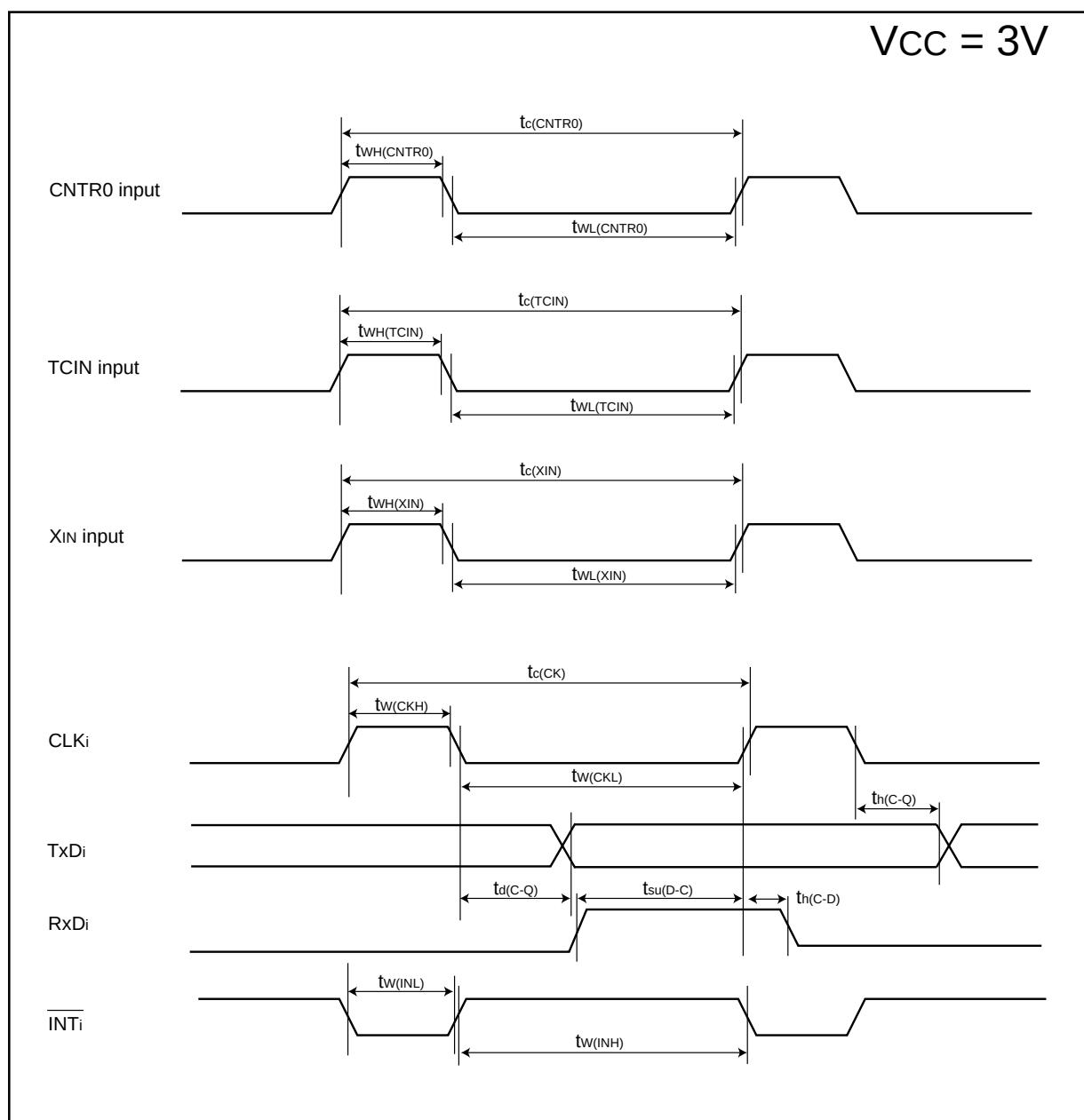
Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_C(CLK_i)$	CLK_i input cycle time	300	—	ns
$t_W(CLK_H)$	CLK_i input HIGH pulse width	150	—	ns
$t_W(CLK_L)$	CLK_i input LOW pulse width	150	—	ns
$t_d(C-Q)$	TxD_i output delay time	—	160	ns
$t_h(C-Q)$	TxD_i hold time	0	—	ns
$t_{su}(D-C)$	RxD_i input setup time	55	—	ns
$t_h(C-D)$	RxD_i input hold time	90	—	ns

Table 5.20 External interrupt $\overline{INT0}$ input

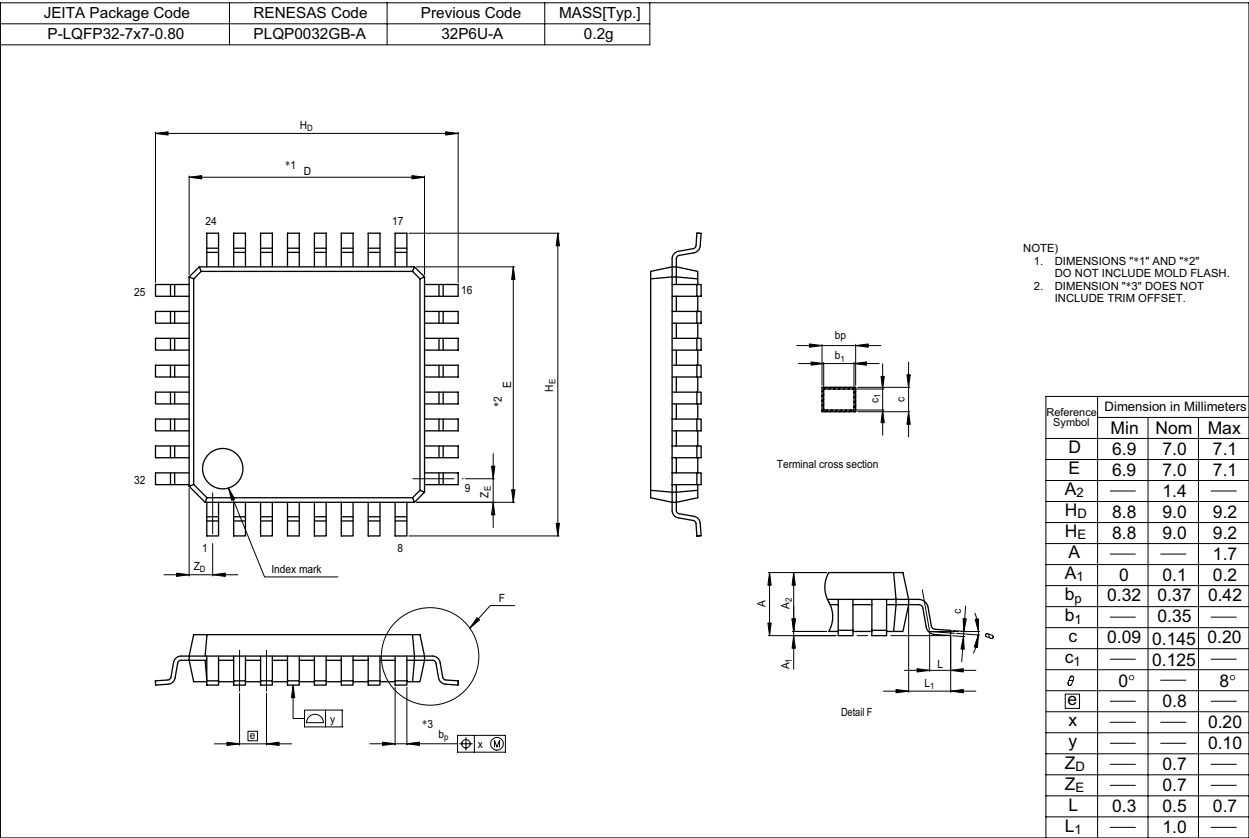
Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_W(\overline{INT0}_H)$	$\overline{INT0}$ input HIGH pulse width	380 ⁽¹⁾	—	ns
$t_W(\overline{INT0}_L)$	$\overline{INT0}$ input LOW pulse width	380 ⁽²⁾	—	ns

NOTES:

1. When selecting the digital filter by the $\overline{INT0}$ input filter select bit, use the $\overline{INT0}$ input HIGH pulse width to the greater value, either (1/ digital filter clock frequency x 3) or the minimum value of standard.
2. When selecting the digital filter by the $\overline{INT0}$ input filter select bit, use the $\overline{INT0}$ input LOW pulse width to the greater value, either (1/ digital filter clock frequency x 3) or the minimum value of standard.

Figure 5.4 $V_{CC}=3V$ timing diagram

Package Dimensions



REVISION HISTORY	R8C/12 Group Datasheet
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Rev.	Date	Description	
		Page	Summary
0.10	Oct 28, 2003		First edition issued
0.20	Dec05, 2003	16	Table 16.5 revised
1.00	Sep30, 2004	All pages	Words standardized (on-chip oscillator, serial interface, A/D)
		2	Table 1.1 revised
		5	Figure 1.3, NOTES 3 added
		6	Table 1.3 revised
		9	Figure 3.1, NOTES added
		10-13	One body sentence in chapter 4 added ; Titles of Table 4.1 to 4.4 added
		12	Table 4.3 revised ; Table 4.4 revised
		14	Table 5.2 revised
		15	Table 5.3 revised
		16	Table 5.4 and 5.5 revised
		17	Table 5.7 revised
		18	Table 5.8 revised
		19	Table 5.13 revised
		21	Table 5.14 revised
		22	Table 5.15 revised
		23	Table 5.17 revised
1.10	Apr.27.2005	4	Table 1.2, Figure 1.2 package name revised
		5	Figure 1.3 package name revised
		10	Table 4.1 revised
		12	Table 4.3 revised
		15	Table 5.3 partly revised
		16	Table 5.4, Table 5.5 partly added
		17	Table 5.6, Table 5.7 partly revised
		21	Table 5.14 partly revised
		26	Package Dimensions revised
1.20	Jan.27.2006	2	Table 1.1 Performance outline revised
		3	Figure 1.1 Block diagram partly revised
		4	1.4 Product Information, title of Table 1.2
			“Product List” → “Product Informaton” revised
			ROM capacity; “Program area” → “Program ROM”,
			“Data area” → “Data flash” revised
			Figure 1.2 Type No., Memory Size, and Package partly revised
		6	Table 1.3 Pin description revised
		7-8	2 Central Processing Unit (CPU) revised
			Figure 2.1 CPU register revised
		9	3 Memory, Figure 3.1 Memory Map;
			“Program area” → “Program ROM”, “Data area” → “Data flash” revised
		10	Table 4.1 SFR Information(1) NOTES:1 revised