Renesas Electronics America Inc - R8A77440HA01BG#UA Datasheet

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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Not For New Designs
Core Processor	ARM® Cortex®-A15
Number of Cores/Bus Width	-
Speed	1.5GHz
Co-Processors/DSP	-
RAM Controllers	-
Graphics Acceleration	-
Display & Interface Controllers	-
Ethernet	-
SATA	-
USB	-
Voltage - I/O	-
Operating Temperature	-40°C ~ 85°C (TA)
Security Features	-
Package / Case	-
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r8a77440ha01bg-ua

General Precautions in the Handling of MPU/MCU Products

The following usage notes are applicable to all MPU/MCU products from Renesas. For detailed usage notes on the products covered by this manual, refer to the relevant sections of the manual. If the descriptions under General Precautions in the Handling of MPU/MCU Products and in the body of the manual differ from each other, the description in the body of the manual takes precedence.

1. Handling of Unused Pins

   Handle unused pins in accord with the directions given under Handling of Unused Pins in the manual.

   ¾ The input pins of CMOS products are generally in the high-impedance state. In operation with unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on

   The state of the product is undefined at the moment when power is supplied.

   ¾ The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.
   In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.
   In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses

   Access to reserved addresses is prohibited.

   ¾ The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock Signals

   After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

   ¾ When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

5. Differences between Products

   Before changing from one product to another, i.e. to one with a different part number, confirm that the change will not lead to problems.

   ¾ The characteristics of MPU/MCU in the same group but having different part numbers may differ because of the differences in internal memory capacity and layout pattern. When changing to products of different part numbers, implement a system-evaluation test for each of the products.

Item	Description
LBSC-DMAC	• Three channels • Address space: Physical address space • Transfer direction: Peripheral to memory (AXI-bus), memory (AXI-bus) to peripheral • Data packing for peripheral read data: Memory write data length is selectable as transfer data length to memory side. • Transfer data length: Peripheral (APB-bus) side: 1, 2, 4 bytes Memory (AXI-bus) side: 4 or 16 (channel 2), 32 (channels 0 and 1) bytes • Transfer burst length: 1, 8 (transfer with a burst length of 8 supported only for LBSCDMAC00, 01) • Number of transfers — Maximum number of transfers: 16 M (16,777,216 transfers), 64M (67,108,864 transfers), (64 M transfers supported only for LBSC-DMAC00) — Minimum number of transfers: One • Address mode: Dual address mode • Transfer modes: Single transfer mode, continuous transfer mode • Transfer end interrupt: Occurs at the end of the number of transfers specified in the register
External bus controller for DDR3-SDRAM (DBSC3)	• Single channel (32-bit bus) • DDR3L-SDRAM can be connected directly. • Memory Size: Up to 4 Gbytes (8-Gbit memory × 4) • Data bus width: 32 bits • Auto Refresh/Self Refresh/Partial Array Self Refresh supported • Deep-Power-Down-Mode supported • Auto Pre-charge Mode/Bank Active Mode • DDR Back Up supported
Memory connections	DDR3-SDRAM compliant to JEDEC JESD79-3E Supports from 512-Mbit to 4-Gbit memory unit configurations 32-bit DDR3L-1600 (four units with 8-bit width)

Item	Description
Fine display processor 1 (FDP1)	The FDP1 is the de-interlacing module which converts the interlaced video to progressive video, and has the following features. (1) Supports various data formats — Input: YCbCr444/422/420 — Output: YCbCr444/422/420 and RGB/αRGB (2) Full HD video processing performance (3) High image quality de-interlacing algorithm — Motion adaptive de-interlacing — Accurate still detection — Diagonal line interpolation (DLI)
Image extraction direct memory access controller (2D-DMAC)	• Supports conversion between various RGB formats. • Image extraction function: Capable of extracting an image and storing it as a separate image in the RAM. • Image rotation/reversal function: Reverses an image vertically/horizontally or rotates it by 90°/270°. • Simple scaling function: Capable of scaling an image two times in the X or Y direction. • Format conversion • Supports conversion from RGB to RGB and from YCbCr to YCbCr.

Item	Description
Timer pulse unit (TPU)	• 4-channel 16-bit timers • Each channel outputs PWM
Compare match timer 0 (CMT0)	• 32-bit timer, two channels (16 bits/32 bits can be selected) • Source clock: RCLK clock • Compare match function provided • Interrupt requests
Compare match timer 1 (CMT1)	• 48-bit timer, eight channels (16 bits/32 bits/48 bits can be selected) • Source clock: RCLK/system clock • Compare match function provided • Interrupt requests
Timer unit (TMU)	• Four sets of 3-channel 32-bit timer • Auto-reload type 32-bit down counter • Internal prescaler • Interrupt request • Two channels for input capture

CPG, RESET, SYSTEM, AVS, POWER ISO and Debug (No.189 to 212): Single Function

	Function 1	
No.	Module	During POR
Pin No.	Pin Name	V/|IOH|
	I/O	Pull-up
189	CPG	I
AL18	EXTAL	1.8V/-
	I	-
190	CPG	O
AL17	XTAL	1.8V/-
	O	-
191	CPG	P
F16	VDD_CPGPLL1	-
	P	-
192	CPG	P
F15	VSS_CPGPLL1	-
	P	-
193	CPG	P
H15	VDD_CPGPLL1	-
	P	-
194	CPG	P
G15	VSS_CPGPLL1	-
	P	-
195	CPG	P
L25	VDD_CPGPLL0	-
	P	-
196	CPG	P
M25	VSS_CPGPLL0	-
	P	-
197	CPG	P
L26	VDD_CPGPLL3	-
	P	-
198	CPG	P
M26	VSS_CPGPLL3	-
	P	-
199	RESET	I(S)
AE19	PRESET#	1.8V/-
	I(S)	-
200	RESET	L
U5	PRESETOUT#	3.3V/4mA
	O(L to H)	-

	Function 1	
No.	Module	During POR
Pin No.	Pin Name	V/|IOH|
	I/O	Pull-up(pull-down)*2
201	SYSTEM	I(S)
AG19	MPMD0	1.8V/-
	I(S)	-
202	SYSTEM	I(S)
AG18	MPMD1	1.8V/-
	I(S)	-
203	SYSTEM	I(S)
AF17	BSMODE	1.8V/-
	I(S)	-
204	AVS	L
U6	AVS1	3.3V/4mA
	O(H/L)*1	Off
205	AVS	L
U7	AVS2	3.3V/4mA
	O(H/L)*1	Off
206	POWER ISO	P
AD19	VCCQ_ISO	-
	P	-
207	Debug	I
AF19	TRST#	1.8V/-
	I	On
208	Debug	I
AE18	TCK	1.8V/-
	I	On
209	Debug	I
AF18	TMS	1.8V/-
	I(I)	On
210	Debug	I
AH17	TDI	1.8V/-
	I	On
211	Debug	Z
AJ17	TDO	1.8V/8mA
	O(Z)	-
212	Debug	I
AE17	ACK	1.8V/4mA
	IO(I)	On(pulled-down)*2

Notes: 1. (No.204 and 205): Output value of the AVS[2:1] pins depends on each product.
2. (No.212): ACK pin is available for pull-down function.

VIN, EtherAVB, I2C, RCAN, MSIOF, SCIFA, TMU and GPIO (No.456 to 475): Up to 8-Function Multiplexed

These pins are set for GPIO after power-on reset. For details, refer to GPSR5 register in section 5, Pin Function Controller (PFC).

	Function								
	1	2	3	4	5	6	7	GPIO	
No.	Module								During POR
Pin No.	Pin Name								V/|IOH|
	I/O								Pull-up
456	VIN0	Reserved	SCIF1	RCAN0	I2C4	HSCIF1	SCIFB0		I(GPIO)
AG4	VI0_R7	–	RX1_C	CAN0_RX_E	I2C4_SDA_B	HRX1_D	SCIFB0_RXD_D	GP4_28	3.3V/4mA
	I	–	I	I	IO	I	I	IO(I)	Off
457	VIN1	EtherAVB	Reserved	SCIF4	SCIFA4	-	-		I(GPIO)
AF1	VI1_HSYNC#	AVB_RXD0	–	TX4_B	SCIFA4_TXD_B	-	-	GP5_0	3.3V/4mA
	I	I	–	O	O	-	-	IO(I)	On
458	VIN1	EtherAVB	Reserved	SCIF4	SCIFA4	-	-		I(GPIO)
AF2	VI1_VSYNC#	AVB_RXD1	–	RX4_B	SCIFA4_RXD_B	-	-	GP5_1	3.3V/4mA
	I	I	–	I	I	-	-	IO(I)	On
459	VIN1	EtherAVB	Reserved	-	-	-	-		I(GPIO)
AG3	VI1_CLKENB	AVB_RXD2	–	-	-	-	-	GP5_2	3.3V/4mA
	I	I	–	-	-	-	-	IO(I)	On
460	VIN1	EtherAVB	Reserved	-	-	-	-		I(GPIO)
AH2	VI1_FIELD	AVB_RXD3	–	-	-	-	-	GP5_3	3.3V/4mA
	I	I	–	-	-	-	-	IO(I)	On
461	VIN1	EtherAVB	-	-	-	-	-		I(GPIO)
AG1	VI1_CLK	AVB_RXD4	-	-	-	-	-	GP5_4	3.3V/4mA
	I	I	-	-	-	-	-	IO(I)	On
462	VIN1	EtherAVB	-	-	-	-	-		I(GPIO)
AH3	VI1_DATA0	AVB_RXD5	-	-	-	-	-	GP5_5	3.3V/4mA
	I	I	-	-	-	-	-	IO(I)	On
463	VIN1	EtherAVB	-	-	-	-	-		I(GPIO)
AH1	VI1_DATA1	AVB_RXD6	-	-	-	-	-	GP5_6	3.3V/4mA
	I	I	-	-	-	-	-	IO(I)	On
464	VIN1	EtherAVB	-	-	-	-	-		I(GPIO)
AJ1	VI1_DATA2	AVB_RXD7	-	-	-	-	-	GP5_7	3.3V/4mA
	I	I	-	-	-	-	-	IO(I)	On
465	VIN1	EtherAVB	-	-	-	-	-		I(GPIO)
AJ2	VI1_DATA3	AVB_RX_ER	-	-	-	-	-	GP5_8	3.3V/4mA
	I	I	-	-	-	-	-	IO(I)	On
466	VIN1	EtherAVB	-	-	-	-	-		I(GPIO)
AK1	VI1_DATA4	AVB_MDIO	-	-	-	-	-	GP5_9	3.3V/8mA
	I	IO	-	-	-	-	-	IO(I)	On
467	VIN1	EtherAVB	-	-	-	-	-		I(GPIO)
AL2	VI1_DATA5	AVB_RX_DV	-	-	-	-	-	GP5_10	3.3V/4mA
	I	I	-	-	-	-	-	IO(I)	On
468	VIN1	EtherAVB	-	-	-	-	-		I(GPIO)
AK3	VI1_DATA6	AVB_MAGIC	-	-	-	-	-	GP5_11	3.3V/8mA
	I	O	-	-	-	-	-	IO(I)	On
469	VIN1	EtherAVB	-	-	-	-	-		I(GPIO)
AJ4	VI1_DATA7	AVB_MDC	-	-	-	-	-	GP5_12	3.3V/8mA
	I	O	-	-	-	-	-	IO(I)	On
470	EtherMAC	EtherAVB	I2C2	-	-	-	-		I(GPIO)
AL3	ETH_MDIO	AVB_RX_CLK	I2C2_SCL_C	-	-	-	-	GP5_13	3.3V/4mA
	IO	I	IO	-	-	-	-	IO(I)	On
471	EtherMAC	EtherAVB	I2C2	-	-	-	-		I(GPIO)
AK4	ETH_CRS_DV	AVB_LINK	I2C2_SDA_C	-	-	-	-	GP5_14	3.3V/4mA
	I	I	IO	-	-	-	-	IO(I)	On
472	EtherMAC	EtherAVB	I2C3	IIC0(I2C7)	-	-	-		I(GPIO)
AL4	ETH_RX_ER	AVB_CRS	I2C3_SCL	IIC0_SCL	-	-	-	GP5_15	3.3V/4mA
	I	I	IO	IO	-	-	-	IO(I)	On
473	EtherMAC	EtherAVB	I2C3	IIC0(I2C7)	-	-	-		I(GPIO)
AH5	ETH_RXD0	AVB_PHY_INT	I2C3_SDA	IIC0_SDA	-	-	-	GP5_16	3.3V/4mA
	I	I	IO	IO	-	-	-	IO(I)	On
474	EtherMAC	EtherAVB	RCAN0	I2C2	MSIOF1	-	-		I(GPIO)
AL5	ETH_RXD1	AVB_GTXREFCLK	CAN0_TX_C	I2C2_SCL_D	MSIOF1_RXD_E	-	-	GP5_17	3.3V/4mA
	I	I	O	IO	I	-	-	IO(I)	On
475	EtherMAC	EtherAVB	RCAN0	I2C2	MSIOF1	-	-		I(GPIO)
AH6	ETH_LINK	AVB_TXD0	CAN0_RX_C	I2C2_SDA_D	MSIOF1_SCK_E	-	-	GP5_18	3.3V/8mA
	I	O	I	IO	IO	-	-	IO(I)	On

No.	Pin No.	Pin Name (Function 1)	I/O	During POR	Default Pin Function	Default State	Default Pull-up
214	AL24	(NC)	-	-	(NC)	-	-
215	AL25	(NC)	-	-	(NC)	-	-
216	AL26	(NC)	-	-	(NC)	-	-
217	AJ26	(NC)	-	-	(NC)	-	-
218	AJ25	(NC)	-	-	(NC)	-	-
219	AE23	(NC)	-	-	(NC)	-	-
220	AF24	(NC)	-	-	(NC)	-	-
221	AG24	(NC)	-	-	(NC)	-	-
222	AF23	(NC)	-	-	(NC)	-	-
223	AG23	(NC)	-	-	(NC)	-	-
224	AH24	(NC)	-	-	(NC)	-	-
225	AD23	(NC)	-	-	(NC)	-	-
226	AE24	(NC)	-	-	(NC)	-	-
227	AJ24	(NC)	-	-	(NC)	-	-
228	AK24	(NC)	-	-	(NC)	-	-
229	AK25	(NC)	-	-	(NC)	-	-
230	AK26	(NC)	-	-	(NC)	-	-
231	AK23	(NC)	-	-	(NC)	-	-
232	AL27	RIDP0_SATA	I	I	RIDP0_SATA/RIDP0_USB3/RIDP0_PCIe*4	I/I	-
233	AL28	RIDN0_SATA	I	I	RIDN0_SATA/RIDN0_USB3/RIDN0_PCIe*4	I/I	-
234	AL29	TODP0_SATA	O	O	TODP0_SATA/TODP0_USB3/TODP0_PCIe*4	O/O	-
235	AL30	TODN0_SATA	O	O	TODN0_SATA/TODN0_USB3/TODN0_PCIe*4	O/O	-
236	AJ28	CICREFP0_SATA	I	I	CICREFP0_SATA/CICREFP0_USB3/CICREFP0_PCIe*4	I/I	-
237	AJ27	CICREFN0_SATA	I	I	CICREFN0_SATA/CICREFN0_USB3/CICREFN0_PCIe*4	I/I	-
238	AF25	VSS_SATA0	-	P	VSS_SATA0/VSS_USB3/VSS_PCIe*4	P	-
239	AG26	VDDA_SATA0	-	P	VDDA_SATA0/VDDA_USB3/VDDA_PCIe*4	P	-
240	AH27	VDDA_SATA0	-	P	VDDA_SATA0/VDDA_USB3/VDDA_PCIe *4	P	-
241	AH25	VDDD_SATA0	-	P	VDDD_SATA0/VDDD_USB3/VDDD_PCIe *4	P	-
242	AH26	VDDD_SATA0	-	P	VDDD_SATA0/VDDD_USB3/VDDD_PCIe *4	P	-
243	AG25	VDDD_SATA0	-	P	VDDD_SATA0/VDDD_USB3/VDDD_PCIe *4	P	-
244	AD24	VSS_SATA0	-	P	VSS_SATA0/VSS_USB3/VSS_PCIe *4	P	-
245	AE25	VSS_SATA0	-	P	VSS_SATA0/VSS_USB3/VSS_PCIe *4	P	-
246	AF26	VSS_SATA0	-	P	VSS_SATA0/VSS_USB3/VSS_PCIe *4	P	-
247	AG27	VSS_SATA0	-	P	VSS_SATA0/VSS_USB3/VSS_PCIe *4	P	-
248	AK27	VSS_SATA0	-	P	VSS_SATA0/VSS_USB3/VSS_PCIe *4	P	-
249	AH28	VSS_SATA0	-	P	VSS_SATA0/VSS_USB3/VSS_PCIe *4	P	-
250	AK28	VSS_SATA0	-	P	VSS_SATA0/VSS_USB3/VSS_PCIe *4	P	-
251	AJ29	VSS_SATA0	-	P	VSS_SATA0/VSS_USB3/VSS_PCIe *4	P	-
252	AK29	VSS_SATA0	-	P	VSS_SATA0/VSS_USB3/VSS_PCIe *4	P	-
253	AK30	VSS_SATA0	-	P	VSS_SATA0/VSS_USB3/VSS_PCIe *4	P	-
254	AL31	VSS_SATA0	-	P	VSS_SATA0/VSS_USB3/VSS_PCIe *4	P	-
255	AL20	USB_EXTAL	I	I	USB_EXTAL	I	-
256	AL19	USB_XTAL	O	O	USB_XTAL	O	-

No.	Pin No.	Pin Name (Function 1)	I/O	During POR	Default Pin Function	Default State	Default Pull-up
300	Y7	D7	IO	I	D7/GP0_7*5	I/I	On
301	Y6	D8	IO	I	D8/GP0_8*5	I/I	On
302	Y5	D9	IO	I	D9/GP0_9*5	I/I	On
303	Y4	D10	IO	I	D10/GP0_10*5	I/I	On
304	Y3	D11	IO	I	D11/GP0_11*5	I/I	On
305	Y2	D12	IO	I	D12/GP0_12*5	I/I	On
306	Y1	D13	IO	I	D13/GP0_13*5	I/I	On
307	W2	D14	IO	I	D14/GP0_14*5	I/I	On
308	W1	D15	IO	I	D15/GP0_15*5	I/I	On
309	T7	A0	IO	I	A0/GP0_16*5	L/I	On
310	W7	A1	IO	I(MD28)	A1/GP0_17*5	L/I	Off
311	W6	A2	IO	I(MD23)	A2/GP0_18*5	L/I	Off
312	W5	A3	IO	I(MD13)	A3/GP0_19*5	L/I	Off
313	W4	A4	IO	I(MD24)	A4/GP0_20*5	L/I	Off
314	W3	A5	IO	I	A5/GP0_21*5	L/I	On
315	T6	A6	IO	I	A6/GP0_22*5	L/I	On
316	V7	A7	IO	I(MD27)	A7/GP0_23*5	L/I	Off
317	T5	A8	IO	I	A8/GP0_24*5	L/I	On
318	T4	A9	IO	I	A9/GP0_25*5	L/I	On
319	V6	A10	IO	I(MD22)	A10/GP0_26*5	L/I	Off
320	T3	A11	IO	I	A11/GP0_27*5	L/I	On
321	T2	A12	IO	I	A12/GP0_28*5	L/I	On
322	R7	A13	IO	I(MD21)	A13/GP0_29*5	L/I	Off
323	R6	A14	IO	I(MD19)	A14/GP0_30*5	L/I	Off
324	R5	A15	IO	I(MD20)	A15/GP0_31*5	L/I	Off
325	R4	A16	IO	I	A16/GP1_0*5	L/I	On
326	R3	A17	IO	I	A17/GP1_1*5	L/I	On
327	R2	A18	IO	I	A18/GP1_2*5	L/I	On
328	P7	A19	IO	I(MD14)	A19/GP1_3*5	L/I	Off
329	P6	A20	IO	I	A20/GP1_4*5	L/I	On
330	P5	A21	IO	I	A21/GP1_5*5	L/I	On
331	P4	A22	IO	I	A22/GP1_6*5	L/I	On
332	P3	A23	IO	I	A23/GP1_7*5	L/I	On
333	P2	A24	IO	I	A24/GP1_8*5	L/I	On
334	P1	A25	IO	I	A25/GP1_9*5	L/I	On
335	U1	CLKOUT	O	O	CLKOUT	O	-
336	T1	CS0#	IO	I	CS0#/GP1_10*5	H/I	On
337	R1	CS1#/A26	IO	I	[CS1#/A26]/GP1_11*5	[H or L]*6 /I	On
338	V1	EX_CS0#	IO	I	GP1_12	I	Off
339	N1	EX_CS1#	IO	I	GP1_13	I	On
340	N2	EX_CS2#	IO	I	GP1_14	I	On
341	V3	EX_CS3#	IO	I(MD9)	GP1_15	I	Off

No.	Pin No.	Pin Name (Function 1)	I/O	During POR	Default Pin Function	Default State	Default Pull-up
469	AJ4	VI1_DATA7	IO	I	GP5_12	I	On
470	AL3	ETH_MDIO	IO	I	GP5_13	I	On
471	AK4	ETH_CRS_DV	IO	I	GP5_14	I	On
472	AL4	ETH_RX_ER	IO	I	GP5_15	I	On
473	AH5	ETH_RXD0	IO	I	GP5_16	I	On
474	AL5	ETH_RXD1	IO	I	GP5_17	I	On
475	AH6	ETH_LINK	IO	I	GP5_18	I	On
476	AL6	ETH_REFCLK	IO	I	GP5_19	I	On
477	AJ5	ETH_TXD1	IO	I	GP5_20	I	On
478	AG6	ETH_TX_EN	IO	I	GP5_21	I	On
479	AJ6	ETH_MAGIC	IO	I	GP5_22	I	On
480	AG7	ETH_TXD0	IO	I	GP5_23	I	On
481	AF7	ETH_MDC	IO	I	GP5_24	I	On
482	AK8	STP_IVCXO27_0	IO	I	GP5_25	I	On
483	AL8	STP_ISCLK_0	IO	I	GP5_26	I	On
484	AH7	STP_ISD_0	IO	I	GP5_27	I	On
485	AJ7	STP_ISEN_0	IO	I	GP5_28	I	On
486	AK7	STP_ISSYNC_0	IO	I	GP5_29	I	On
487	AL7	STP_OPWM_0	IO	I	GP5_30	I	On
488	AL15	SD0_CLK	IO	I	GP6_0	I	Off
489	AH16	SD0_CMD	IO	I	GP6_1	I	Off
490	AG16	SD0_DATA0	IO	I	GP6_2	I	Off
491	AF16	SD0_DATA1	IO	I	GP6_3	I	Off
492	AE16	SD0_DATA2	IO	I	GP6_4	I	Off
493	AH15	SD0_DATA3	IO	I	GP6_5	I	Off
494	AJ15	SD0_CD	IO	I	GP6_6	I	Off
495	AJ16	SD0_WP	IO	I	GP6_7	I	Off
496	AD16	VCCQ_SD0	-	-	VCCQ_SD0	-	-
497	AL14	SD2_CLK	IO	I/Z*7	GP6_8/TDO2*8	I/Z*7	Off/-*9
498	AH14	SD2_CMD	IO	I	GP6_9/TRST2#*8	I/I	Off/-*9
499	AG15	SD2_DATA0	IO	I	GP6_10/TCK2*8	I/I	Off/-*9
500	AF15	SD2_DATA1	IO	I	GP6_11/TMS2*8	I/I	Off/-*9
501	AE15	SD2_DATA2	IO	I	GP6_12/TDI2*8	I/I	Off/-*9
502	AG14	SD2_DATA3	IO	I	GP6_13*8	I/I	Off/-*9
503	AJ14	SD2_CD	IO	I	GP6_14	I	Off
504	AF14	SD2_WP	IO	I	GP6_15	I	Off
505	AD15	VCCQ_SD2	-	P	VCCQ_SD2	P	-
506	AL13	SD3_CLK	IO	I/Z*7	GP6_16/TDO3*8	I/Z*7	Off/-*9
507	AH13	SD3_CMD	IO	I	GP6_17/TRST3#*8	I/I	Off/-*9
508	AG13	SD3_DATA0	IO	I	GP6_18/TCK3*8	I/I	Off/-*9
509	AF13	SD3_DATA1	IO	I	GP6_19/TMS3*8	I/I	Off/-*9
510	AE14	SD3_DATA2	IO	I	GP6_20/TDI3*8	I/I	Off/-*9
511	AE13	SD3_DATA3	IO	I	GP6_21*8	I/I	Off/-*9

No.	Pin No.	Pin Name (Function 1)	Default State	Mode Pin	Boot	Default Pull-up	Pin Handling when not in Use
99	J5	(NC)	-	-	-	-	Open, or connected to VSS or VDDQ_M0
100	H5	(NC)	-	-	-	-	Open, or connected to VSS or VDDQ_M0
101	L5	(NC)	-	-	-	-	Open, or connected to VSS or VDDQ_M0
102	K5	(NC)	-	-	-	-	Open, or connected to VSS or VDDQ_M0
103	F2	(NC)	-	-	-	-	Open, or connected to VSS or VDDQ_M0
104	G1	(NC)	-	-	-	-	Open, or connected to VSS or VDDQ_M0
105	F4	(NC)	-	-	-	-	Open, or connected to VSS or VDDQ_M0
106	H4	(NC)	-	-	-	-	Open, or connected to VSS or VDDQ_M0
107	L8	(NC)	-	-	-	-	Open, or connected to VSS or VDDQ_M0
108	E3	(NC)	-	-	-	-	Open, or connected to VSS or VDDQ_M0
109	D3	(NC)	-	-	-	-	Open, or connected to VSS or VDDQ_M0
110	E4	(NC)	-	-	-	-	Open, or connected to VSS or VDDQ_M0
111	B1	(NC)	-	-	-	-	Open, or connected to VSS or VDDQ_M0
112	H2	(NC)	-	-	-	-	Open, or connected to VSS or VDDQ_M0
113	E2	(NC)	-	-	-	-	Open, or connected to VSS or VDDQ_M0
114	M3	(NC)	-	-	-	-	Open, or connected to VSS or VDDQ_M0
115	E1	(NC)	-	-	-	-	Open, or connected to VSS or VDDQ_M0
116	D1	(NC)	-	-	-	-	Open, or connected to VSS or VDDQ_M0
117	K2	(NC)	-	-	-	-	Open, or connected to VSS or VDDQ_M0
118	H1	(NC)	-	-	-	-	Open, or connected to VSS or VDDQ_M0
119	M1	(NC)	-	-	-	-	Open, or connected to VSS or VDDQ_M0
120	J2	(NC)	-	-	-	-	Open, or connected to VSS or VDDQ_M0
121	L3	(NC)	-	-	-	-	Open, or connected to VSS or VDDQ_M0
122	K1	(NC)	-	-	-	-	Open, or connected to VSS or VDDQ_M0
123	C2	(NC)	-	-	-	-	Open, or connected to VSS or VDDQ_M0
124	L1	(NC)	-	-	-	-	Open, or connected to VSS or VDDQ_M0
125	M2	(NC)	-	-	-	-	Open, or connected to VSS or VDDQ_M0
126	K3	(NC)	-	-	-	-	Open, or connected to VSS or VDDQ_M0
127	J3	(NC)	-	-	-	-	Open, or connected to VSS or VDDQ_M0
128	C1	(NC)	-	-	-	-	Open, or connected to VSS or VDDQ_M0
129	H3	(NC)	-	-	-	-	Open, or connected to VSS or VDDQ_M0
130	L7	(NC)	-	-	-	-	Open, or connected to VSS or VDDQ_M0
131	K7	(NC)	-	-	-	-	Open, or connected to VSS or VDDQ_M0
132	L6	(NC)	-	-	-	-	Open, or connected to VSS or VDDQ_M0
133	K6	(NC)	-	-	-	-	Open, or connected to VSS or VDDQ_M0
134	B12	(NC)	-	-	-	-	Open, or connected to VSS or VDDQ_M0
135	B11	(NC)	-	-	-	-	Open, or connected to VSS or VDDQ_M0
136	D12	(NC)	-	-	-	-	Open, or connected to VSS or VDDQ_M0
137	A10	(NC)	-	-	-	-	Open, or connected to VSS or VDDQ_M0
138	C11	(NC)	-	-	-	-	Open, or connected to VSS or VDDQ_M0
139	D10	(NC)	-	-	-	-	Open, or connected to VSS or VDDQ_M0
140	C10	(NC)	-	-	-	-	Open, or connected to VSS or VDDQ_M0
141	D11	(NC)	-	-	-	-	Open, or connected to VSS or VDDQ_M0
142	E12	(NC)	-	-	-	-	Open, or connected to VSS or VDDQ_M0
143	E11	(NC)	-	-	-	-	Open, or connected to VSS or VDDQ_M0
144	A11	(NC)	-	-	-	-	Open, or connected to VSS or VDDQ_M0
145	G13	(NC)	-	-	-	-	Open, or connected to VSS or VDDQ_M0
146	G12	(NC)	-	-	-	-	Open, or connected to VSS or VDDQ_M0
147	G14	(NC)	-	-	-	-	Open, or connected to VSS or VDDQ_M0
148	A13	(NC)	-	-	-	-	Open, or connected to VSS or VDDQ_M0

No.	Pin No.	Pin Name (Function 1)	Default State	Mode Pin	Boot	Default Pull-up	Pin Handling when not in Use
398	AJ12	DU1_DR2	I	-	-	On	Open
399	AH12	DU1_DR3	I	-	-	On	Open
400	AG12	DU1_DR4	I	-	-	On	Open
401	AF12	DU1_DR5	I	-	-	On	Open
402	AE12	DU1_DR6	I	-	-	On	Open
403	AE11	DU1_DR7	I	-	-	On	Open
404	AL11	DU1_DG0	I	-	-	On	Open
405	AK11	DU1_DG1	I	-	-	On	Open
406	AJ11	DU1_DG2	I	-	-	On	Open
407	AH11	DU1_DG3	I	-	-	On	Open
408	AG11	DU1_DG4	I	-	-	On	Open
409	AF11	DU1_DG5	I	-	-	On	Open
410	AF10	DU1_DG6	I	-	-	On	Open
411	AE10	DU1_DG7	I	-	-	On	Open
412	AJ9	DU1_DB0	I	-	-	On	Open
413	AH9	DU1_DB1	I	-	-	On	Open
414	AG9	DU1_DB2	I	-	-	On	Open
415	AF9	DU1_DB3	I	-	-	On	Open
416	AE9	DU1_DB4	I	-	-	On	Open
417	AJ10	DU1_DB5	I	MD11	-	Off	Pulled-up to VCCQ or pulled-down to VSS
418	AH10	DU1_DB6	I	-	-	On	Open
419	AG10	DU1_DB7	I	-	-	On	Open
420	AL9	DU1_DOTCLKIN	I	-	-	On	Open
421	AL10	DU1_DOTCLKOUT0	I	-	-	On	Open
422	AK10	DU1_DOTCLKOUT1	I	-	-	On	Open
423	AE8	DU1_EXHSYNC/DU1_HSYNC	I	MD3	-	Off	Pulled-up to VCCQ or pulled-down to VSS
424	AF8	DU1_EXVSYNC/DU1_VSYNC	I	MD2	-	Off	Pulled-up to VCCQ or pulled-down to VSS
425	AG8	DU1_EXODDF/DU1_ODDF/DISP/CDE	I	-	-	On	Open
426	AH8	DU1_DISP	I	MD1	-	Off	Pulled-up to VCCQ or pulled-down to VSS
427	AJ8	DU1_CDE	I	MD0	-	Off	Pulled-up to VCCQ or pulled-down to VSS
428	AC1	VI0_CLK	I	-	-	On	Open
429	AB1	VI0_CLKENB	I	-	-	On	Open
430	AC2	VI0_FIELD	I	-	-	On	Open
431	AB2	VI0_HSYNC#	I	-	-	On	Open
432	AB3	VI0_VSYNC#	I	-	-	On	Open
433	AB4	VI0_DATA0/VI0_B0	I	-	-	On	Open
434	AB5	VI0_DATA1/VI0_B1	I	-	-	On	Open
435	AB6	VI0_DATA2/VI0_B2	I	-	-	On	Open
436	AC3	VI0_DATA3/VI0_B3	I	-	-	On	Open
437	AB7	VI0_DATA4/VI0_B4	I	-	-	On	Open
438	AC4	VI0_DATA5/VI0_B5	I	-	-	On	Open
439	AC6	VI0_DATA6/VI0_B6	I	-	-	On	Open
440	AC7	VI0_DATA7/VI0_B7	I	-	-	On	Open
441	AD1	VI0_G0	I	-	-	On	Open
442	AD2	VI0_G1	I	-	-	On	Open
443	AD3	VI0_G2	I	-	-	On	Open
444	AD4	VI0_G3	I	-	-	On	Open
445	AD5	VI0_G4	I	-	-	On	Open

No.	Pin No.	Pin Name (Function 1)	Default State	Mode Pin	Boot	Default Pull-up	Pin Handling when not in Use
546	K31	NC	-	-	-	-	Open
547	N31	NC	-	-	-	-	Open
548	M31	NC	-	-	-	-	Open
549	L29	NC	-	-	-	-	Open
550	L28	NC	-	-	-	-	Open
551	M29	NC	-	-	-	-	Open
552	M28	NC	-	-	-	-	Open
553	N25	VDD_MLBPPLL0	P	-	-	-	Must be used
554	P25	VSS_MLBPPLL0	P	-	-	-	Must be used
555	N26	VDD_MLBPPLL1	P	-	-	-	Must be used
556	P26	VSS_MLBPPLL1	P	-	-	-	Must be used
557	K28	VCCQ18_MLBP	P	-	-	-	Must be used
558	N28	VCCQ18_MLBP	P	-	-	-	Must be used
559	K29	VCCQ33_MLBP	P	-	-	-	Must be used
560	N29	VCCQ33_MLBP	P	-	-	-	Must be used
561	P27	VTHSENSE0	O	-	-	-	Open or fixed to VSS*3
562	N27	VTHREF0	O	-	-	-	Open or fixed to VSS*3

Notes: 1. No.293 to 325, 335 to 337, 344, 345 and 347 to 349: Boot
Minimum number of pins that is necessary for area 0 boot operation must be used.

2. No.329 to 334: Boot
These pins must be used for QSPI boot.

3. No.561 and 562: Pin handling when not in use
Thermal sensor should be idle state (THSCR.THIDLE[1:0] = B'11) when fixed to VSS. For details, refer to section 60, Thermal Sensor (THS/TSC).

5.3.5 GPIO/Peripheral Function Select Register 3 (GPSR3)

Function: GPSR3 selects the functions of the multiplexed LSI pins.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	GP3 [31]	GP3 [30]	GP3 [29]	GP3 [28]	GP3 [27]	GP3 [26]	GP3 [25]	GP3 [24]	GP3 [23]	GP3 [22]	GP3 [21]	GP3 [20]	GP3 [19]	GP3 [18]	GP3 [17]	GP3 [16]
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	GP3 [15]	GP3 [14]	GP3 [13]	GP3 [12]	GP3 [11]	GP3 [10]	GP3 [9]	GP3 [8]	GP3 [7]	GP3 [6]	GP3 [5]	GP3 [4]	GP3 [3]	GP3 [2]	GP3 [1]	GP3 [0]
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 0	GP3[31:0]	H'0000 0000	R/W	The functions of the LSI pins are selected according to the table below.

Note: To enable this register to be set, appropriately set the multiplexed pin setting mask register (PMMR) immediately before setting this register.

Bit Name	GPIO (Set Value = 0)	Peripheral Function (Set Value = 1)
GP3[0]	GP-3-0	Peripheral function selected by IP7[5:3]
GP3[1]	GP-3-1	Peripheral function selected by IP7[8:6]
GP3[2]	GP-3-2	Peripheral function selected by IP7[10:9]
GP3[3]	GP-3-3	Peripheral function selected by IP7[12:11]
GP3[4]	GP-3-4	Peripheral function selected by IP7[14:13]
GP3[5]	GP-3-5	Peripheral function selected by IP7[16:15]
GP3[6]	GP-3-6	Peripheral function selected by IP7[18:17]
GP3[7]	GP-3-7	Peripheral function selected by IP7[20:19]
GP3[8]	GP-3-8	Peripheral function selected by IP7[23:21]
GP3[9]	GP-3-9	Peripheral function selected by IP7[26:24]
GP3[10]	GP-3-10	Peripheral function selected by IP7[29:27]
GP3[11]	GP-3-11	Peripheral function selected by IP8[2:0]
GP3[12]	GP-3-12	Peripheral function selected by IP8[5:3]
GP3[13]	GP-3-13	Peripheral function selected by IP8[8:6]
GP3[14]	GP-3-14	Peripheral function selected by IP8[11:9]
GP3[15]	GP-3-15	Peripheral function selected by IP8[14:12]
GP3[16]	GP-3-16	Peripheral function selected by IP8[17:15]
GP3[17]	GP-3-17	Peripheral function selected by IP8[20:18]
GP3[18]	GP-3-18	Peripheral function selected by IP8[23:21]
GP3[19]	GP-3-19	Peripheral function selected by IP8[25:24]
GP3[20]	GP-3-20	Peripheral function selected by IP8[27:26]
GP3[21]	GP-3-21	Peripheral function selected by IP8[30:28]
GP3[22]	GP-3-22	Peripheral function selected by IP9[2:0]
GP3[23]	GP-3-23	Peripheral function selected by IP9[5:3]
GP3[24]	GP-3-24	Peripheral function selected by IP9[6]

5.3.7 GPIO/Peripheral Function Select Register 5 (GPSR5)

Function: GPSR5 selects the functions of the multiplexed LSI pins.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	GP5 [31]	GP5 [30]	GP5 [29]	GP5 [28]	GP5 [27]	GP5 [26]	GP5 [25]	GP5 [24]	GP5 [23]	GP5 [22]	GP5 [21]	GP5 [20]	GP5 [19]	GP5 [18]	GP5 [17]	GP5 [16]
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	GP5 [15]	GP5 [14]	GP5 [13]	GP5 [12]	GP5 [11]	GP5 [10]	GP5 [9]	GP5 [8]	GP5 [7]	GP5 [6]	GP5 [5]	GP5 [4]	GP5 [3]	GP5 [2]	GP5 [1]	GP5 [0]
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 0	GP5[31:0]	H'0000 0000	R/W	The functions of the LSI pins are selected according to the table below.

Note: To enable this register to be set, appropriately set the multiplexed pin setting mask register (PMMR) immediately before setting this register.

Bit Name	GPIO (Set Value = 0)	Peripheral Function (Set Value = 1)
GP5[0]	GP-5-0	Peripheral function selected by IP11[11:9]
GP5[1]	GP-5-1	Peripheral function selected by IP11[14:12]
GP5[2]	GP-5-2	Peripheral function selected by IP11[16:15]
GP5[3]	GP-5-3	Peripheral function selected by IP11[18:17]
GP5[4]	GP-5-4	Peripheral function selected by IP11[19]
GP5[5]	GP-5-5	Peripheral function selected by IP11[20]
GP5[6]	GP-5-6	Peripheral function selected by IP11[21]
GP5[7]	GP-5-7	Peripheral function selected by IP11[22]
GP5[8]	GP-5-8	Peripheral function selected by IP11[23]
GP5[9]	GP-5-9	Peripheral function selected by IP11[24]
GP5[10]	GP-5-10	Peripheral function selected by IP11[25]
GP5[11]	GP-5-11	Peripheral function selected by IP11[26]
GP5[12]	GP-5-12	Peripheral function selected by IP11[27]
GP5[13]	GP-5-13	Peripheral function selected by IP11[29:28]
GP5[14]	GP-5-14	Peripheral function selected by IP11[31:30]
GP5[15]	GP-5-15	Peripheral function selected by IP12[1:0]
GP5[16]	GP-5-16	Peripheral function selected by IP12[3:2]
GP5[17]	GP-5-17	Peripheral function selected by IP12[6:4]
GP5[18]	GP-5-18	Peripheral function selected by IP12[9:7]
GP5[19]	GP-5-19	Peripheral function selected by IP12[12:10]
GP5[20]	GP-5-20	Peripheral function selected by IP12[15:13]
GP5[21]	GP-5-21	Peripheral function selected by IP12[17:16]
GP5[22]	GP-5-22	Peripheral function selected by IP12[19:18]
GP5[23]	GP-5-23	Peripheral function selected by IP12[21:20]
GP5[24]	GP-5-24	Peripheral function selected by IP12[23:22]

5.3.10 Peripheral Function Select Register 0 (IPSR0)

Function: IPSR0 selects the functions of the multiplexed LSI pins.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	IP0 [30]	IP0 [29]	IP0 [28]	IP0 [27]	IP0 [26]	IP0 [25]	IP0 [24]	IP0 [23]	IP0 [22]	IP0 [21]	IP0 [20]	IP0 [19]	IP0 [18]	IP0 [17]	IP0 [16]
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	IP0 [15]	IP0 [14]	IP0 [13]	IP0 [12]	IP0 [11]	IP0 [10]	IP0 [9]	IP0 [8]	IP0 [7]	IP0 [6]	IP0 [5]	IP0 [4]	IP0 [3]	IP0 [2]	IP0 [1]	IP0 [0]
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Initial Value	R/W	Description
31 to 0	H'0000 0000	R/W	The functions of the LSI pins are selected according to the table below.

Note: To enable this register to be set, appropriately set the multiplexed pin setting mask register (PMMR) immediately before setting this register.

Bit Name	Function 1 (Set Value = H'0)	Function 2 (Set Value = H'1)	Function 3 (Set Value = H'2)	Function 4 (Set Value = H'3)	Function 5 (Set Value = H'4)	Function 6 (Set Value = H'5)	Others (Set Value = H'6 to H'F)
IP0[0]	D0	—	—	—	—	—	—
IP0[1]	D1	—	—	—	—	—	—
IP0[2]	D2	—	—	—	—	—	—
IP0[3]	D3	—	—	—	—	—	—
IP0[4]	D4	—	—	—	—	—	—
IP0[5]	D5	—	—	—	—	—	—
IP0[6]	D6	—	—	—	—	—	—
IP0[7]	D7	—	—	—	—	—	—
IP0[8]	D8	—	—	—	—	—	—
IP0[9]	D9	—	—	—	—	—	—
IP0[10]	D10	—	—	—	—	—	—
IP0[11]	D11	—	—	—	—	—	—
IP0[12]	D12	—	—	—	—	—	—
IP0[13]	D13	—	—	—	—	—	—
IP0[14]	D14	—	—	—	—	—	—
IP0[15]	D15	—	—	—	—	—	—
IP0[18:16]	A0	ATAWR0#_C	MSIOF0_SCK_B	I2C0_SCL_C	PWM2_B	—	—
IP0[20:19]	A1	MSIOF0_SYNC_B	—	—	—	—	—
IP0[22:21]	A2	MSIOF0_SS1_B	—	—	—	—	—
IP0[24:23]	A3	MSIOF0_SS2_B	—	—	—	—	—
IP0[26:25]	A4	MSIOF0_TXD_B	—	—	—	—	—
IP0[28:27]	A5	MSIOF0_RXD_B	—	—	—	—	—
IP0[30:29]	A6	MSIOF1_SCK	—	—	—	—	—

Legend: — Setting prohibited

5.3.19 Peripheral Function Select Register 9 (IPSR9)

Function: IPSR9 selects the functions of the multiplexed LSI pins.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	IP9 [31]	IP9 [30]	IP9 [29]	IP9 [28]	IP9 [27]	IP9 [26]	IP9 [25]	IP9 [24]	IP9 [23]	IP9 [22]	IP9 [21]	IP9 [20]	IP9 [19]	IP9 [18]	IP9 [17]	IP9 [16]
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	IP9 [15]	IP9 [14]	IP9 [13]	IP9 [12]	IP9 [11]	IP9 [10]	IP9 [9]	IP9 [8]	IP9 [7]	IP9 [6]	IP9 [5]	IP9 [4]	IP9 [3]	IP9 [2]	IP9 [1]	IP9 [0]
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Initial Value	R/W	Description
31 to 0	H'0000 0000	R/W	The functions of the LSI pins are selected according to the table below.

Note: To enable this register to be set, appropriately set the multiplexed pin setting mask register (PMMR) immediately before setting this register.

Bit Name	Function 1 (Set Value = H'0)	Function 2 (Set Value = H'1)	Function 3 (Set Value = H'2)	Function 4 (Set Value = H'3)	Function 5 (Set Value = H'4)	Function 6 (Set Value = H'5)	Function 7 (Set Value = H'6)	Others (Set Value = H'7 to H'F)
IP9[2:0]	DU1_DB6	—	I2C3_SCL_C	RX3	SCIFA3_RXD	—	—	—
IP9[5:3]	DU1_DB7	—	I2C3_SDA_C	SCIF3_SCK	SCIFA3_SCK	—	—	—
IP9[6]	DU1_DOTCLKIN	—	—	—	—	—	—	—
IP9[7]	DU1_DOTCLKOUT0	—	—	—	—	—	—	—
IP9[10:8]	DU1_DOTCLKOUT1	—	CAN0_TX	TX3_B	I2C2_SCL_B	PWM4	—	—
IP9[11]	DU1_EXHSYNC_DU1_HSYNC	—	—	—	—	—	—	—
IP9[12]	DU1_EXVSYNC_DU1_VSYNC	—	—	—	—	—	—	—
IP9[15:13]	DU1_EXODDF_DU1_ODDF_DISP_CDE	—	CAN0_RX	RX3_B	I2C2_SDA_B	—	—	—
IP9[16]	DU1_DISP	—	—	—	—	—	—	—
IP9[18:17]	DU1_CDE	—	PWM4_B	—	—	—	—	—
IP9[20:19]	VI0_CLKENB	TX4	SCIFA4_TXD	—	—	—	—	—
IP9[22:21]	VI0_FIELD	RX4	SCIFA4_RXD	—	—	—	—	—
IP9[24:23]	VI0_HSYNC#	TX5	SCIFA5_TXD	—	—	—	—	—
IP9[26:25]	VI0_VSYNC#	RX5	SCIFA5_RXD	—	—	—	—	—
IP9[28:27]	VI0_DATA3_VI0_B3	SCIF3_SCK_B	SCIFA3_SCK_B	—	—	—	—	—
IP9[31:29]	VI0_G0	IIC1_SCL	—	I2C4_SCL	HCTS2#	SCIFB2_CTS#	ATAWR1#	—

Legend: — Setting prohibited

5.3.31 LSI Pin Pull-Up Control Register 0 (PUPR0)

Function: PUPR0 performs on/off control of the pull-up resistors.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	PUPR0 [31]	PUPR0 [30]	PUPR0 [29]	PUPR0 [28]	PUPR0 [27]	PUPR0 [26]	PUPR0 [25]	PUPR0 [24]	PUPR0 [23]	PUPR0 [22]	PUPR0 [21]	PUPR0 [20]	PUPR0 [19]	PUPR0 [18]	PUPR0 [17]	PUPR0 [16]
Initial value:	1	1	0	1	1	0	0	0	0	1	1	1	1	1	1	1
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	PUPR0 [15]	PUPR0 [14]	PUPR0 [13]	PUPR0 [12]	PUPR0 [11]	PUPR0 [10]	PUPR0 [9]	PUPR0 [8]	PUPR0 [7]	PUPR0 [6]	PUPR0 [5]	PUPR0 [4]	PUPR0 [3]	PUPR0 [2]	PUPR0 [1]	PUPR0 [0]
Initial value:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 0	PUPR0[31:0]	H'D87F FFFF	R/W	Performs individual on/off control of the pull-up resistor provided in each signal pin of the LSI. 0: Pull-up function is disabled. 1: Pull-up function is enabled.

Bit Name	Set Value = 1
PUPR0[31]	A9 pin is pulled up
PUPR0[30]	A8 pin is pulled up
PUPR0[29]	A7 pin is pulled up
PUPR0[28]	A6 pin is pulled up
PUPR0[27]	A5 pin is pulled up
PUPR0[26]	A4 pin is pulled up
PUPR0[25]	A3 pin is pulled up
PUPR0[24]	A2 pin is pulled up
PUPR0[23]	A1 pin is pulled up
PUPR0[22]	A0 pin is pulled up
PUPR0[21]	D15 pin is pulled up
PUPR0[20]	D14 pin is pulled up
PUPR0[19]	D13 pin is pulled up
PUPR0[18]	D12 pin is pulled up
PUPR0[17]	D11 pin is pulled up
PUPR0[16]	D10 pin is pulled up
PUPR0[15]	D9 pin is pulled up
PUPR0[14]	D8 pin is pulled up
PUPR0[13]	D7 pin is pulled up
PUPR0[12]	D6 pin is pulled up
PUPR0[11]	D5 pin is pulled up
PUPR0[10]	D4 pin is pulled up
PUPR0[9]	D3 pin is pulled up
PUPR0[8]	D2 pin is pulled up
PUPR0[7]	D1 pin is pulled up

Bit Name	Set Value = 1
PUPR3[6]	IRQ8 pin is pulled up
PUPR3[5]	IRQ7 pin is pulled up
PUPR3[4]	IRQ6 pin is pulled up
PUPR3[3]	IRQ5 pin is pulled up
PUPR3[2]	IRQ4 pin is pulled up
PUPR3[1]	IRQ3 pin is pulled up
PUPR3[0]	IRQ2 pin is pulled up

(2) Procedure for changing pin function from peripheral function to GPIO

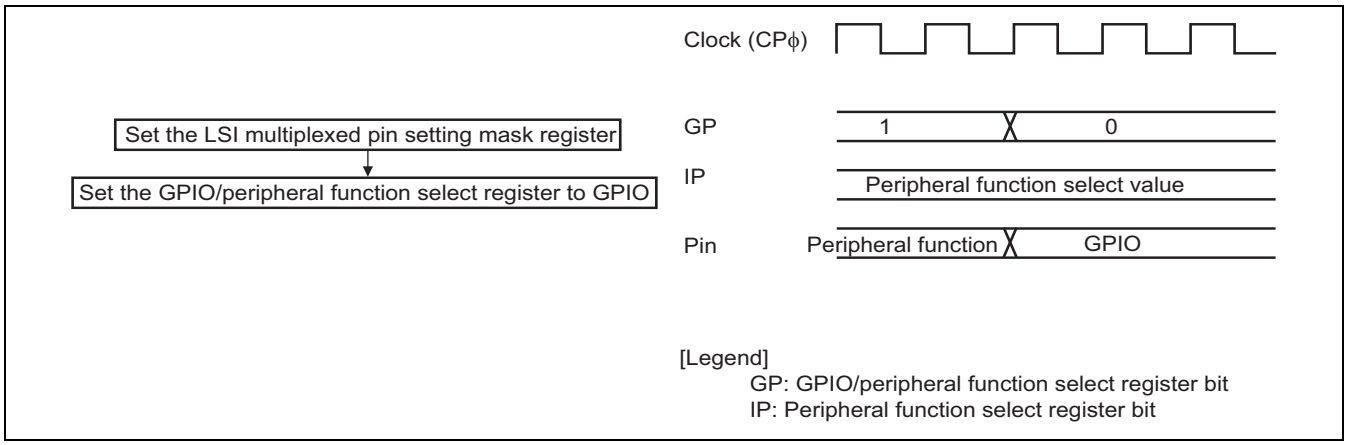

Figure 5.2 Procedure for Changing Pin Function from Peripheral function to GPIO

When changing pin function from peripheral function to GPIO of LSI pin in the below list, make sure to disable the data reception of corresponding SCIFAn channel before performing the sequence in the Figure 5.2.

LSI Pin	Pin Function
DU1_DB6	SCIFA3_RXD
ETH_REFCLK	SCIFA3_RXD_B
GPS_MAG	SCIFA4_RXD_C
GPS_SIGN	SCIFA3_RXD_C
SD0_WP	SCIFA5_RXD_B
SD3_WP	SCIFA5_RXD_C
VI0_FIELD	SCIFA4_RXD_
VI0_VSYNC#	SCIFA5_RXD
VI1_VSYNC#	SCIFA4_RXD_B

(3) Procedure 1 for changing pin function from one peripheral function to another peripheral function

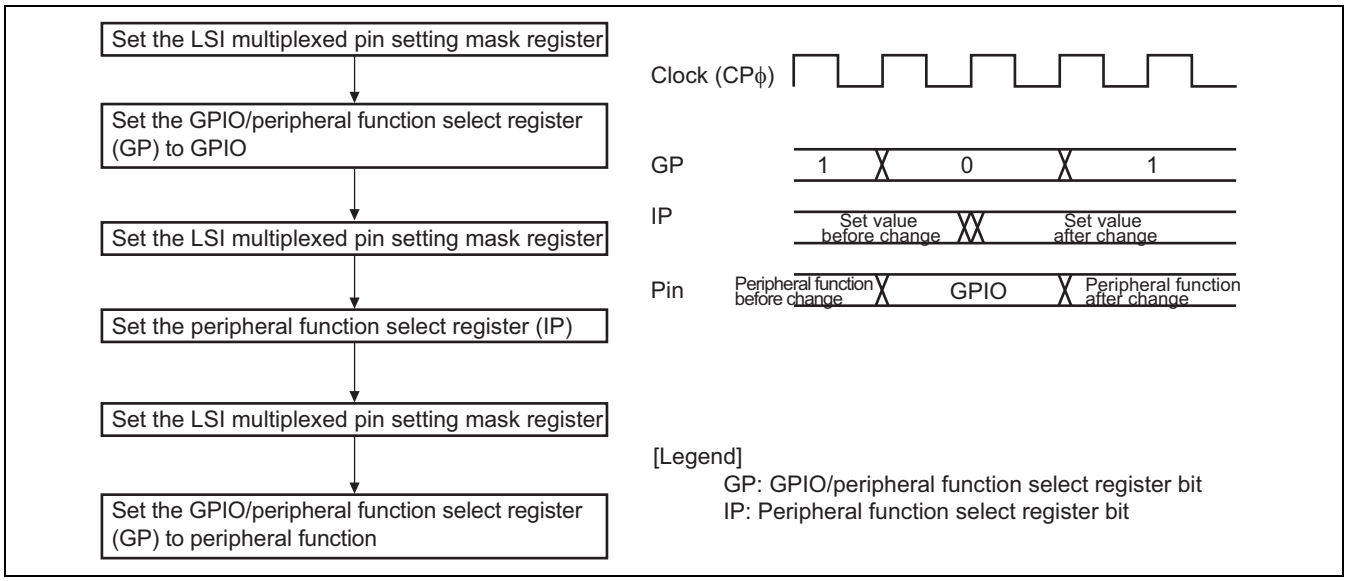

Figure 5.3 Procedure for Changing Pin Function from One Peripheral Function to Another Peripheral Function (with GPIO Setting)

Main Revisions and Additions in this Edition

Minor revisions such as corrections of errors in spelling and modifications of wording are not included in the revision history.

Rev.	Description		
	Page	Contents	Summary
1.00	—	First edition issued	