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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	56800E
Core Size	16-Bit
Speed	40MHz
Connectivity	EBI/EMI, SCI, SPI
Peripherals	POR, PWM, WDT
Number of I/O	49
Program Memory Size	128KB (64K x 16)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	4K x 16
Voltage - Supply (Vcc/Vdd)	2.25V ~ 3.6V
Data Converters	A/D 16x12b
Oscillator Type	External
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	128-LQFP
Supplier Device Package	128-LQFP (14x20)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mc56f8145vfge

2.2 Signal Pins

After reset, each pin is configured for its primary function (listed first). Any alternate functionality must be programmed.

EMI is not functional in this package; since only part of the address/data bus is bonded out, use as GPIO pins.

Note: *Signals in italics are NOT available in the 56F8145 device.*

If the "State During Reset" lists more than one state for a pin, the first state is the actual reset state. Other states show the reset condition of the alternate function, which you get if the alternate pin function is selected without changing the configuration of the alternate peripheral. For example, the A8/GPIOA0 pin shows that it is tri-stated during reset. If the GPIOA_PER is changed to select the GPIO function of the pin, it will become an input if no other registers are changed.

Table 2-2 Signal and Package Information for the 128-Pin LQFP

Signal Name	Pin No.	Type	State During Reset	Signal Description
V_{DD_IO}	4	Supply		**I/O Power** — This pin supplies 3.3V power to the chip I/O interface and also the Processor core throught the on-chip voltage regulator, if it is enabled.
V_{DD_IO}	14			
V_{DD_IO}	25			
V_{DD_IO}	36			
V_{DD_IO}	62			
V_{DD_IO}	76			
V_{DD_IO}	112			
V_{DDA_ADC}	94	Supply		**ADC Power** — This pin supplies 3.3V power to the ADC modules. It must be connected to a clean analog power supply.
$V_{DDA\_OSC\_PLL}$	72	Supply		**Oscillator** and **PLL Power** — This pin supplies 3.3V power to the OSC and to the internal regulator that in turn supplies the Phase Locked Loop. It must be connected to a clean analog power supply.
V_{SS}	3	Supply		**Ground** — These pins provide ground for chip logic and I/O drivers.
V_{SS}	21			
V_{SS}	35			
V_{SS}	59			
V_{SS}	65			

Table 2-2 Signal and Package Information for the 128-Pin LQFP

Signal Name	Pin No.	Type	State During Reset	Signal Description
CLKO	6	Output	In reset, output is disabled	**Clock Output** — This pin outputs a buffered clock signal. Using the SIM CLKO Select Register (SIM_CLKOSR), this pin can be programmed as any of the following: disabled, CLK_MSTR (system clock), IPBus clock, oscillator output, prescaler clock and postscaler clock. Other signals are also available for test purposes. See **Part 6.5.7** for details.
A8 **(GPIOA0)**	15	Output Schmitt Input/ Output	In reset, output is disabled, pull-up is enabled	**Address Bus** — A8 - A13 specify six of the address lines for external program or data memory accesses. Depending upon the state of the DRV bit in the EMI bus control register (BCR), A8 - A13 and EMI control signals are tri-stated when the external bus is inactive. **Port A GPIO** — These six GPIO pins can be individually programmed as input or output pins. After reset, these pins default to address bus functionality and must be programmed as GPIO. To deactivate the internal pull-up resistor, clear the appropriate GPIO bit in the GPIOA_PUR register. Example: GPIOA0, clear bit 0 in the GPIOA_PUR register. **Note:** Primary function is not available in this package configuration; GPIO function must be used instead.
A9 (GPIOA1)	16			
A10 (GPIOA2)	17			
A11 (GPIOA3)	18			
A12 (GPIOA4)	19			
A13 (GPIOA5)	20			
GPIOB0 **(A16)**	27	Schmitt Input/ Output Output	Input, pull-up enabled	**Port B GPIO** — These four GPIO pins can be individually programmed as an input or output pin. **Address Bus** — A16 - A19 specify four of the address lines for external program or data memory accesses. Depending upon the state of the DRV bit in the EMI bus control register (BCR), A16 - A19 and EMI control signals are tri-stated when the external bus is inactive. After reset, the default state is GPIO. To deactivate the internal pull-up resistor, clear bit 0 in the GPIOB_PUR register. Example: GPIOB1, clear bit 1 in the GPIOB_PUR register.
GPIOB1 **(A17)**	28			
GPIOB2 **(A18)**	29			
GPIOB3 **(A19)**	30			

Table 2-2 Signal and Package Information for the 128-Pin LQFP

Signal Name	Pin No.	Type	State During Reset	Signal Description
FAULTA0	67	Schmitt Input	Input, pull-up enabled	**FAULTA0 - 2** — These three fault input pins are used for disabling selected PWMA outputs in cases where fault conditions originate off-chip. To deactivate the internal pull-up resistor, set the PWMA0 bit in the SIM_PUDR register. See **Part 6.5.6** for details.
FAULTA1	68			
FAULTA2	69			
FAULTA3	70	Schmitt Input	Input, pull-up enabled	**FAULTA3** — This fault input pin is used for disabling selected PWMA outputs in cases where fault conditions originate off-chip. To deactivate the internal pull-up resistor, set the PWMA1 bit in the SIM_PUDR register. See **Part 6.5.6** for details.
PWMB0	32	Output	In reset, output is disabled, pull-up is enabled	**PWMB0 - 5** — Six PWMB output pins.
PWMB1	33			
PWMB2	34			
PWMB3	37			
PWMB4	38			
PWMB5	39			
ISB0 **(GPIOD10)**	48	Schmitt Input Schmitt Input/ Output	Input, pull-up enabled	**ISB0 - 2** — These three input current status pins are used for top/bottom pulse width correction in complementary channel operation for PWMB. **Port D GPIO** — These GPIO pins can be individually programmed as input or output pins. At reset, these pins default to ISB functionality. To deactivate the internal pull-up resistor, clear the appropriate bit of the GPIOD_PUR register. See **Part 6.5.6** for details.
ISB1 (GPIOD11)	50			
ISB2 (GPIOD12)	51			
FAULTB0	54	Schmitt Input	Input, pull-up enabled	**FAULTB0 - 3** — These four fault input pins are used for disabling selected PWMB outputs in cases where fault conditions originate off-chip. To deactivate the internal pull-up resistor, set the PWMB bit in the SIM_PUDR register. See **Part 6.5.6** for details.
FAULTB1	55			
FAULTB2	56			
FAULTB3	57			
ANA0	80	Input	Analog Input	**ANA0 - 3** — Analog inputs to ADC A, channel 0
ANA1	81			
ANA2	82			
ANA3	83			

Table 4-36 Power Supervisor Registers Address Map (LVI_BASE = $00 F360)

Register Acronym	Address Offset	Register Description
LVI_CONTROL	$0	Control Register
LVI_STATUS	$1	Status Register

Table 4-37 Flash Module Registers Address Map (FM_BASE = $00 F400)

Register Acronym	Address Offset	Register Description
FMCLKD	$0	Clock Divider Register
FMMCR	$1	Module Control Register
		Reserved
FMSECH	$3	Security High Half Register
FMSECL	$4	Security Low Half Register
		Reserved
		Reserved
FMPROT	$10	Protection Register (Banked)
FMPROTB	$11	Protection Boot Register (Banked)
		Reserved
FMUSTAT	$13	User Status Register (Banked)
FMCMD	$14	Command Register (Banked)
		Reserved
		Reserved
FMOPT 0	$1A	16-Bit Information Option Register 0 Hot temperature ADC reading of Temperature Sensor; value set during factory test
FMOPT 1	$1B	16-Bit Information Option Register 1 Not used
FMOPT 2	$1C	16-Bit Information Option Register 2 Room temperature ADC reading of Temperature Sensor; value set during factory test

Add. Offset	Register Name		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
$0	IPR0	R	0	0	BKPT_U0 IPL		STPCNT IPL		0	0	0	0	0	0	0	0	0	0
		W																
$1	IPR1	R	0	0	0	0	0	0	0	0	0	0	RX_REG IPL		TX_REG IPL		TRBUF IPL	
		W																
$2	IPR2	R	FMCBE IPL		FMCC IPL		FMERR IPL		LOCK IPL		LVI IPL		0	0	IRQB IPL		IRQA IPL	
		W																
$3	IPR3	R	GPIOD IPL		GPIOE IPL		GPIOF IPL		FCMSGBUF IPL		FCWKUP IPL		FCERR IPL		FCBOFF IPL		0	0
		W																
$4	IPR4	R	SPI0_RCV IPL		SPI1_XMIT IPL		SPI1_RCV IPL		0	0	0	0	GPIOA IPL		GPIOB IPL		GPIOC IPL	
		W																
$5	IPR5	R	DEC1_XIRQ IPL		DEC1_HIRQ IPL		SCI1_RCV IPL		SCI1_RERR IPL		0	0	SCI1_TIDL IPL		SCI1_XMIT IPL		SPI0_XMIT IPL	
		W																
$6	IPR6	R	TMRC0 IPL		TMRD3 IPL		TMRD2 IPL		TMRD1 IPL		TMRD0 IPL		0	0	DEC0_XIRQ IPL		DEC0_HIRQ IPL	
		W																
$7	IPR7	R	TMRA0 IPL		TMRB3 IPL		TMRB2 IPL		TMRB1 IPL		TMRB0 IPL		TMRC3 IPL		TMRC2 IPL		TMRC1 IPL	
		W																
$8	IPR8	R	SCI0_RCV IPL		SCI0_RERR IPL		0	0	SCI0_TIDL IPL		SCI0_XMIT IPL		TMRA3 IPL		TMRA2 IPL		TMRA1 IPL	
		W																
$9	IPR9	R	PWMA_F IPL		PWMB_F IPL		PWMA_RL IPL		PWMB_RL IPL		ADCA_ZC IPL		ABCB_ZC IPL		ADCA_CC IPL		ADCB_CC IPL	
		W																
$A	VBA	R	0	0	0	VECTOR BASE ADDRESS												
		W																
$B	FIM0	R	0	0	0	0	0	0	0	0	0	FAST INTERRUPT 0						
		W																
$C	FIVAL0	R	FAST INTERRUPT 0 VECTOR ADDRESS LOW															
		W																
$D	FIVAH0	R	0	0	0	0	0	0	0	0	0	0	0	FAST INTERRUPT 0 VECTOR ADDRESS HIGH				
		W																
$E	FIM1	R	0	0	0	0	0	0	0	0	0	FAST INTERRUPT 1						
		W																
$F	FIVAL1	R	FAST INTERRUPT 1 VECTOR ADDRESS LOW															
		W																
$10	FIVAH1	R	0	0	0	0	0	0	0	0	0	0	0	FAST INTERRUPT 1 VECTOR ADDRESS HIGH				
		W	0	0	0	0	0	0	0	0	0	0	0					
$11	IRQP0	R	PENDING [16:2]															1
		W																
$12	IRQP1	R	PENDING [32:17]															
		W																
$13	IRQP2	R	PENDING [48:33]															
		W																
$14	IRQP3	R	PENDING [64:49]															
		W																
$15	IRQP4	R	PENDING [80:65]															
		W																
$16	IRQP5	R	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	PEND-ING [81]
		W																
	Reserved																	
$1D	ICTL	R	INT	IPIC			VAB						INT_DIS	1	$\overline{\text{IRQB}}$ STATE	$\overline{\text{IRQA}}$ STATE	$\overline{\text{IRQB}}$ EDG	$\overline{\text{IRQA}}$ EDG
		W																

= Reserved

set the bit, while writing a 1 to the bit will clear it.

6.5.2.4 External Reset (EXTR)—Bit 3

If 1, the EXTR bit indicates an external system reset has occurred. This bit will be cleared by a Power-On Reset or by software. Writing a 0 to this bit position will set the bit, while writing a 1 to the bit position will clear it. Basically, when the EXTR bit is 1, the previous system reset was caused by the external $\overline{\text{RESET}}$ pin being asserted low.

6.5.2.5 Power-On Reset (POR)—Bit 2

When 1, the POR bit indicates a Power-On Reset occurred some time in the past. This bit can be cleared only by software or by another type of reset. Writing a 0 to this bit will set the bit, while writing a 1 to the bit position will clear the bit. In summary, if the bit is 1, the previous system reset was due to a Power-On Reset.

6.5.2.6 Reserved—Bits 1–0

This bit field is reserved or not implemented. It is read as 0 and cannot be modified by writing.

6.5.3 SIM Software Control Registers (SIM_SCR0, SIM_SCR1, SIM_SCR2, and SIM_SCR3)

Only SIM_SCR0 is shown in this section. SIM_SCR1, SIM_SCR2, and SIM_SCR3 are identical in functionality.

Base + $2	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read	FIELD															
Write																
POR	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 6-5 SIM Software Control Register 0 (SIM_SCR0)

6.5.3.1 Software Control Data 1 (FIELD)—Bits 15–0

This register is reset only by the Power-On Reset (POR). It has no part-specific functionality and is intended for use by a software developer to contain data that will be unaffected by the other reset sources ($\overline{\text{RESET}}$ pin, software reset, and COP reset).

6.5.4 Most Significant Half of JTAG ID (SIM_MSH_ID)

This read-only register displays the most significant half of the JTAG ID for the chip. This register reads $11F4.

6.5.6.2 PWMA1—Bit 14
This bit controls the pull-up resistors on the FAULTA3 pin.

6.5.6.3 CAN—Bit 13
This bit controls the pull-up resistors on the CAN_RX pin.

6.5.6.4 EMI_MODE—Bit 12
This bit controls the pull-up resistors on the EMI_MODE pin.

Note: In this package, this input pin is double-bonded with the adjacent V_{SS} pin and this bit should be changed to a 1 in order to reduce power consumption.

6.5.6.5 $\overline{\text{RESET}}$—Bit 11
This bit controls the pull-up resistors on the $\overline{\text{RESET}}$ pin.

6.5.6.6 IRQ—Bit 10
This bit controls the pull-up resistors on the $\overline{\text{IRQA}}$ and $\overline{\text{IRQB}}$ pins.

6.5.6.7 XBOOT—Bit 9
This bit controls the pull-up resistors on the EXTBOOT pin.

Note: In this package, this input pin is double-bonded with the adjacent V_{SS} pin and this bit should be changed to a 1 in order to reduce power consumption.

6.5.6.8 PWMB—Bit 8
This bit controls the pull-up resistors on the FAULTB0, FAULTB1, FAULTB2, and FAULTB3 pins.

6.5.6.9 PWMA0—Bit 7
This bit controls the pull-up resistors on the FAULTA0, FAULTA1, and FAULTA2 pins.

6.5.6.10 Reserved—Bit 6
This bit field is reserved or not implemented. It is read as 0 and cannot be modified by writing.

6.5.6.11 CTRL—Bit 5
This bit controls the pull-up resistors on the $\overline{\text{WR}}$ and $\overline{\text{RD}}$ pins.

6.5.6.12 Reserved—Bit 4
This bit field is reserved or not implemented. It is read as 0 and cannot be modified by writing.

6.5.6.13 JTAG—Bit 3
This bit controls the pull-up resistors on the $\overline{\text{TRST}}$, TMS and TDI pins.

Table 6-3 Clock Operation in Power-Down Modes

Mode	Core Clocks	Peripheral Clocks	Description
Run	Active	Active	Device is fully functional
Wait	Core and memory clocks disabled	Active	Peripherals are active and can produce interrupts if they have not been masked off. Interrupts will cause the core to come out of its suspended state and resume normal operation. Typically used for power-conscious applications.
Stop	System clocks continue to be generated in the SIM, but most are gated prior to reaching memory, core and peripherals.		The only possible recoveries from Stop mode are: 1. CAN traffic (1st message will be lost) 2. Non-clocked interrupts 3. COP reset 4. External reset 5. Power-on reset

All peripherals, except the COP/watchdog timer, run off the IPBus clock frequency, which is the same as the main processor frequency in this architecture. The maximum frequency of operation is SYS_CLK = 60MHz.

6.8 Stop and Wait Mode Disable Function

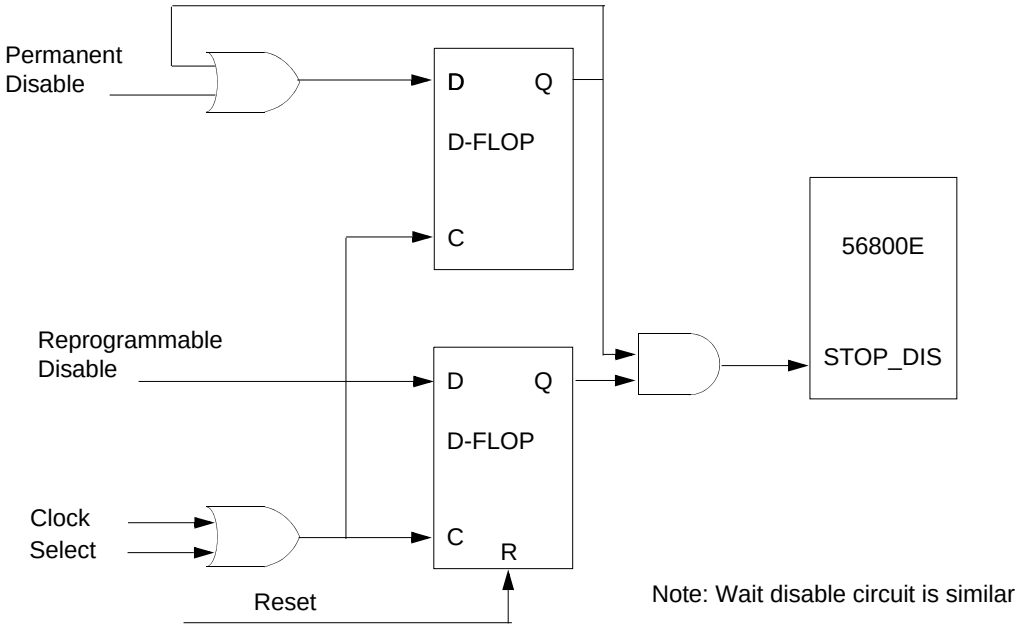


Figure 6-16 Internal Stop Disable Circuit

The 56800E core contains both STOP and WAIT instructions. Both put the CPU to sleep. For lowest power consumption in Stop mode, the PLL can be shut down. This must be done explicitly before entering Stop mode, since there is no automatic mechanism for this. When the PLL is shut down, the 56800E system clock must be set equal to the oscillator output.

Some applications require the 56800E STOP and WAIT instructions to be disabled. To disable those instructions, write to the SIM control register (SIM_CONTROL), described in **Part 6.5.1**. This procedure can be on either a permanent or temporary basis. Permanently assigned applications last only until their next reset.

6.9 Resets

The SIM supports four sources of reset. The two asynchronous sources are the external $\overline{\text{RESET}}$ pin and the Power-On Reset (POR). The two synchronous sources are the software reset, which is generated within the SIM itself by writing to the SIM_CONTROL register, and the COP reset.

Reset begins with the assertion of any of the reset sources. Release of reset to various blocks is sequenced to permit proper operation of the device. A POR reset is first extended for 2^{21} clock cycles to permit stabilization of the clock source, followed by a 32 clock window in which SIM clocking is initiated. It is then followed by a 32 clock window in which peripherals are released to implement Flash security, and, finally, followed by a 32 clock window in which the core is initialized. After completion of the described reset sequence, application code will begin execution.

Resets may be asserted asynchronously, but are always released internally on a rising edge of the system clock.

Part 7 Security Features

The 56F8345/56F8145 offer security features intended to prevent unauthorized users from reading the contents of the Flash Memory (FM) array. The Flash security consists of several hardware interlocks that block the means by which an unauthorized user could gain access to the Flash array.

However, part of the security must lie with the user's code. An extreme example would be user's code that dumps the contents of the internal program, as this code would defeat the purpose of security. At the same time, the user may also wish to put a "backdoor" in his program. As an example, the user downloads a security key through the SCI, allowing access to a programming routine that updates parameters stored in another section of the Flash.

7.1 Operation with Security Enabled

Once the user has programmed the Flash with his application code, the device can be secured by programming the security bytes located in the FM configuration field, which occupies a portion of the FM array. These non-volatile bytes will keep the part secured through reset and through power-down of the device. Only two bytes within this field are used to enable or disable security. Refer to the Flash Memory section in the **56F8300 Peripheral User Manual** for the state of the security bytes and the resulting state of security. When Flash security mode is enabled in accordance with the method described in the Flash Memory module specification, the device will disable the core EOnCE debug capabilities. Normal program execution is otherwise unaffected.

The LOCKOUT_RECOVERY instruction has an associated 7-bit Data Register (DR) that is used to control the clock divider circuit within the FM module. This divider, FM_CLKDIV[6:0], is used to control the period of the clock used for timed events in the FM erase algorithm. This register must be set with appropriate values before the lockout sequence can begin. Refer to the JTAG section of the **56F8300 Peripheral User Manual** for more details on setting this register value.

The value of the JTAG FM_CLKDIV[6:0] will replace the value of the FM register FMCLKD that divides down the system clock for timed events, as illustrated in **Figure 7-1**. FM_CLKDIV[6] will map to the PRDIV8 bit, and FM_CLKDIV[5:0] will map to the DIV[5:0] bits. The combination of PRDIV8 and DIV must divide the FM input clock down to a frequency of 150kHz-200kHz. The **"Writing the FMCLKD Register**" section in the Flash Memory chapter of the **56F8300 Peripheral User Manual** gives specific equations for calculating the correct values.

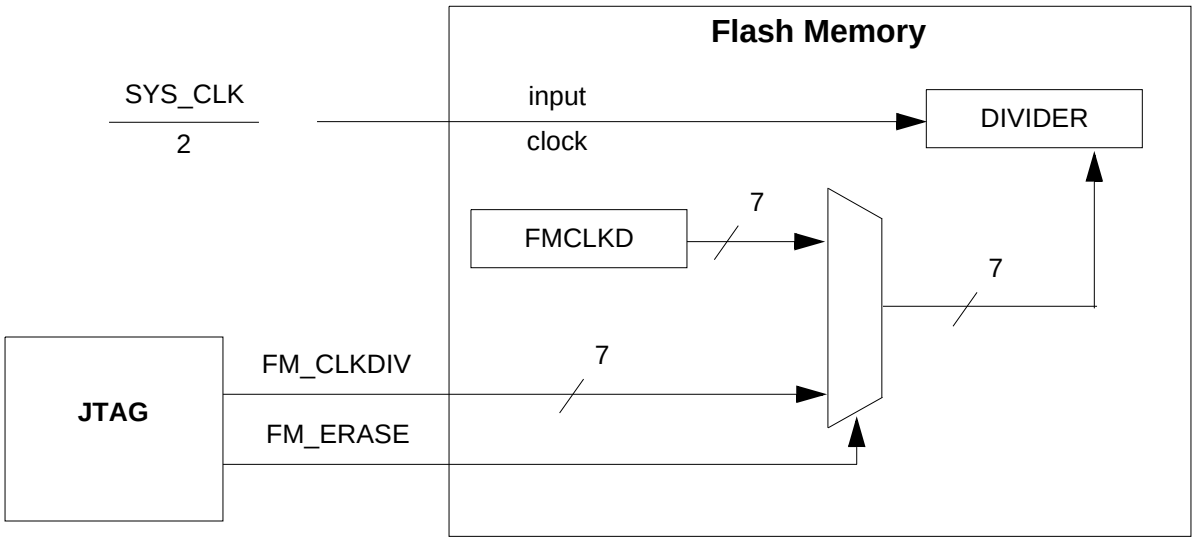


Figure 7-1 JTAG to FM Connection for Lockout Recovery

Two examples of FM_CLKDIV calculations follow.

the backdoor key access. The customer would need to supply Technical Support with the backdoor key and the protocol to access the backdoor routine in the Flash. Additionally, the KEYEN bit that allows backdoor key access must be set.

An alternative method for performing analysis on a secured hybrid controller would be to mass-erase and reprogram the Flash with the original code, but to modify the security bytes.

To insure that a customer does not inadvertently lock himself out of the device during programming, it is recommended that he program the backdoor access key first, his application code second, and the security bytes within the FM configuration field last.

Part 8 General Purpose Input/Output (GPIO)

8.1 Introduction

This section is intended to supplement the GPIO information found in the **56F8300 Peripheral User Manual** and contains only chip-specific information. This information supercedes the generic information in the **56F8300 Peripheral User Manual**.

8.2 Memory Maps

The width of the GPIO port defines how many bits are implemented in each of the GPIO registers. Based on this and the default function of each of the GPIO pins, the reset values of the GPIOx_PUR and GPIOx_PER registers change from port to port. Tables **4-29** through **4-34** define the actual reset values of these registers.

8.3 Configuration

There are six GPIO ports defined on the 56F8345/56F8145. The width of each port and the associated peripheral function is shown in **Table 8-1** and **Table 8-2**. The specific mapping of GPIO port pins is shown in **Table 8-3**.

Table 8-1 56F8345 GPIO Ports Configuration

GPIO Port	Port Width	Available Pins in 56F8345	Peripheral Function	Reset Function
A	14	6	6 pins - EMI Address pins - Can only be used as GPIO 8 pins - EMI Address pins - Not available in this package	EMI Address N/A
B	8	5	5 pins - EMI Address pins - Can only be used as GPIO 3 pins - EMI Address pins - Not available in this package	GPIO N/A

Table 8-3 GPIO External Signals Map (Continued)

Pins in shaded rows are not available in 56F8345 / 56F8145

Pins in italics are NOT available in the 56F8145 device

GPIO Port	GPIO Bit	Reset Function	Functional Signal	Package Pin #
GPIOE	0	Peripheral	TXD0	7
	1	Peripheral	RXD0	8
	2	N/A		
	3	N/A		
	4	Peripheral	SCLK0	124
	5	Peripheral	MOSI0	126
	6	Peripheral	MISO0	125
	7	Peripheral	$\overline{\text{SS0}}$	123
	8	Peripheral	TC0	111
	9	Peripheral	TC1	113
	10	Peripheral	*TD0*	107
	11	Peripheral	*TD1*	108
	12	Peripheral	*TD2*	109
	13	Peripheral	*TD3*	110

Table 10-2 56F8345/56F8145 ElectroStatic Discharge (ESD) Protection

Characteristic	Min	Typ	Max	Unit
ESD for Human Body Model (HBM)	2000	—	—	V
ESD for Machine Model (MM)	200	—	—	V
ESD for Charge Device Model (CDM)	500	—	—	V

Table 10-3 Thermal Characteristics[6]

Characteristic	Comments	Symbol	Value	Unit	Notes
			128-pin LQFP		
Junction to ambient Natural convection		$R_{\theta JA}$	50.8	°C/W	2
Junction to ambient (@1m/sec)		$R_{\theta JMA}$	46.5	°C/W	2
Junction to ambient Natural convection	Four layer board (2s2p)	$R_{\theta JMA}$ (2s2p)	43.9	°C/W	1,2
Junction to ambient (@1m/sec)	Four layer board (2s2p)	$R_{\theta JMA}$	41.7	°C/W	1,2
Junction to case		$R_{\theta JC}$	13.9	°C/W	3
Junction to center of case		Ψ_{JT}	1.2	°C/W	4, 5
I/O pin power dissipation		$P_{I/O}$	User-determined	W	
Power dissipation		P_D	$P_D = (I_{DD} \times V_{DD} + P_{I/O})$	W	
Maximum allowed P_D		P_{DMAX}	$(TJ - TA) / R\theta JA$[7]	W	

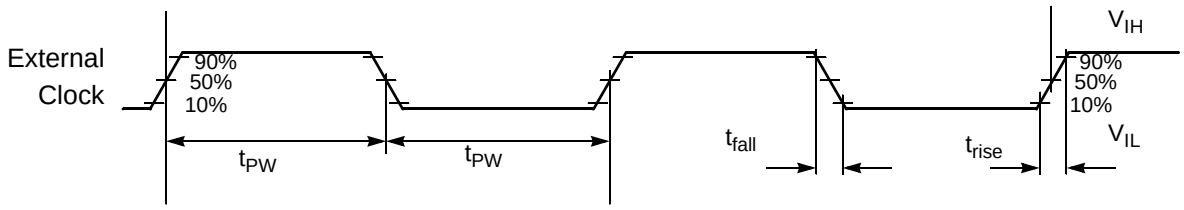
1. Theta-JA determined on 2s2p test boards is frequently lower than would be observed in an application. Determined on 2s2p thermal test board.
2. Junction to ambient thermal resistance, Theta-JA ($R_{\theta JA}$) was simulated to be equivalent to the JEDEC specification JESD51-2 in a horizontal configuration in natural convection. Theta-JA was also simulated on a thermal test board with two internal planes (2s2p, where “s” is the number of signal layers and “p” is the number of planes) per JESD51-6 and JESD51-7. The correct name for Theta-JA for forced convection or with the non-single layer boards is Theta-JMA.
3. Junction to case thermal resistance, Theta-JC ($R_{\theta JC}$), was simulated to be equivalent to the measured values using the cold plate technique with the cold plate temperature used as the "case" temperature. The basic cold plate measurement technique is described by MIL-STD 883D, Method 1012.1. This is the correct thermal metric to use to calculate thermal performance when the package is being used with a heat sink.
4. Thermal Characterization Parameter, Psi-JT (Ψ_{JT}), is the "resistance" from junction to reference point thermocouple on top center of case as defined in JESD51-2. Ψ_{JT} is a useful value to use to estimate junction temperature in steady-state customer environments.
5. Junction temperature is a function of on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
6. See **Part 12.1** for more details on thermal design considerations.

10.5 External Clock Operation Timing

Table 10-13 External Clock Operation Timing Requirements[1]

Characteristic	Symbol	Min	Typ	Max	Unit
Frequency of operation (external clock driver)[2]	f_{osc}	0	—	120	MHz
Clock Pulse Width[3]	t_{PW}	3.0	—	—	ns
External clock input rise time[4]	t_{rise}	—	—	10	ns
External clock input fall time[5]	t_{fall}	—	—	10	ns

1. Parameters listed are guaranteed by design.
2. See **Figure 10-3** for details on using the recommended connection of an external clock driver.
3. The high or low pulse width must be no smaller than 8.0ns or the chip will not function.
4. External clock input rise time is measured from 10% to 90%.
5. External clock input fall time is measured from 90% to 10%.



Note: The midpoint is $V_{IL} + (V_{IH} – V_{IL})/2$.

Figure 10-3 External Clock Timing

10.6 Phase Locked Loop Timing

Table 10-14 PLL Timing

Characteristic	Symbol	Min	Typ	Max	Unit
External reference crystal frequency for the PLL[1]	f_{osc}	4	8	8.4	MHz
PLL output frequency[2] (f_{OUT})	f_{op}	160	—	260	MHz
PLL stabilization time[3] -40° to +125°C	t_{plls}	—	1	10	ms

1. An externally supplied reference clock should be as free as possible from any phase jitter for the PLL to work correctly. The PLL is optimized for 8MHz input crystal.
2. ZCLK may not exceed 60MHz. For additional information on ZCLK and (f_{OUT}/2), please refer to the OCCS chapter in the **56F8300 Peripheral User Manual**.

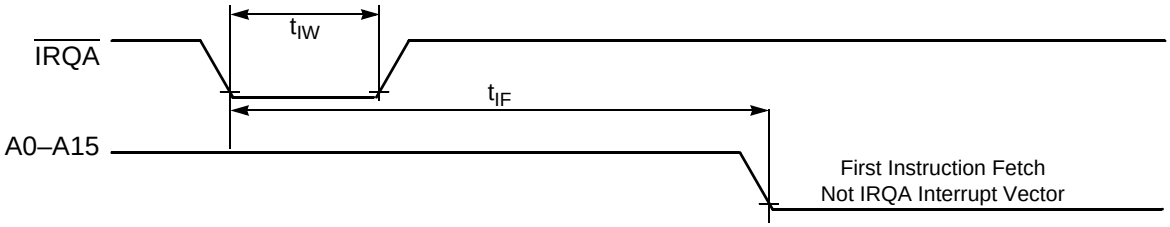


Figure 10-8 Recovery from Stop State Using Asynchronous Interrupt Timing

10.9 Serial Peripheral Interface (SPI) Timing

Table 10-17 SPI Timing[1]

Characteristic	Symbol	Min	Max	Unit	See Figure
Cycle time Master Slave	t_C	 50 50	 — —	 ns ns	10-9, 10-10, 10-11, 10-12
Enable lead time Master Slave	t_{ELD}	 — 25	 — —	 ns ns	10-12
Enable lag time Master Slave	t_{ELG}	 — 100	 — —	 ns ns	10-12
Clock (SCK) high time Master Slave	t_{CH}	 17.6 25	 — —	 ns ns	10-9, 10-10, 10-11, 10-12
Clock (SCK) low time Master Slave	t_{CL}	 24.1 25	 — —	 ns ns	10-12
Data set up time required for inputs Master Slave	t_{DS}	 20 0	 — —	 ns ns	10-9, 10-10, 10-11, 10-12
Data hold time required for inputs Master Slave	t_{DH}	 0 2	 — —	 ns ns	10-9, 10-10, 10-11, 10-12
Access time (time to data active from high-impedance state) Slave	t_A	4.8	15	ns	10-12
Disable time (hold time to high-impedance state) Slave	t_D	3.7	15.2	ns	10-12
Data Valid for outputs Master Slave (after enable edge)	t_{DV}	 — —	 4.5 20.4	 ns ns	10-9, 10-10, 10-11, 10-12

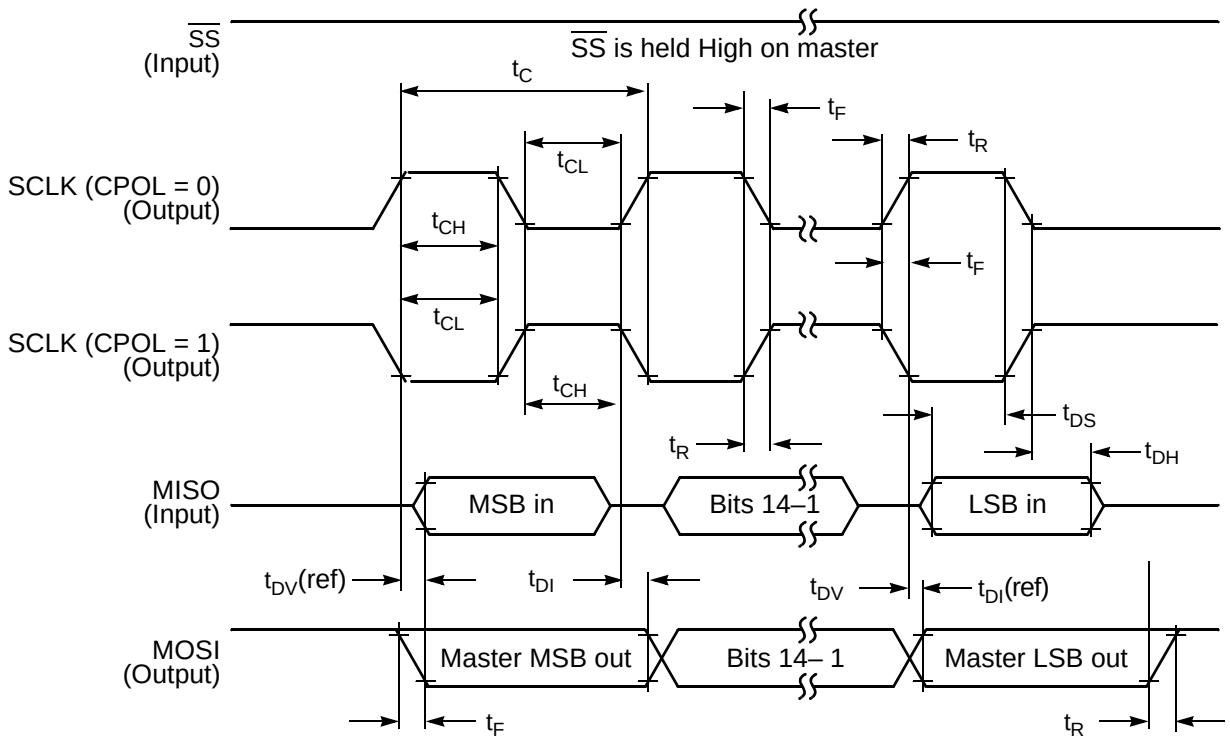


Figure 10-10 SPI Master Timing (CPHA = 1)

10.16 Equivalent Circuit for ADC Inputs

Figure 10-22 illustrates the ADC input circuit during sample and hold. S1 and S2 are always open/closed at the same time that S3 is closed/open. When S1/S2 are closed & S3 is open, one input of the sample and hold circuit moves to V_{REFH} - V_{REFH} / 2, while the other charges to the analog input voltage. When the switches are flipped, the charge on C1 and C2 are averaged via S3, with the result that a single-ended analog input is switched to a differential voltage centered about V_{REFH} - V_{REFH} / 2. The switches switch on every cycle of the ADC clock (open one-half ADC clock, closed one-half ADC clock). Note that there are additional capacitances associated with the analog input pad, routing, etc., but these do not filter into the S/H output voltage, as S1 provides isolation during the charge-sharing phase.

One aspect of this circuit is that there is an on-going input current, which is a function of the analog input voltage, V_{REF} and the ADC clock frequency.

The thermal characterization parameter is measured per JESD51-2 specification using a 40-gauge type T thermocouple epoxied to the top center of the package case. The thermocouple should be positioned so that the thermocouple junction rests on the package. A small amount of epoxy is placed over the thermocouple junction and over about 1mm of wire extending from the junction. The thermocouple wire is placed flat against the package case to avoid measurement errors caused by cooling effects of the thermocouple wire.

When heat sink is used, the junction temperature is determined from a thermocouple inserted at the interface between the case of the package and the interface material. A clearance slot or hole is normally required in the heat sink. Minimizing the size of the clearance is important to minimize the change in thermal performance caused by removing part of the thermal interface to the heat sink. Because of the experimental difficulties with this technique, many engineers measure the heat sink temperature and then back-calculate the case temperature using a separate measurement of the thermal resistance of the interface. From this case temperature, the junction temperature is determined from the junction-to-case thermal resistance.

12.2 Electrical Design Considerations

CAUTION

This device contains protective circuitry to guard against damage due to high static voltage or electrical fields. However, normal precautions are advised to avoid application of any voltages higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate voltage level.

Use the following list of considerations to assure correct operation of the 56F8345/56F8145:

- Provide a low-impedance path from the board power supply to each V_{DD} pin on the device, and from the board ground to each V_{SS} (GND) pin
- The minimum bypass requirement is to place six 0.01–0.1µF capacitors positioned as close as possible to the package supply pins. The recommended bypass configuration is to place one bypass capacitor on each of the V_{DD}/V_{SS} pairs, including V_{DDA}/V_{SSA}. Ceramic and tantalum capacitors tend to provide better performance tolerances.
- Ensure that capacitor leads and associated printed circuit traces that connect to the chip V_{DD} and V_{SS} (GND) pins are less than 0.5 inch per capacitor lead
- Use at least a four-layer Printed Circuit Board (PCB) with two inner layers for V_{DD} and V_{SS}
- Bypass the V_{DD} and V_{SS} layers of the PCB with approximately 100µF, preferably with a high-grade capacitor such as a tantalum capacitor

Part 13 Ordering Information

Table 13-1 lists the pertinent information needed to place an order. Consult a Freescale Semiconductor sales office or authorized distributor to determine availability and to order parts.

Table 13-1 Ordering Information

Part	Supply Voltage	Package Type	Pin Count	Frequency (MHz)	Ambient Temperature Range	Order Number
MC56F8345	3.0–3.6 V	Low-Profile Quad Flat Pack (LQFP)	128	60	-40° to + 105° C	MC56F8345VFG60
MC56F8345	3.0–3.6 V	Low-Profile Quad Flat Pack (LQFP)	128	60	-40° to + 125° C	MC56F8345MFG60
MC56F8145	3.0–3.6 V	Low-Profile Quad Flat Pack (LQFP)	128	40	-40° to + 105° C	MC56F8145VFG
MC56F8345	3.0–3.6 V	Low-Profile Quad Flat Pack (LQFP)	128	60	-40° to + 105° C	MC56F8345VFGE*
MC56F8345	3.0–3.6 V	Low-Profile Quad Flat Pack (LQFP)	128	60	-40° to + 125° C	MC56F8345MFGE*
MC56F8145	3.0–3.6 V	Low-Profile Quad Flat Pack (LQFP)	128	40	-40° to + 105° C	MC56F8145VFGE*

*This package is RoHS compliant.

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