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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	56800E
Core Size	16-Bit
Speed	60MHz
Connectivity	CANbus, EBI/EMI, SCI, SPI
Peripherals	POR, PWM, Temp Sensor, WDT
Number of I/O	49
Program Memory Size	128KB (64K x 16)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	6K x 16
Voltage - Supply (Vcc/Vdd)	2.25V ~ 3.6V
Data Converters	A/D 16x12b
Oscillator Type	External
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	128-LQFP
Supplier Device Package	128-LQFP (14x20)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mc56f8345mfge

Table 1-2 Bus Signal Names

Name	Function
Program Memory Interface	
pdb_m[15:0]	Program data bus for instruction word fetches or read operations.
cdbw[15:0]	Primary core data bus used for program memory writes. (Only these 16 bits of the cdbw[31:0] bus are used for writes to program memory.)
pab[20:0]	Program memory address bus. Data is returned on pdb_m bus.
Primary Data Memory Interface Bus	
cdbr_m[31:0]	Primary core data bus for memory reads. Addressed via xab1 bus.
cdbw[31:0]	Primary core data bus for memory writes. Addressed via xab1 bus.
xab1[23:0]	Primary data address bus. Capable of addressing bytes[1], words, and long data types. Data is written on cdbw and returned on cdbr_m. Also used to access memory-mapped I/O.
Secondary Data Memory Interface	
xdb2_m[15:0]	Secondary data bus used for secondary data address bus xab2 in the dual memory reads.
xab2[23:0]	Secondary data address bus used for the second of two simultaneous accesses. Capable of addressing only words. Data is returned on xdb2_m.
Peripheral Interface Bus	
IPBus [15:0]	Peripheral bus accesses all on-chip peripherals registers. This bus operates at the same clock rate as the Primary Data Memory and therefore generates no delays when accessing the processor. Write data is obtained from cdbw. Read data is provided to cdbr_m.

1. Byte accesses can only occur in the bottom half of the memory address space. The MSB of the address will be forced to 0.

Table 2-2 Signal and Package Information for the 128-Pin LQFP

Signal Name	Pin No.	Type	State During Reset	Signal Description
PHASEA1	9	Schmitt Input	Input, pull-up enabled	**Phase A1** — Quadrature Decoder 1, PHASEA input for decoder 1.
(*TB0*)		Schmitt Input/ Output		**TB0** — Timer B, Channel 0
(SCLK1)		Schmitt Input/ Output		**SPI 1 Serial Clock** — In the master mode, this pin serves as an output, clocking slaved listeners. In slave mode, this pin serves as the data clock input. To activate the SPI function, set the PHSA_ALT bit in the SIM_GPS register. For details, see **Part 6.5.8**.
(GPIOC0)		Schmitt Input/ Output		**Port C GPIO** — This GPIO pin can be individually programmed as an input or output pin. In the 56F8345, the default state after reset is PHASEA1. In the 56F8145, the default state is not one of the functions offered and must be reconfigured. To deactivate the internal pull-up resistor, clear bit 0 in the GPIOC_PUR register.
PHASEB1	10	Schmitt Input	Input, pull-up enabled	**Phase B1** — Quadrature Decoder 1, PHASEB input for decoder 1.
(*TB1*)		Schmitt Input/ Output		**TB1** — Timer B, Channel 1
(MOSI1)		Schmitt Input/ Output		**SPI 1 Master Out/Slave In** — This serial data pin is an output from a master device and an input to a slave device. The master device places data on the MOSI line a half-cycle before the clock edge the slave device uses to latch the data. To activate the SPI function, set the PHSB_ALT bit in the SIM_GPS register. For details, see **Part 6.5.8**.
(GPIOC1)		Schmitt Input/ Output		**Port C GPIO** — This GPIO pin can be individually programmed as an input or output pin. In the 56F8345, the default state after reset is PHASEB1. In the 56F8145, the default state is not one of the functions offered and must be reconfigured. To deactivate the internal pull-up resistor, clear bit 1 in the GPIOC_PUR register.

JMP instructions. All other entries must contain JSR instructions.

Note: *PWMA, FlexCAN, Quadrature Decoder 1, and Quad Timers B and D are NOT available on the 56F8145 device.*

Table 4-5 Interrupt Vector Table Contents[1]

Peripheral	Vector Number	Priority Level	Vector Base Address +	Interrupt Function
				Reserved for Reset Overlay[2]
				Reserved for COP Reset Overlay[2]
core	2	3	P:$04	Illegal Instruction
core	3	3	P:$06	SW Interrupt 3
core	4	3	P:$08	HW Stack Overflow
core	5	3	P:$0A	Misaligned Long Word Access
core	6	1-3	P:$0C	OnCE Step Counter
core	7	1-3	P:$0E	OnCE Breakpoint Unit 0
				Reserved
core	9	1-3	P:$12	OnCE Trace Buffer
core	10	1-3	P:$14	OnCE Transmit Register Empty
core	11	1-3	P:$16	OnCE Receive Register Full
				Reserved
core	14	2	P:$1C	SW Interrupt 2
core	15	1	P:$1E	SW Interrupt 1
core	16	0	P:$20	SW Interrupt 0
core	17	0-2	P:$22	IRQA
core	18	0-2	P:$24	IRQB
				Reserved
LVI	20	0-2	P:$28	Low Voltage Detector (power sense)
PLL	21	0-2	P:$2A	PLL
FM	22	0-2	P:$2C	FM Access Error Interrupt
FM	23	0-2	P:$2E	FM Command Complete
FM	24	0-2	P:$30	FM Command, data and address Buffers Empty
				Reserved
FLEXCAN	26	0-2	P:$34	FLEXCAN Bus Off
FLEXCAN	27	0-2	P:$36	FLEXCAN Error
FLEXCAN	28	0-2	P:$38	FLEXCAN Wake Up

Table 4-8 EOnCE Memory Map (Continued)

Address	Register Acronym	Register Name
		Reserved
X:$FF FF90	OBMSK (32 bits)	Breakpoint 1 Unit [0] Mask Register
X:$FF FF91	—	Breakpoint 1 Unit [0] Mask Register
X:$FF FF92	OBAR2 (32 bits)	Breakpoint 2 Unit [0] Address Register
X:$FF FF93	—	Breakpoint 2 Unit [0] Address Register
X:$FF FF94	OBAR1 (24 bits)	Breakpoint 1 Unit [0] Address Register
X:$FF FF95	—	Breakpoint 1 Unit [0] Address Register
X:$FF FF96	OBCR (24 bits)	Breakpoint Unit [0] Control Register
X:$FF FF97	—	Breakpoint Unit [0] Control Register
X:$FF FF98	OTB (21-24 bits/stage)	Trace Buffer Register Stages
X:$FF FF99	—	Trace Buffer Register Stages
X:$FF FF9A	OTBPR (8 bits)	Trace Buffer Pointer Register
X:$FF FF9B	OTBCR	Trace Buffer Control Register
X:$FF FF9C	OBASE (8 bits)	Peripheral Base Address Register
X:$FF FF9D	OSR	Status Register
X:$FF FF9E	OSCNTR (24 bits)	Instruction Step Counter
X:$FF FF9F	—	Instruction Step Counter
X:$FF FFA0	OCR (bits)	Control Register
		Reserved
X:$FF FFFC	OCLSR (8 bits)	Core Lock / Unlock Status Register
X:$FF FFFD	OTXRXSR (8 bits)	Transmit and Receive Status and Control Register
X:$FF FFFE	OTX / ORX (32 bits)	Transmit Register / Receive Register
X:$FF FFFF	OTX1 / ORX1	Transmit Register Upper Word Receive Register Upper Word

4.7 Peripheral Memory Mapped Registers

On-chip peripheral registers are part of the data memory map on the 56800E series. These locations may be accessed with the same addressing modes used for ordinary Data memory, except all peripheral registers should be read/written using word accesses only.

Table 4-9 summarizes base addresses for the set of peripherals on the 56F8345 and 56F8145 devices. Peripherals are listed in order of the base address.

The following tables list all of the peripheral registers required to control or access the peripherals.

Note: *Features in italics are NOT available in the 56F8145 device.*

Table 4-11 Quad Timer A Registers Address Map (Continued) (TMRA_BASE = $00 F040)

Register Acronym	Address Offset	Register Description
TMRA2_CMPLD2	$29	Comparator Load Register 2
TMRA2_COMSCR	$2A	Comparator Status and Control Register
		Reserved
TMRA3_CMP1	$30	Compare Register 1
TMRA3_CMP2	$31	Compare Register 2
TMRA3_CAP	$32	Capture Register
TMRA3_LOAD	$33	Load Register
TMRA3_HOLD	$34	Hold Register
TMRA3_CNTR	$35	Counter Register
TMRA3_CTRL	$36	Control Register
TMRA3_SCR	$37	Status and Control Register
TMRA3_CMPLD1	$38	Comparator Load Register 1
TMRA3_CMPLD2	$39	Comparator Load Register 2
TMRA3_COMSCR	$3A	Comparator Status and Control Register

Table 4-12 Quad Timer B Registers Address Map (TMRB_BASE = $00 F080)

Quad Timer B is NOT available in the 56F8145 device

Register Acronym	Address Offset	Register Description
TMRB0_CMP1	$0	Compare Register 1
TMRB0_CMP2	$1	Compare Register 2
TMRB0_CAP	$2	Capture Register
TMRB0_LOAD	$3	Load Register
TMRB0_HOLD	$4	Hold Register
TMRB0_CNTR	$5	Counter Register
TMRB0_CTRL	$6	Control Register
TMRB0_SCR	$7	Status and Control Register
TMRB0_CMPLD1	$8	Comparator Load Register 1
TMRB0_CMPLD2	$9	Comparator Load Register 2
TMRB0_COMSCR	$A	Comparator Status and Control Register
		Reserved
TMRB1_CMP1	$10	Compare Register 1

Table 4-20 Analog-to-Digital Converter Registers Address Map (ADCA_BASE = $00 F200)

Register Acronym	Address Offset	Register Description
ADCA_CR1	$0	Control Register 1
ADCA_CR2	$1	Control Register 2
ADCA_ZCC	$2	Zero Crossing Control Register
ADCA_LST 1	$3	Channel List Register 1
ADCA_LST 2	$4	Channel List Register 2
ADCA_SDIS	$5	Sample Disable Register
ADCA_STAT	$6	Status Register
ADCA_LSTAT	$7	Limit Status Register
ADCA_ZCSTAT	$8	Zero Crossing Status Register
ADCA_RSLT 0	$9	Result Register 0
ADCA_RSLT 1	$A	Result Register 1
ADCA_RSLT 2	$B	Result Register 2
ADCA_RSLT 3	$C	Result Register 3
ADCA_RSLT 4	$D	Result Register 4
ADCA_RSLT 5	$E	Result Register 5
ADCA_RSLT 6	$F	Result Register 6
ADCA_RSLT 7	$10	Result Register 7
ADCA_LLMT 0	$11	Low Limit Register 0
ADCA_LLMT 1	$12	Low Limit Register 1
ADCA_LLMT 2	$13	Low Limit Register 2
ADCA_LLMT 3	$14	Low Limit Register 3
ADCA_LLMT 4	$15	Low Limit Register 4
ADCA_LLMT 5	$16	Low Limit Register 5
ADCA_LLMT 6	$17	Low Limit Register 6
ADCA_LLMT 7	$18	Low Limit Register 7
ADCA_HLMT 0	$19	High Limit Register 0
ADCA_HLMT 1	$1A	High Limit Register 1
ADCA_HLMT 2	$1B	High Limit Register 2
ADCA_HLMT 3	$1C	High Limit Register 3
ADCA_HLMT 4	$1D	High Limit Register 4
ADCA_HLMT 5	$1E	High Limit Register 5
ADCA_HLMT 6	$1F	High Limit Register 6

Table 4-29 GPIOA Registers Address Map (Continued)
(GPIOA_BASE = $00 F2E0)

Register Acronym	Address Offset	Register Description	Reset Value
GPIOA_PPMODE	$9	Push-Pull Mode Register	0 x 3FFF
GPIOA_RAWDATA	$A	Raw Data Input Register	—

Table 4-30 GPIOB Registers Address Map
(GPIOB_BASE = $00 F300)

Register Acronym	Address Offset	Register Description	Reset Value
GPIOB_PUR	$0	Pull-up Enable Register	0 x 00FF
GPIOB_DR	$1	Data Register	0 x 0000
GPIOB_DDR	$2	Data Direction Register	0 x 0000
GPIOB_PER	$3	Peripheral Enable Register	0 x 0000
GPIOB_IAR	$4	Interrupt Assert Register	0 x 0000
GPIOB_IENR	$5	Interrupt Enable Register	0 x 0000
GPIOB_IPOLR	$6	Interrupt Polarity Register	0 x 0000
GPIOB_IPR	$7	Interrupt Pending Register	0 x 0000
GPIOB_IESR	$8	Interrupt Edge-Sensitive Register	0 x 0000
GPIOB_PPMODE	$9	Push-Pull Mode Register	0 x 00FF
GPIOB_RAWDATA	$A	Raw Data Input Register	—

Table 4-31 GPIOC Registers Address Map
(GPIOC_BASE = $00 F310)

Register Acronym	Address Offset	Register Description	Reset Value
GPIOC_PUR	$0	Pull-up Enable Register	0 x 07FF
GPIOC_DR	$1	Data Register	0 x 0000
GPIOC_DDR	$2	Data Direction Register	0 x 0000
GPIOC_PER	$3	Peripheral Enable Register	0 x 07FF
GPIOC_IAR	$4	Interrupt Assert Register	0 x 0000
GPIOC_IENR	$5	Interrupt Enable Register	0 x 0000
GPIOC_IPOLR	$6	Interrupt Polarity Register	0 x 0000
GPIOC_IPR	$7	Interrupt Pending Register	0 x 0000
GPIOC_IESR	$8	Interrupt Edge-Sensitive Register	0 x 0000
GPIOC_PPMODE	$9	Push-Pull Mode Register	0 x 07FF

5.6.7.1 Timer C, Channel 0 Interrupt Priority Level (TMRC0 IPL)—Bits 15–14

This field is used to set the interrupt priority level for IRQs. This IRQ is limited to priorities 0 through 2. They are disabled by default.

- 00 = IRQ disabled (default)
- 01 = IRQ is priority level 0
- 10 = IRQ is priority level 1
- 11 = IRQ is priority level 2

5.6.7.2 Timer D, Channel 3 Interrupt Priority Level (TMRD3 IPL)—Bits 13–12

This field is used to set the interrupt priority level for IRQs. This IRQ is limited to priorities 0 through 2. They are disabled by default.

- 00 = IRQ disabled (default)
- 01 = IRQ is priority level 0
- 10 = IRQ is priority level 1
- 11 = IRQ is priority level 2

5.6.7.3 Timer D, Channel 2 Interrupt Priority Level (TMRD2 IPL)—Bits 11–10

This field is used to set the interrupt priority level for IRQs. This IRQ is limited to priorities 0 through 2. They are disabled by default.

- 00 = IRQ disabled (default)
- 01 = IRQ is priority level 0
- 10 = IRQ is priority level 1
- 11 = IRQ is priority level 2

5.6.7.4 Timer D, Channel 1 Interrupt Priority Level (TMRD1 IPL)—Bits 9–8

This field is used to set the interrupt priority level for IRQs. This IRQ is limited to priorities 0 through 2. They are disabled by default.

- 00 = IRQ disabled (default)
- 01 = IRQ is priority level 0
- 10 = IRQ is priority level 1
- 11 = IRQ is priority level 2

5.6.7.5 Timer D, Channel 0 Interrupt Priority Level (TMRD0 IPL)—Bits 7–6

This field is used to set the interrupt priority level for IRQs. This IRQ is limited to priorities 0 through 2. They are disabled by default.

- 00 = IRQ disabled (default)
- 01 = IRQ is priority level 0
- 10 = IRQ is priority level 1
- 11 = IRQ is priority level 2

5.6.9.8 Timer A, Channel 1 Interrupt Priority Level (TMRA1 IPL)—Bits 1–0

This field is used to set the interrupt priority level for IRQs. This IRQ is limited to priorities 0 through 2. They are disabled by default.

- 00 = IRQ disabled (default)
- 01 = IRQ is priority level 0
- 10 = IRQ is priority level 1
- 11 = IRQ is priority level 2

5.6.10 Interrupt Priority Register 9 (IPR9)

Base + $9	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read	PWMA_F IPL		PWMB_F IPL		PWMA_RL IPL		PWMB_RL IPL		ADCA_ZC IPL		ABCB_ZC IPL		ADCA_CC IPL		ADCB_CC IPL	
Write																
RESET	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 5-12 Interrupt Priority Register 9 (IPR9)

5.6.10.1 PWM A Fault Interrupt Priority Level (PWMA_F IPL)—Bits 15–14

This field is used to set the interrupt priority level for IRQs. This IRQ is limited to priorities 0 through 2. They are disabled by default.

- 00 = IRQ disabled (default)
- 01 = IRQ is priority level 0
- 10 = IRQ is priority level 1
- 11 = IRQ is priority level 2

5.6.10.2 PWM B Fault Interrupt Priority Level (PWMB_F IPL)—Bits 13–12

This field is used to set the interrupt priority level for IRQs. This IRQ is limited to priorities 0 through 2. They are disabled by default.

- 00 = IRQ disabled (default)
- 01 = IRQ is priority level 0
- 10 = IRQ is priority level 1
- 11 = IRQ is priority level 2

6.5 Register Descriptions

Table 6-1 SIM Registers (SIM_BASE = $00 F350)

Address Offset	Address Acronym	Register Name	Section Location
Base + $0	SIM_CONTROL	Control Register	6.5.1
Base + $1	SIM_RSTSTS	Reset Status Register	6.5.2
Base + $2	SIM_SCR0	Software Control Register 0	6.5.3
Base + $3	SIM_SCR1	Software Control Register 1	6.5.3
Base + $4	SIM_SCR2	Software Control Register 2	6.5.3
Base + $5	SIM_SCR3	Software Control Register 3	6.5.3
Base + $6	SIM_MSH_ID	Most Significant Half of JTAG ID	6.5.4
Base + $7	SIM_LSH_ID	Least Significant Half of JTAG ID	6.5.5
Base + $8	SIM_PUDR	Pull-up Disable Register	6.5.6
		Reserved	
Base + $A	SIM_CLKOSR	CLKO Select Register	6.5.7
Base + $B	SIM_GPS	GPIO Peripheral Select Register	6.5.8
Base + $C	SIM_PCE	Peripheral Clock Enable Register	6.5.9
Base + $D	SIM_ISALH	I/O Short Address Location High Register	6.5.10
Base + $E	SIM_ISALL	I/O Short Address Location Low Register	6.5.10

6.5.9.7 Quad Timer D Enable (TMRD)—Bit 9

Each bit controls clocks to the indicated peripheral.

- 1 = Clocks are enabled
- 0 = The clock is not provided to the peripheral (the peripheral is disabled)

6.5.9.8 Quad Timer C Enable (TMRC)—Bit 8

Each bit controls clocks to the indicated peripheral.

- 1 = Clocks are enabled
- 0 = The clock is not provided to the peripheral (the peripheral is disabled)

6.5.9.9 Quad Timer B Enable (TMRB)—Bit 7

Each bit controls clocks to the indicated peripheral.

- 1 = Clocks are enabled
- 0 = The clock is not provided to the peripheral (the peripheral is disabled)

6.5.9.10 Quad Timer A Enable (TMRA)—Bit 6

Each bit controls clocks to the indicated peripheral.

- 1 = Clocks are enabled
- 0 = The clock is not provided to the peripheral (the peripheral is disabled)

6.5.9.11 Serial Communications Interface 1 Enable (SCI1)—Bit 5

Each bit controls clocks to the indicated peripheral.

- 1 = Clocks are enabled
- 0 = The clock is not provided to the peripheral (the peripheral is disabled)

6.5.9.12 Serial Communications Interface 0 Enable (SCI0)—Bit 4

Each bit controls clocks to the indicated peripheral.

- 1 = Clocks are enabled
- 0 = The clock is not provided to the peripheral (the peripheral is disabled)

6.5.9.13 Serial Peripheral Interface 1 Enable (SPI1)—Bit 3

Each bit controls clocks to the indicated peripheral.

- 1 = Clocks are enabled
- 0 = The clock is not provided to the peripheral (the peripheral is disabled)

6.5.9.14 Serial Peripheral Interface 0 Enable (SPI0)—Bit 2

Each bit controls clocks to the indicated peripheral.

- 1 = Clocks are enabled
- 0 = The clock is not provided to the peripheral (the peripheral is disabled)

The LOCKOUT_RECOVERY instruction has an associated 7-bit Data Register (DR) that is used to control the clock divider circuit within the FM module. This divider, FM_CLKDIV[6:0], is used to control the period of the clock used for timed events in the FM erase algorithm. This register must be set with appropriate values before the lockout sequence can begin. Refer to the JTAG section of the **56F8300 Peripheral User Manual** for more details on setting this register value.

The value of the JTAG FM_CLKDIV[6:0] will replace the value of the FM register FMCLKD that divides down the system clock for timed events, as illustrated in **Figure 7-1**. FM_CLKDIV[6] will map to the PRDIV8 bit, and FM_CLKDIV[5:0] will map to the DIV[5:0] bits. The combination of PRDIV8 and DIV must divide the FM input clock down to a frequency of 150kHz-200kHz. The **"Writing the FMCLKD Register**" section in the Flash Memory chapter of the **56F8300 Peripheral User Manual** gives specific equations for calculating the correct values.

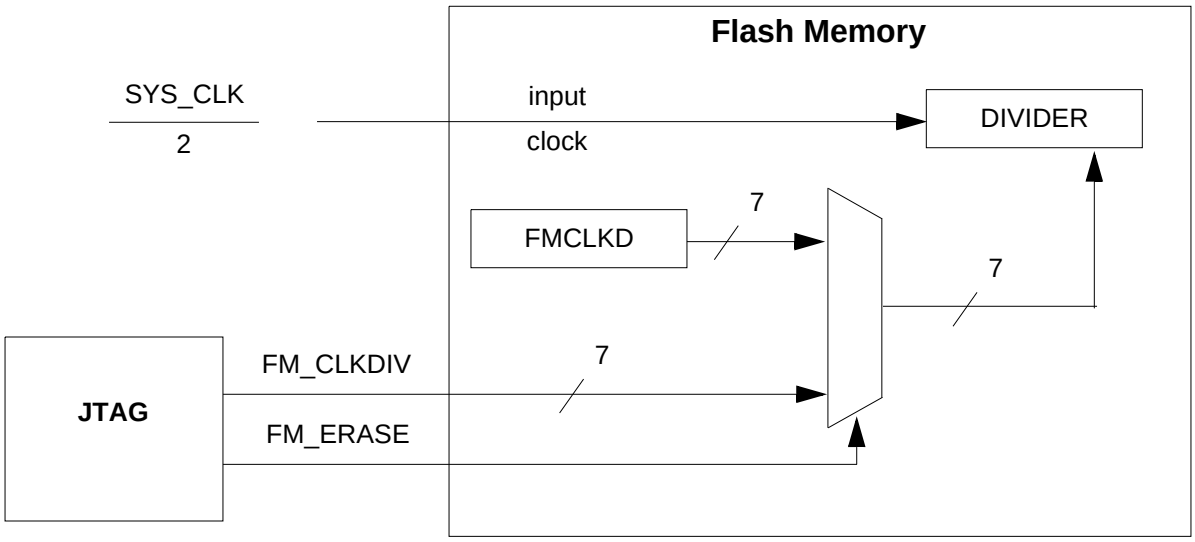


Figure 7-1 JTAG to FM Connection for Lockout Recovery

Two examples of FM_CLKDIV calculations follow.

Table 8-3 GPIO External Signals Map (Continued)

Pins in shaded rows are not available in 56F8345 / 56F8145

Pins in italics are NOT available in the 56F8145 device

GPIO Port	GPIO Bit	Reset Function	Functional Signal	Package Pin #
GPIOB	0	GPIO	A16[1]	27
	1	GPIO	A17[1]	28
	2	GPIO	A18[1]	29
	3	GPIO	A19[1]	30
	4	GPIO	A20 / Prescaler_clock	31
	5	N/A		
	6	N/A		
	7	N/A		
GPIOC	0	Peripheral	*PHASEA1* / *TB0* / SCLK1[2]	9
	1	Peripheral	*PHASEB1* / *TB1* / MOSI1[2]	10
	2	Peripheral	*INDEX1* / *TB2* / MISO1[2]	11
	3	Peripheral	*HOME1* / *TB3* / $\overline{\text{SS1}}$[2]	12
	4	Peripheral	PHASEA0 / TA0	127
	5	Peripheral	PHASEB0 / TA1	128
	6	Peripheral	INDEX0 / TA2	1
	7	Peripheral	HOME0 / TA3	2
	8	Peripheral	*ISA0*	104
	9	Peripheral	*ISA1*	105
	10	Peripheral	*ISA2*	106

7. TJ = Junction temperature
   TA = Ambient temperature

Note: *The 56F8145 device is guaranteed to 40MHz and specified to meet Industrial requirements only; CAN is NOT available on the 56F8145 device.*

Table 10-4 Recommended Operating Conditions

(V_{REFLO} = 0V, V_{SS} = V_{SSA_ADC} = 0V, V_{DDA} = V_{DDA_ADC} = $V_{DDA\_OSC\_PLL}$)

Characteristic	Symbol	Notes	Min	Typ	Max	Unit
Supply voltage	V_{DD_IO}		3	3.3	3.6	V
ADC Supply Voltage	V_{DDA_ADC}, V_{REFH}	V_{REFH} must be less than or equal to V_{DDA_ADC}	3	3.3	3.6	V
Oscillator / PLL Supply Voltage	$V_{DDA\_OSC\_PLL}$		3	3.3	3.6	V
Internal Logic Core Supply Voltage	V_{DD_CORE}	OCR_DIS is High	2.25	2.5	2.75	V
Device Clock Frequency	FSYSCLK		0	—	60	MHz
Input High Voltage (digital)	V_{IN}	Pin Groups 1, 2, 5, 6, 9, 10	2	—	5.5	V
Input High Voltage (analog)	V_{IHA}	Pin Group 13	2	—	V_{DDA}+0.3	V
Input High Voltage (XTAL/EXTAL, XTAL is not driven by an external clock)	V_{IHC}	Pin Group 11	V_{DDA}-0.8	—	V_{DDA}+0.3	V
Input high voltage (XTAL/EXTAL, XTAL is driven by an external clock)	V_{IHC}	Pin Group 11	2	—	V_{DDA}+0.3	V
Input Low Voltage	V_{IL}	Pin Groups 1, 2, 5, 6, 9, 10, 11, 13	-0.3	—	.8	V
Output High Source Current V_{OH} = 2.4V (V_{OH} min.)	I_{OH}	Pin Groups 1, 2, 3	—	—	-4	mA
		Pin Groups 5, 6, 7	—	—	-8	
		Pin Groups 8	—	—	-12	
Output Low Sink Current V_{OL} = 0.4V (V_{OL} max)	I_{OL}	Pin Groups 1, 2, 3, 4	—	—	4	mA
		Pin Groups 5, 6, 7	—	—	8	
		Pin Group 8	—	—	12	
Ambient Operating Temperature (Automotive)	T_A		-40	—	125	°C
Ambient Operating Temperature (Industrial)	T_A		-40	—	105	°C
Flash Endurance (Automotive) (Program Erase Cycles)	N_F	T_A = -40°C to 125°C	10,000	—	—	Cycles
Flash Endurance (Industrial) (Program Erase Cycles)	N_F	T_A = -40°C to 105°C	10,000	—	—	Cycles
Flash Data Retention (Automotive)	T_R	T_J <= 85°C avg	15	—	—	Years

Note: Total chip source or sink current cannot exceed 200mA
See Pin Groups listed in **Table 10-1**

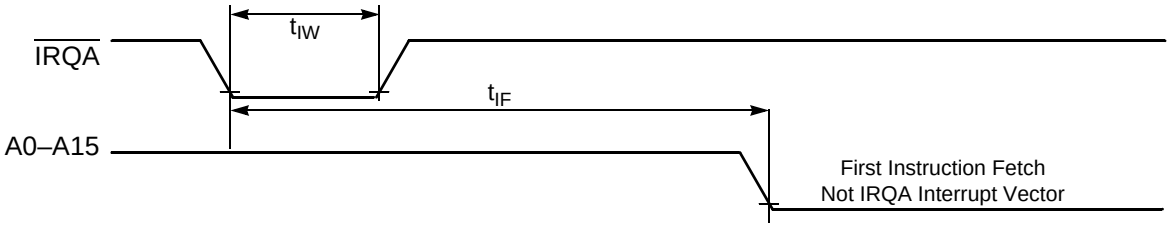


Figure 10-8 Recovery from Stop State Using Asynchronous Interrupt Timing

10.9 Serial Peripheral Interface (SPI) Timing

Table 10-17 SPI Timing[1]

Characteristic	Symbol	Min	Max	Unit	See Figure
Cycle time Master Slave	t_C	 50 50	 — —	 ns ns	10-9, 10-10, 10-11, 10-12
Enable lead time Master Slave	t_{ELD}	 — 25	 — —	 ns ns	10-12
Enable lag time Master Slave	t_{ELG}	 — 100	 — —	 ns ns	10-12
Clock (SCK) high time Master Slave	t_{CH}	 17.6 25	 — —	 ns ns	10-9, 10-10, 10-11, 10-12
Clock (SCK) low time Master Slave	t_{CL}	 24.1 25	 — —	 ns ns	10-12
Data set up time required for inputs Master Slave	t_{DS}	 20 0	 — —	 ns ns	10-9, 10-10, 10-11, 10-12
Data hold time required for inputs Master Slave	t_{DH}	 0 2	 — —	 ns ns	10-9, 10-10, 10-11, 10-12
Access time (time to data active from high-impedance state) Slave	t_A	4.8	15	ns	10-12
Disable time (hold time to high-impedance state) Slave	t_D	3.7	15.2	ns	10-12
Data Valid for outputs Master Slave (after enable edge)	t_{DV}	 — —	 4.5 20.4	 ns ns	10-9, 10-10, 10-11, 10-12

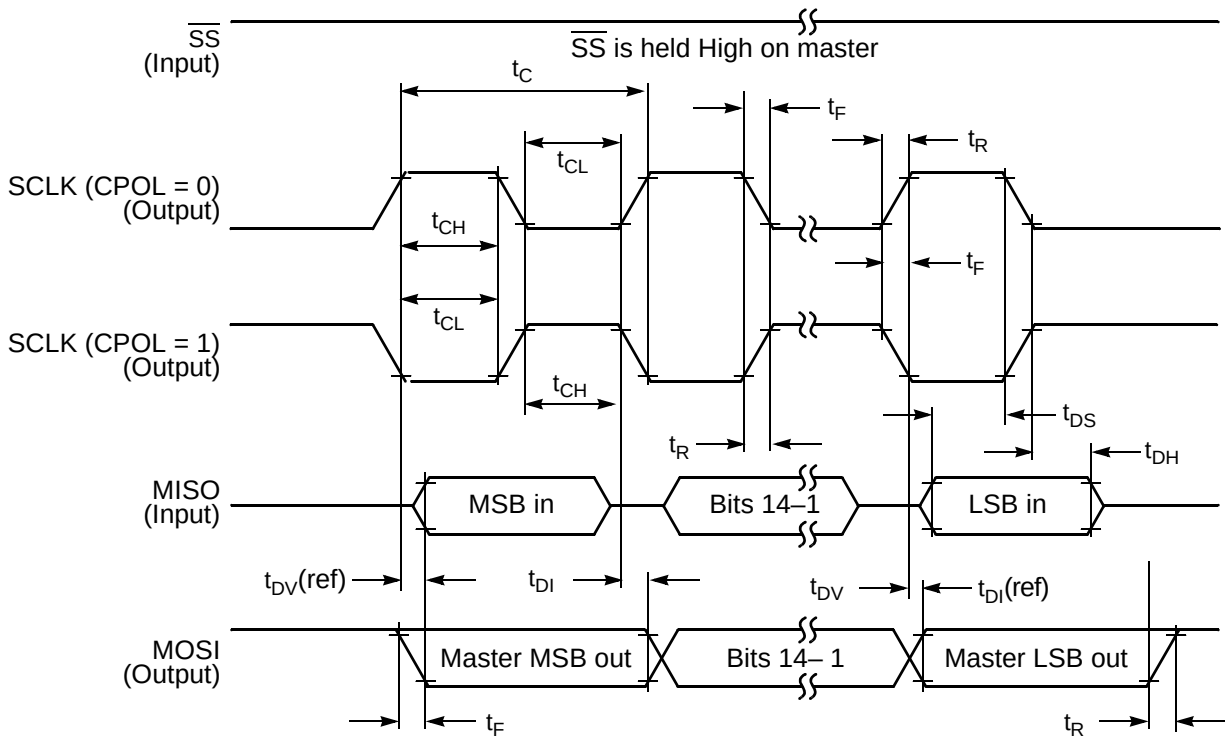
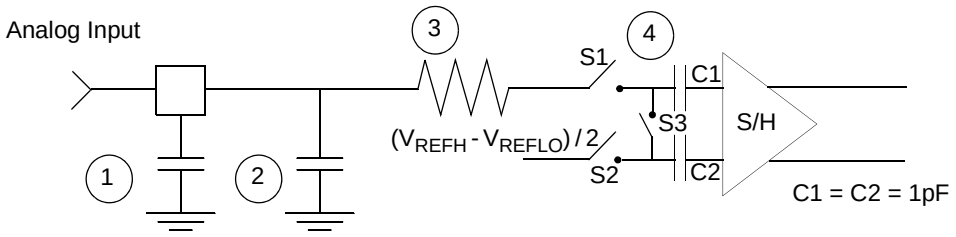


Figure 10-10 SPI Master Timing (CPHA = 1)

Table 10-23 ADC Parameters (Continued)

Characteristic	Symbol	Min	Typ	Max	Unit
Uncalibrated Offset Voltage	V_{OFFSET}	—	+/- 18	+/- 46	mV
Calibrated Absolute Error[6]	AE_{CAL}	—	See **Figure 10-21**	—	LSBs
Calibration Factor 1[7]	CF1	—	-0.003141	—	—
Calibration Factor 2[7]	CF2	—	-17.6	—	—
Crosstalk between channels	—	—	-60	—	dB
Common Mode Voltage	V_{common}	—	$(V_{REFH} - V_{REFLO}) / 2$	—	V
Signal-to-noise ratio	SNR	—	64.6	—	db
Signal-to-noise plus distortion ratio	SINAD	—	59.1	—	db
Total Harmonic Distortion	THD	—	60.6	—	db
Spurious Free Dynamic Range	SFDR	—	61.1	—	db
Effective Number Of Bits[8]	ENOB	—	9.6	—	Bits

1. INL measured from $V_{in} = .1V_{REFH}$ to $V_{in} = .9V_{REFH}$
   10% to 90% Input Signal Range
2. LSB = Least Significant Bit
3. ADC clock cycles
4. Assumes each voltage reference pin is bypassed with 0.1μF ceramic capacitors to ground
5. The current that can be injected or sourced from an unselected ADC signal input without impacting the performance of the ADC. This allows the ADC to operate in noisy industrial environments where inductive flyback is possible.
6. Absolute error includes the effects of both gain error and offset error.
7. Please see the **56F8300 Peripheral User's Manual** for additional information on ADC calibration.
8. ENOB = (SINAD - 1.76)/6.02



1. Parasitic capacitance due to package, pin-to-pin and pin-to-package base coupling; 1.8pf
2. Parasitic capacitance due to the chip bond pad, ESD protection devices and signal routing; 2.04pf
3. Equivalent resistance for the ESD isolation resistor and the channel select mux; 500 ohms
4. Sampling capacitor at the sample and hold circuit. Capacitor C1 is normally disconnected from the input and is only connected to it at sampling time; 1pf

Figure 10-22 Equivalent Circuit for A/D Loading

10.17 Power Consumption

This section provides additional detail which can be used to optimize power consumption for a given application.

Power consumption is given by the following equation:

Total power = A: internal [static component]
+B: internal [state-dependent component]
+C: internal [dynamic component]
+D: external [dynamic component]
+E: external [static]

A, the internal [static component], is comprised of the DC bias currents for the oscillator, leakage current, PLL, and voltage references. These sources operate independently of processor state or operating frequency.

B, the internal [state-dependent component], reflects the supply current required by certain on-chip resources only when those resources are in use. These include RAM, Flash memory and the ADCs.

C, the internal [dynamic component], is classic $C*V^2*F$ CMOS power dissipation corresponding to the 56800E core and standard cell logic.

D, the external [dynamic component], reflects power dissipated on-chip as a result of capacitive loading on the external pins of the chip. This is also commonly described as $C*V^2*F$, although simulations on two of the IO cell types used on the device reveal that the power-versus-load curve does have a non-zero Y-intercept.

The thermal characterization parameter is measured per JESD51-2 specification using a 40-gauge type T thermocouple epoxied to the top center of the package case. The thermocouple should be positioned so that the thermocouple junction rests on the package. A small amount of epoxy is placed over the thermocouple junction and over about 1mm of wire extending from the junction. The thermocouple wire is placed flat against the package case to avoid measurement errors caused by cooling effects of the thermocouple wire.

When heat sink is used, the junction temperature is determined from a thermocouple inserted at the interface between the case of the package and the interface material. A clearance slot or hole is normally required in the heat sink. Minimizing the size of the clearance is important to minimize the change in thermal performance caused by removing part of the thermal interface to the heat sink. Because of the experimental difficulties with this technique, many engineers measure the heat sink temperature and then back-calculate the case temperature using a separate measurement of the thermal resistance of the interface. From this case temperature, the junction temperature is determined from the junction-to-case thermal resistance.

12.2 Electrical Design Considerations

CAUTION

This device contains protective circuitry to guard against damage due to high static voltage or electrical fields. However, normal precautions are advised to avoid application of any voltages higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate voltage level.

Use the following list of considerations to assure correct operation of the 56F8345/56F8145:

- Provide a low-impedance path from the board power supply to each V_{DD} pin on the device, and from the board ground to each V_{SS} (GND) pin
- The minimum bypass requirement is to place six 0.01–0.1µF capacitors positioned as close as possible to the package supply pins. The recommended bypass configuration is to place one bypass capacitor on each of the V_{DD}/V_{SS} pairs, including V_{DDA}/V_{SSA}. Ceramic and tantalum capacitors tend to provide better performance tolerances.
- Ensure that capacitor leads and associated printed circuit traces that connect to the chip V_{DD} and V_{SS} (GND) pins are less than 0.5 inch per capacitor lead
- Use at least a four-layer Printed Circuit Board (PCB) with two inner layers for V_{DD} and V_{SS}
- Bypass the V_{DD} and V_{SS} layers of the PCB with approximately 100µF, preferably with a high-grade capacitor such as a tantalum capacitor

Part 13 Ordering Information

Table 13-1 lists the pertinent information needed to place an order. Consult a Freescale Semiconductor sales office or authorized distributor to determine availability and to order parts.

Table 13-1 Ordering Information

Part	Supply Voltage	Package Type	Pin Count	Frequency (MHz)	Ambient Temperature Range	Order Number
MC56F8345	3.0–3.6 V	Low-Profile Quad Flat Pack (LQFP)	128	60	-40° to + 105° C	MC56F8345VFG60
MC56F8345	3.0–3.6 V	Low-Profile Quad Flat Pack (LQFP)	128	60	-40° to + 125° C	MC56F8345MFG60
MC56F8145	3.0–3.6 V	Low-Profile Quad Flat Pack (LQFP)	128	40	-40° to + 105° C	MC56F8145VFG
MC56F8345	3.0–3.6 V	Low-Profile Quad Flat Pack (LQFP)	128	60	-40° to + 105° C	MC56F8345VFGE*
MC56F8345	3.0–3.6 V	Low-Profile Quad Flat Pack (LQFP)	128	60	-40° to + 125° C	MC56F8345MFGE*
MC56F8145	3.0–3.6 V	Low-Profile Quad Flat Pack (LQFP)	128	40	-40° to + 105° C	MC56F8145VFGE*

*This package is RoHS compliant.