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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	56800E
Core Size	16-Bit
Speed	60MHz
Connectivity	CANbus, EBI/EMI, SCI, SPI
Peripherals	POR, PWM, Temp Sensor, WDT
Number of I/O	49
Program Memory Size	128KB (64K x 16)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	6K x 16
Voltage - Supply (Vcc/Vdd)	2.25V ~ 3.6V
Data Converters	A/D 16x12b
Oscillator Type	External
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	128-LQFP
Supplier Device Package	128-LQFP (14x20)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mc56f8345vfge

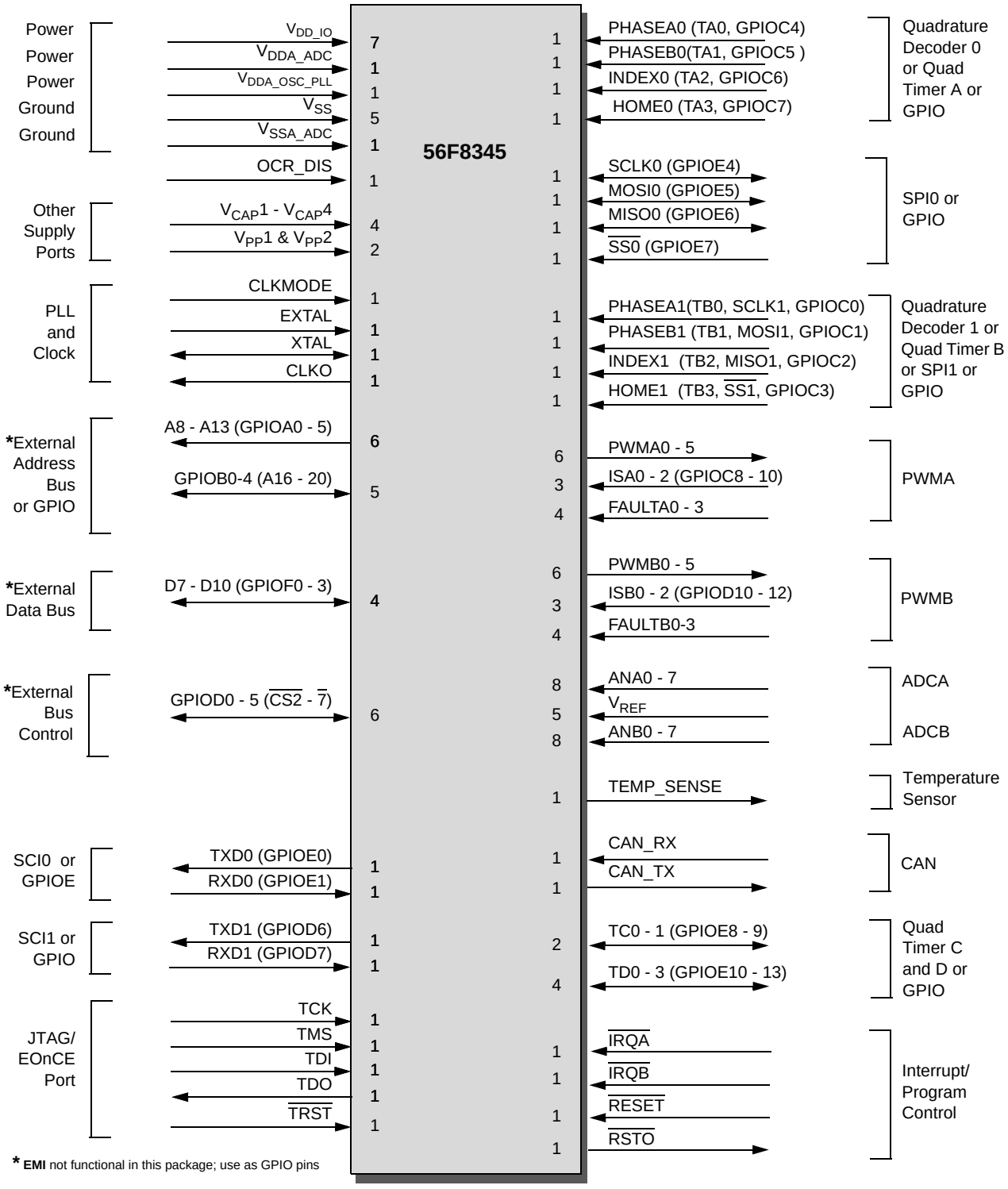


Figure 2-1 56F8345 Signals Identified by Functional Group[1] (128-Pin LQFP)

1. Alternate pin functionality is shown in parenthesis; pin direction/type shown is the default functionality.

Table 2-2 Signal and Package Information for the 128-Pin LQFP

Signal Name	Pin No.	Type	State During Reset	Signal Description
HOME1	12	Schmitt Input	Input, pull-up enabled	**Home** — Quadrature Decoder 1, HOME input
(*TB3*)		Schmitt Input/ Output		**TB3** — Timer B, Channel 3
($\overline{SS1}$)		Schmitt Input		**SPI 1 Slave Select** — In the master mode, this pin is used to arbitrate multiple masters. In slave mode, this pin is used to select the slave. To activate the SPI function, set the HOME_ALT bit in the SIM_GPS register. See **Part 6.5.8** for details.
(GPIOC3)		Schmitt Input/ Output		**Port C GPIO** — This GPIO pin can be individually programmed as input or output pin. In the 56F8345, the default state after reset is HOME1. In the 56F8145, the default state is not one of the functions offered and must be reconfigured. To deactivate the internal pull-up resistor, clear bit 3 in the GPIOC_PUR register.
PWMA0	58	Output	In reset, output is disabled, pull-up is enabled	**PWMA0 - 5** — These are six PWMA output pins.
PWMA1	60			
PWMA2	61			
PWMA3	63			
PWMA4	64			
PWMA5	66			
ISA0	104	Schmitt Input	Input, pull-up enabled	**ISA0 - 2** — These three input current status pins are used for top/bottom pulse width correction in complementary channel operation for PWMA.
(GPIOC8)		Schmitt Input/ Output		**Port C GPIO** — These GPIO pins can be individually programmed as input or output pins. In the 56F8345, these pins default to ISA functionality. In the 56F8145, the default state is not one of the functions offered and must be reconfigured. To deactivate the internal pull-up resistor, clear the appropriate bit of the GPIOC_PUR register. See **Part 6.5.6** for details.
ISA1 **(GPIOC9)**	105			
ISA2 **(GPIOC10)**	106			

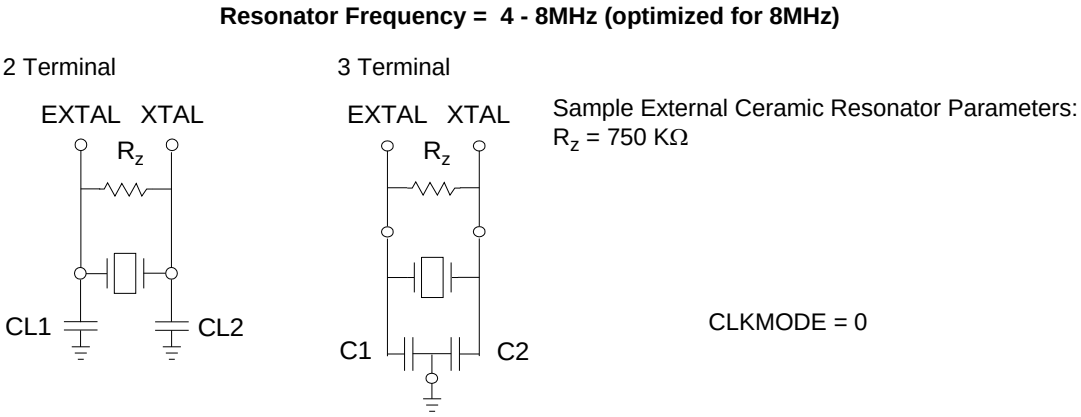


Figure 3-3 Connecting a Ceramic Resonator

Note: The OCCS_COHL bit must be set to 0 when a ceramic resonator is used. The reset condition on the OCCS_COHL bit is 0. Please see the COHL bit in the Oscillator Control (OSCTL) register, discussed in the **56F8300 Peripheral User's Manual**.

3.2.3 External Clock Source

The recommended method of connecting an external clock is illustrated in **Figure 3-4**. The external clock source is connected to XTAL and the EXTAL pin is grounded. Set OCCS_COHL bit high when using an external clock source as well.

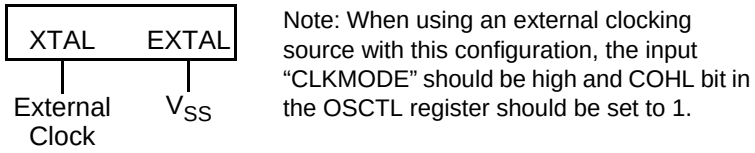


Figure 3-4 Connecting an External Clock Signal Register

3.3 Registers

When referring to the register definitions for the OCCS in the **56F8300 Peripheral User Manual**, use the register definitions **without** the internal Relaxation Oscillator, since the 56F8345/56F8145 devices do NOT contain this oscillator.

Part 4 Memory Map

4.1 Introduction

The 56F8345 and 56F8145 devices are 16-bit motor-control chips based on the 56800E core. These parts use a Harvard-style architecture with two independent memory spaces for Data and Program. On-chip

Table 4-5 Interrupt Vector Table Contents[1] (Continued)

Peripheral	Vector Number	Priority Level	Vector Base Address +	Interrupt Function
FLEXCAN	29	0-2	P:$3A	FLEXCAN Message Buffer Interrupt
GPIOF	30	0-2	P:$3C	GPIO F
GPIOE	31	0-2	P:$3E	GPIO E
GPIOD	32	0-2	P:$40	GPIO D
GPIOC	33	0-2	P:$42	GPIO C
GPIOB	34	0-2	P:$44	GPIO B
GPIOA	35	0-2	P:$46	GPIO A
				Reserved
SPI1	38	0-2	P:$4C	SPI 1 Receiver Full
SPI1	39	0-2	P:$4E	SPI 1 Transmitter Empty
SPI0	40	0-2	P:$50	SPI 0 Receiver Full
SPI0	41	0-2	P:$52	SPI 0 Transmitter Empty
SCI1	42	0-2	P:$54	SCI 1 Transmitter Empty
SCI1	43	0-2	P:$56	SCI 1 Transmitter Idle
				Reserved
SCI1	45	0-2	P:$5A	SCI 1 Receiver Error
SCI1	46	0-2	P:$5C	SCI 1 Receiver Full
DEC1	47	0-2	P:$5E	Quadrature Decoder #1 Home Switch or Watchdog
DEC1	48	0-2	P:$60	Quadrature Decoder #1 INDEX Pulse
DEC0	49	0-2	P:$62	Quadrature Decoder #0 Home Switch or Watchdog
DEC0	50	0-2	P:$64	Quadrature Decoder #0 INDEX Pulse
				Reserved
TMRD	52	0-2	P:$68	Timer D, Channel 0
TMRD	53	0-2	P:$6A	Timer D, Channel 1
TMRD	54	0-2	P:$6C	Timer D, Channel 2
TMRD	55	0-2	P:$6E	Timer D, Channel 3
TMRC	56	0-2	P:$70	Timer C, Channel 0
TMRC	57	0-2	P:$72	Timer C, Channel 1
TMRC	58	0-2	P:$74	Timer C, Channel 2
TMRC	59	0-2	P:$76	Timer C, Channel 3

Table 4-12 Quad Timer B Registers Address Map (Continued)
(TMRB_BASE = $00 F080)
Quad Timer B is NOT available in the 56F8145 device

Register Acronym	Address Offset	Register Description
TMRB3_HOLD	$34	Hold Register
TMRB3_CNTR	$35	Counter Register
TMRB3_CTRL	$36	Control Register
TMRB3_SCR	$37	Status and Control Register
TMRB3_CMPLD1	$38	Comparator Load Register 1
TMRB3_CMPLD2	$39	Comparator Load Register 2
TMRB3_COMSCR	$3A	Comparator Status and Control Register

Table 4-13 Quad Timer C Registers Address Map
(TMRC_BASE = $00 F0C0)

Register Acronym	Address Offset	Register Description
TMRC0_CMP1	$0	Compare Register 1
TMRC0_CMP2	$1	Compare Register 2
TMRC0_CAP	$2	Capture Register
TMRC0_LOAD	$3	Load Register
TMRC0_HOLD	$4	Hold Register
TMRC0_CNTR	$5	Counter Register
TMRC0_CTRL	$6	Control Register
TMRC0_SCR	$7	Status and Control Register
TMRC0_CMPLD1	$8	Comparator Load Register 1
TMRC0_CMPLD2	$9	Comparator Load Register 2
TMRC0_COMSCR	$A	Comparator Status and Control Register
		Reserved
TMRC1_CMP1	$10	Compare Register 1
TMRC1_CMP2	$11	Compare Register 2
TMRC1_CAP	$12	Capture Register
TMRC1_LOAD	$13	Load Register
TMRC1_HOLD	$14	Hold Register
TMRC1_CNTR	$15	Counter Register
TMRC1_CTRL	$16	Control Register
TMRC1_SCR	$17	Status and Control Register
TMRC1_CMPLD1	$18	Comparator Load Register 1

Table 4-13 Quad Timer C Registers Address Map (Continued) (TMRC_BASE = $00 F0C0)

Register Acronym	Address Offset	Register Description
TMRC1_CMPLD2	$19	Comparator Load Register 2
TMRC1_COMSCR	$1A	Comparator Status and Control Register
		Reserved
TMRC2_CMP1	$20	Compare Register 1
TMRC2_CMP2	$21	Compare Register 2
TMRC2_CAP	$22	Capture Register
TMRC2_LOAD	$23	Load Register
TMRC2_HOLD	$24	Hold Register
TMRC2_CNTR	$25	Counter Register
TMRC2_CTRL	$26	Control Register
TMRC2_SCR	$27	Status and Control Register
TMRC2_CMPLD1	$28	Comparator Load Register 1
TMRC2_CMPLD2	$29	Comparator Load Register 2
TMRC2_COMSCR	$2A	Comparator Status and Control Register
		Reserved
TMRC3_CMP1	$30	Compare Register 1
TMRC3_CMP2	$31	Compare Register 2
TMRC3_CAP	$32	Capture Register
TMRC3_LOAD	$33	Load Register
TMRC3_HOLD	$34	Hold Register
TMRC3_CNTR	$35	Counter Register
TMRC3_CTRL	$36	Control Register
TMRC3_SCR	$37	Status and Control Register
TMRC3_CMPLD1	$38	Comparator Load Register 1
TMRC3_CMPLD2	$39	Comparator Load Register 2
TMRC3_COMSCR	$3A	Comparator Status and Control Register

Table 4-14 Quad Timer D Registers Address Map (TMRD_BASE = $00 F100)
Quad Timer D is NOT available in the 56F8145 device

Register Acronym	Address Offset	Register Description
TMRD0_CMP1	$0	Compare Register 1
TMRD0_CMP2	$1	Compare Register 2

Table 4-38 FlexCAN Registers Address Map (FC_BASE = $00 F800)
FlexCAN is NOT available in the 56F8145 device

Register Acronym	Address Offset	Register Description
FCMCR	$0	Module Configuration Register
		Reserved
FCCTL0	$3	Control Register 0 Register
FCCTL1	$4	Control Register 1 Register
FCTMR	$5	Free-Running Timer Register
FCMAXMB	$6	Maximum Message Buffer Configuration Register
		Reserved
FCRXGMASK_H	$8	Receive Global Mask High Register
FCRXGMASK_L	$9	Receive Global Mask Low Register
FCRX14MASK_H	$A	Receive Buffer 14 Mask High Register
FCRX14MASK_L	$B	Receive Buffer 14 Mask Low Register
FCRX15MASK_H	$C	Receive Buffer 15 Mask High Register
FCRX15MASK_L	$D	Receive Buffer 15 Mask Low Register
		Reserved
FCSTATUS	$10	Error and Status Register
FCIMASK1	$11	Interrupt Masks 1 Register
FCIFLAG1	$12	Interrupt Flags 1 Register
FCR/T_ERROR_CNTRS	$13	Receive and Transmit Error Counters Register
		Reserved
		Reserved
		Reserved
FCMB0_CONTROL	$40	Message Buffer 0 Control / Status Register
FCMB0_ID_HIGH	$41	Message Buffer 0 ID High Register
FCMB0_ID_LOW	$42	Message Buffer 0 ID Low Register
FCMB0_DATA	$43	Message Buffer 0 Data Register
FCMB0_DATA	$44	Message Buffer 0 Data Register
FCMB0_DATA	$45	Message Buffer 0 Data Register
FCMB0_DATA	$46	Message Buffer 0 Data Register
		Reserved
FCMSB1_CONTROL	$48	Message Buffer 1 Control / Status Register

5.6 Register Descriptions

A register address is the sum of a base address and an address offset. The base address is defined at the system level and the address offset is defined at the module level. The ITCN peripheral has 24 registers.

Table 5-3 ITCN Register Summary (ITCN_BASE = $00F1A0)

Register Acronym	Base Address +	Register Name	Section Location
IPR0	$0	Interrupt Priority Register 0	5.6.1
IPR1	$1	Interrupt Priority Register 1	5.6.2
IPR2	$2	Interrupt Priority Register 2	5.6.3
IPR3	$3	Interrupt Priority Register 3	5.6.4
IPR4	$4	Interrupt Priority Register 4	5.6.5
IPR5	$5	Interrupt Priority Register 5	5.6.6
IPR6	$6	Interrupt Priority Register 6	5.6.7
IPR7	$7	Interrupt Priority Register 7	5.6.8
IPR8	$8	Interrupt Priority Register 8	5.6.9
IPR9	$9	Interrupt Priority Register 9	5.6.10
VBA	$A	Vector Base Address Register	5.6.11
FIM0	$B	Fast Interrupt 0 Match Register	5.6.12
FIVAL0	$C	Fast Interrupt 0 Vector Address Low Register	5.6.13
FIVAH0	$D	Fast Interrupt 0 Vector Address High Register	5.6.14
FIM1	$E	Fast Interrupt 1 Match Register	5.6.15
FIVAL1	$F	Fast Interrupt 1 Vector Address Low Register	5.6.16
FIVAH1	$10	Fast Interrupt 1 Vector Address High Register	5.6.17
IRQP0	$11	IRQ Pending Register 0	5.6.18
IRQP1	$12	IRQ Pending Register 1	5.6.19
IRQP2	$13	IRQ Pending Register 2	5.6.20
IRQP3	$14	IRQ Pending Register 3	5.6.21
IRQP4	$15	IRQ Pending Register 4	5.6.22
IRQP5	$16	IRQ Pending Register 5	5.6.23
		Reserved	
ICTL	$1D	Interrupt Control Register	5.6.30

Add. Offset	Register Name		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
$0	IPR0	R	0	0	BKPT_U0 IPL		STPCNT IPL		0	0	0	0	0	0	0	0	0	0
		W																
$1	IPR1	R	0	0	0	0	0	0	0	0	0	0	RX_REG IPL		TX_REG IPL		TRBUF IPL	
		W																
$2	IPR2	R	FMCBE IPL		FMCC IPL		FMERR IPL		LOCK IPL		LVI IPL		0	0	IRQB IPL		IRQA IPL	
		W																
$3	IPR3	R	GPIOD IPL		GPIOE IPL		GPIOF IPL		FCMSGBUF IPL		FCWKUP IPL		FCERR IPL		FCBOFF IPL		0	0
		W																
$4	IPR4	R	SPI0_RCV IPL		SPI1_XMIT IPL		SPI1_RCV IPL		0	0	0	0	GPIOA IPL		GPIOB IPL		GPIOC IPL	
		W																
$5	IPR5	R	DEC1_XIRQ IPL		DEC1_HIRQ IPL		SCI1_RCV IPL		SCI1_RERR IPL		0	0	SCI1_TIDL IPL		SCI1_XMIT IPL		SPI0_XMIT IPL	
		W																
$6	IPR6	R	TMRC0 IPL		TMRD3 IPL		TMRD2 IPL		TMRD1 IPL		TMRD0 IPL		0	0	DEC0_XIRQ IPL		DEC0_HIRQ IPL	
		W																
$7	IPR7	R	TMRA0 IPL		TMRB3 IPL		TMRB2 IPL		TMRB1 IPL		TMRB0 IPL		TMRC3 IPL		TMRC2 IPL		TMRC1 IPL	
		W																
$8	IPR8	R	SCI0_RCV IPL		SCI0_RERR IPL		0	0	SCI0_TIDL IPL		SCI0_XMIT IPL		TMRA3 IPL		TMRA2 IPL		TMRA1 IPL	
		W																
$9	IPR9	R	PWMA_F IPL		PWMB_F IPL		PWMA_RL IPL		PWMB_RL IPL		ADCA_ZC IPL		ABCB_ZC IPL		ADCA_CC IPL		ADCB_CC IPL	
		W																
$A	VBA	R	0	0	0	VECTOR BASE ADDRESS												
		W																
$B	FIM0	R	0	0	0	0	0	0	0	0	0	FAST INTERRUPT 0						
		W																
$C	FIVAL0	R	FAST INTERRUPT 0 VECTOR ADDRESS LOW															
		W																
$D	FIVAH0	R	0	0	0	0	0	0	0	0	0	0	0	FAST INTERRUPT 0 VECTOR ADDRESS HIGH				
		W																
$E	FIM1	R	0	0	0	0	0	0	0	0	0	FAST INTERRUPT 1						
		W																
$F	FIVAL1	R	FAST INTERRUPT 1 VECTOR ADDRESS LOW															
		W																
$10	FIVAH1	R	0	0	0	0	0	0	0	0	0	0	0	FAST INTERRUPT 1 VECTOR ADDRESS HIGH				
		W	0	0	0	0	0	0	0	0	0	0	0					
$11	IRQP0	R	PENDING [16:2]															1
		W																
$12	IRQP1	R	PENDING [32:17]															
		W																
$13	IRQP2	R	PENDING [48:33]															
		W																
$14	IRQP3	R	PENDING [64:49]															
		W																
$15	IRQP4	R	PENDING [80:65]															
		W																
$16	IRQP5	R	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	PEND-ING [81]
		W																
	Reserved																	
$1D	ICTL	R	INT	IPIC			VAB						INT_DIS	1	$\overline{\text{IRQB}}$ STATE	$\overline{\text{IRQA}}$ STATE	$\overline{\text{IRQB}}$ EDG	$\overline{\text{IRQA}}$ EDG
		W																

= Reserved

- 00 = IRQ disabled (default)
- 01 = IRQ is priority level 0
- 10 = IRQ is priority level 1
- 11 = IRQ is priority level 2

5.6.9.8 Timer A, Channel 1 Interrupt Priority Level (TMRA1 IPL)—Bits 1–0

This field is used to set the interrupt priority level for IRQs. This IRQ is limited to priorities 0 through 2. They are disabled by default.

- 00 = IRQ disabled (default)
- 01 = IRQ is priority level 0
- 10 = IRQ is priority level 1
- 11 = IRQ is priority level 2

5.6.10 Interrupt Priority Register 9 (IPR9)

Base + $9	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read	PWMA_F IPL		PWMB_F IPL		PWMA_RL IPL		PWMB_RL IPL		ADCA_ZC IPL		ABCB_ZC IPL		ADCA_CC IPL		ADCB_CC IPL	
Write																
RESET	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 5-12 Interrupt Priority Register 9 (IPR9)

5.6.10.1 PWM A Fault Interrupt Priority Level (PWMA_F IPL)—Bits 15–14

This field is used to set the interrupt priority level for IRQs. This IRQ is limited to priorities 0 through 2. They are disabled by default.

- 00 = IRQ disabled (default)
- 01 = IRQ is priority level 0
- 10 = IRQ is priority level 1
- 11 = IRQ is priority level 2

5.6.10.2 PWM B Fault Interrupt Priority Level (PWMB_F IPL)—Bits 13–12

This field is used to set the interrupt priority level for IRQs. This IRQ is limited to priorities 0 through 2. They are disabled by default.

- 00 = IRQ disabled (default)
- 01 = IRQ is priority level 0
- 10 = IRQ is priority level 1
- 11 = IRQ is priority level 2

Part 6 System Integration Module (SIM)

6.1 Introduction

The SIM module is a system catchall for the glue logic that ties together the system-on-chip. It controls distribution of resets and clocks and provides a number of control features. The system integration module is responsible for the following functions:

- Reset sequencing
- Clock generation & distribution
- Stop/Wait control
- Pull-up enables for selected peripherals
- System status registers
- Registers for software access to the JTAG ID of the chip
- Enforcing Flash security

These are discussed in more detail in the sections that follow.

6.2 Features

The SIM has the following features:

- Flash security feature prevents unauthorized access to code/data contained in on-chip Flash memory
- Power-saving clock gating for peripheral
- Three power modes (Run, Wait, Stop) to control power utilization
  - Stop mode shuts down the 56800E core, system clock, peripheral clock, and PLL operation
  - Stop mode entry can optionally disable PLL and Oscillator (low power vs. fast restart); must be done explicitly
  - Wait mode shuts down the 56800E core and unnecessary system clock operation
  - Run mode supports full part operation
- Controls to enable/disable the 56800E core WAIT and STOP instructions
- Calculates base delay for reset extension based upon POR or $\overline{\text{RESET}}$ operations. Reset delay will be 3 x 32 clocks (phased release of reset) for reset, except for POR, which is 2^{21} clock cycles.
- Controls reset sequencing after reset
- Software-initiated reset
- Four 16-bit registers reset only by a Power-On Reset usable for general-purpose software control
- System Control Register
- Registers for software access to the JTAG ID of the chip

6.5.6.2 PWMA1—Bit 14
This bit controls the pull-up resistors on the FAULTA3 pin.

6.5.6.3 CAN—Bit 13
This bit controls the pull-up resistors on the CAN_RX pin.

6.5.6.4 EMI_MODE—Bit 12
This bit controls the pull-up resistors on the EMI_MODE pin.

Note: In this package, this input pin is double-bonded with the adjacent V_{SS} pin and this bit should be changed to a 1 in order to reduce power consumption.

6.5.6.5 $\overline{\text{RESET}}$—Bit 11
This bit controls the pull-up resistors on the $\overline{\text{RESET}}$ pin.

6.5.6.6 IRQ—Bit 10
This bit controls the pull-up resistors on the $\overline{\text{IRQA}}$ and $\overline{\text{IRQB}}$ pins.

6.5.6.7 XBOOT—Bit 9
This bit controls the pull-up resistors on the EXTBOOT pin.

Note: In this package, this input pin is double-bonded with the adjacent V_{SS} pin and this bit should be changed to a 1 in order to reduce power consumption.

6.5.6.8 PWMB—Bit 8
This bit controls the pull-up resistors on the FAULTB0, FAULTB1, FAULTB2, and FAULTB3 pins.

6.5.6.9 PWMA0—Bit 7
This bit controls the pull-up resistors on the FAULTA0, FAULTA1, and FAULTA2 pins.

6.5.6.10 Reserved—Bit 6
This bit field is reserved or not implemented. It is read as 0 and cannot be modified by writing.

6.5.6.11 CTRL—Bit 5
This bit controls the pull-up resistors on the $\overline{\text{WR}}$ and $\overline{\text{RD}}$ pins.

6.5.6.12 Reserved—Bit 4
This bit field is reserved or not implemented. It is read as 0 and cannot be modified by writing.

6.5.6.13 JTAG—Bit 3
This bit controls the pull-up resistors on the $\overline{\text{TRST}}$, TMS and TDI pins.

Table 6-3 Clock Operation in Power-Down Modes

Mode	Core Clocks	Peripheral Clocks	Description
Run	Active	Active	Device is fully functional
Wait	Core and memory clocks disabled	Active	Peripherals are active and can produce interrupts if they have not been masked off. Interrupts will cause the core to come out of its suspended state and resume normal operation. Typically used for power-conscious applications.
Stop	System clocks continue to be generated in the SIM, but most are gated prior to reaching memory, core and peripherals.		The only possible recoveries from Stop mode are: 1. CAN traffic (1st message will be lost) 2. Non-clocked interrupts 3. COP reset 4. External reset 5. Power-on reset

All peripherals, except the COP/watchdog timer, run off the IPBus clock frequency, which is the same as the main processor frequency in this architecture. The maximum frequency of operation is SYS_CLK = 60MHz.

6.8 Stop and Wait Mode Disable Function

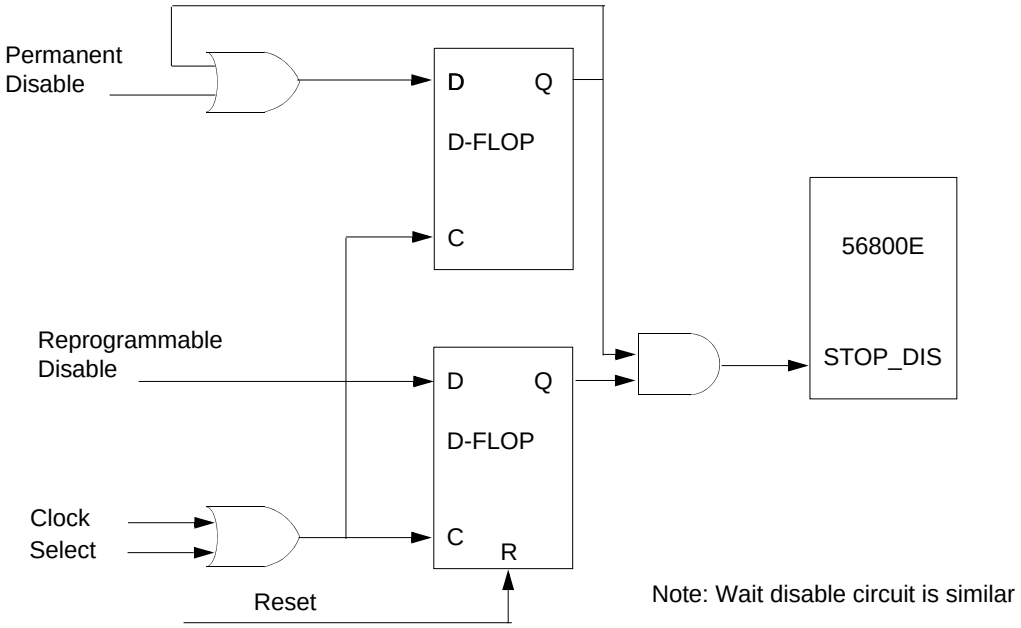


Figure 6-16 Internal Stop Disable Circuit

The 56800E core contains both STOP and WAIT instructions. Both put the CPU to sleep. For lowest power consumption in Stop mode, the PLL can be shut down. This must be done explicitly before entering Stop mode, since there is no automatic mechanism for this. When the PLL is shut down, the 56800E system clock must be set equal to the oscillator output.

Table 8-2 56F8145 GPIO Ports Configuration

GPIO Port	Port Width	Available Pins in 56F8145	Peripheral Function	Reset Function
F	16	4	4 pins - EMI Data - Can only be used as GPIO 12 pins - EMI Data - Not available in this package	EMI Data N/A

Table 8-3 GPIO External Signals Map

Pins in shaded rows are not available in 56F8345 / 56F8145

Pins in italics are NOT available in the 56F8145 device

GPIO Port	GPIO Bit	Reset Function	Functional Signal	Package Pin #
GPIOA	0	Peripheral	A8[1]	15
	1	Peripheral	A9[1]	16
	2	Peripheral	A10[1]	17
	3	Peripheral	A11[1]	18
	4	Peripheral	A12[1]	19
	5	Peripheral	A13[1]	20
	6	N/A		
	7	N/A		
	8	N/A		
	9	N/A		
	10	N/A		
	11	N/A		
	12	N/A		
	13	N/A		

Table 10-1 Absolute Maximum Ratings (Continued)

(V_{SS} = V_{SSA_ADC} = 0)

Characteristic	Symbol	Notes	Min	Max	Unit
Junction Temperature (Automotive)	T_J		-40	150	°C
Junction Temperature (Industrial)	T_J		-40	125	°C
Storage Temperature (Automotive)	T_{STG}		-55	150	°C
Storage Temperature (Industrial)	T_{STG}		-55	150	°C

1. If corresponding GPIO pin is configured as open drain.

Note: *Pins in italics are NOT available in the 56F8145 device.*

Pin Group 1: TXD0-1, RXD0-1, $\overline{SS0}$, MISO0, MOSI0

Pin Group 2: PHASEA0, *PHASEA1*, PHASEB0, *PHASEB1*, INDEX0, *INDEX1*, HOME0, *HOME1*, ISB0-2, *ISA0-2*, *TD2-3*, TC0-1, TDO, SCLK0

Pin Group 3: $\overline{RSTO}$, TDO

Pin Group 4: *CAN_TX*

Pin Group 5: D0-15, GPIOD0-5

Pin Group 6: A8-15, GPIOB0-4, TD0-1

Pin Group 7: CLKO

Pin Group 8: *PWMA0-5*, PWMB0-5

Pin Group 9: $\overline{IRQA}$, $\overline{IRQB}$, $\overline{RESET}$, EXTBOOT, $\overline{TRST}$,TMS, TDI, *CAN_RX*, EMI_MODE, *FAULTA0-3*, FAULTB0-3

Pin Group 10: TCK

Pin Group 11: XTAL, EXTAL

Pin Group 12: ANA0-7, ANB0-7

Pin Group 13: OCR_DIS, CLKMODE

Table 10-6 Power-On Reset Low Voltage Parameters

Characteristic	Symbol	Min	Typ	Max	Units
POR Trip Point	POR	1.75	1.8	1.9	V
LVI, 2.5 volt Supply, trip point[1]	$V_{EI2.5}$	—	2.14	—	V
LVI, 3.3 volt supply, trip point[2]	$V_{EI3.3}$	—	2.7	—	V
Bias Current	I_{bias}	—	110	130	μA

1. When V_{DD_CORE} drops below $V_{EI2.5}$, an interrupt is generated.
2. When V_{DD_CORE} drops below $V_{EI3.3}$, an interrupt is generated.

Table 10-7 Current Consumption per Power Supply Pin (Typical)
On-Chip Regulator Enabled (OCR_DIS = Low)

Mode	I_{DD_IO}[1]	I_{DD_ADC}	$I_{DD\_OSC\_PLL}$	Test Conditions
RUN1_MAC	155mA	50mA	2.5mA	• 60MHz Device Clock • All peripheral clocks are enabled • All peripherals running • Continuous MAC instructions with fetches from Data RAM • ADC powered on and clocked
Wait3	91mA	65μA	2.5mA	• 60MHz Device Clock • All peripheral clocks are enabled • ADC powered off
Stop1	5.8mA	0μA	155μA	• 8MHz Device Clock • All peripheral clocks are off • ADC powered off • PLL powered off
Stop2	5.1mA	0μA	145μA	• External Clock is off • All peripheral clocks are off • ADC powered off • PLL powered off

1. No Output Switching
2. Includes Processor Core current supplied by internal voltage regulator

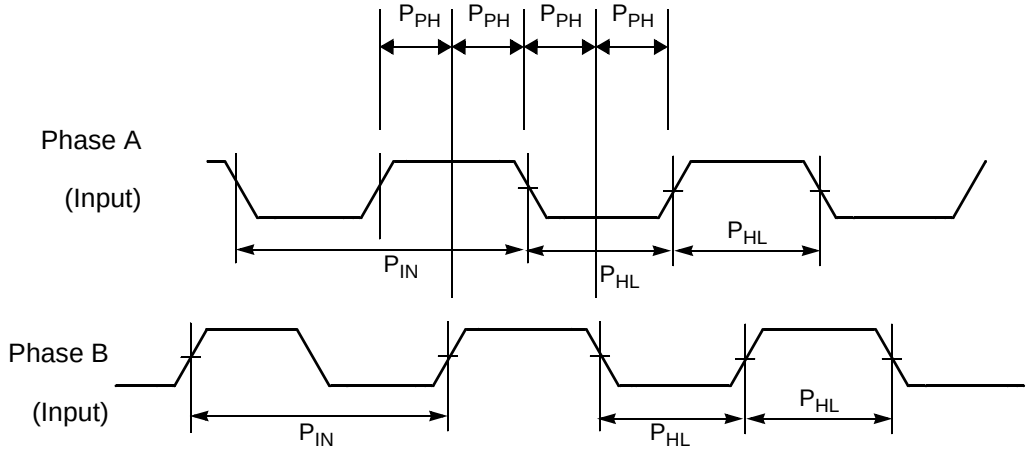


Figure 10-14 Quadrature Decoder Timing

10.12 Serial Communication Interface (SCI) Timing

Table 10-20 SCI Timing[1]

Characteristic	Symbol	Min	Max	Unit	See Figure
Baud Rate[2]	BR	—	(f_{MAX}/16)	Mbps	—
RXD[3] Pulse Width	RXD_{PW}	0.965/BR	1.04/BR	ns	10-15
TXD[4] Pulse Width	TXD_{PW}	0.965/BR	1.04/BR	ns	10-16

1. Parameters listed are guaranteed by design.
2. f_{MAX} is the frequency of operation of the system clock, ZCLK, in MHz, which is 60MHz for the 56F8345 device and 40MHz for the 56F8145 device.
3. The RXD pin in SCI0 is named RXD0 and the RXD pin in SCI1 is named RXD1.
4. The TXD pin in SCI0 is named TXD0 and the TXD pin in SCI1 is named TXD1.

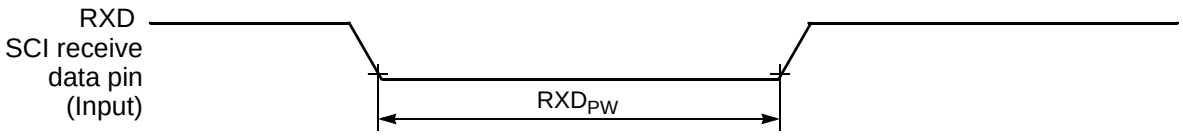


Figure 10-15 RXD Pulse Width

Table 10-24 IO Loading Coefficients at 10MHz

	Intercept	Slope
PDU08DGZ_ME	1.3	0.11mW / pF
PDU04DGZ_ME	1.15mW	0.11mW / pF

Power due to capacitive loading on output pins is (first order) a function of the capacitive load and frequency at which the outputs change. **Table 10-24** provides coefficients for calculating power dissipated in the IO cells as a function of capacitive load. In these cases:

Total Power = Σ((Intercept +Slope*Cload)*frequency/10MHz)

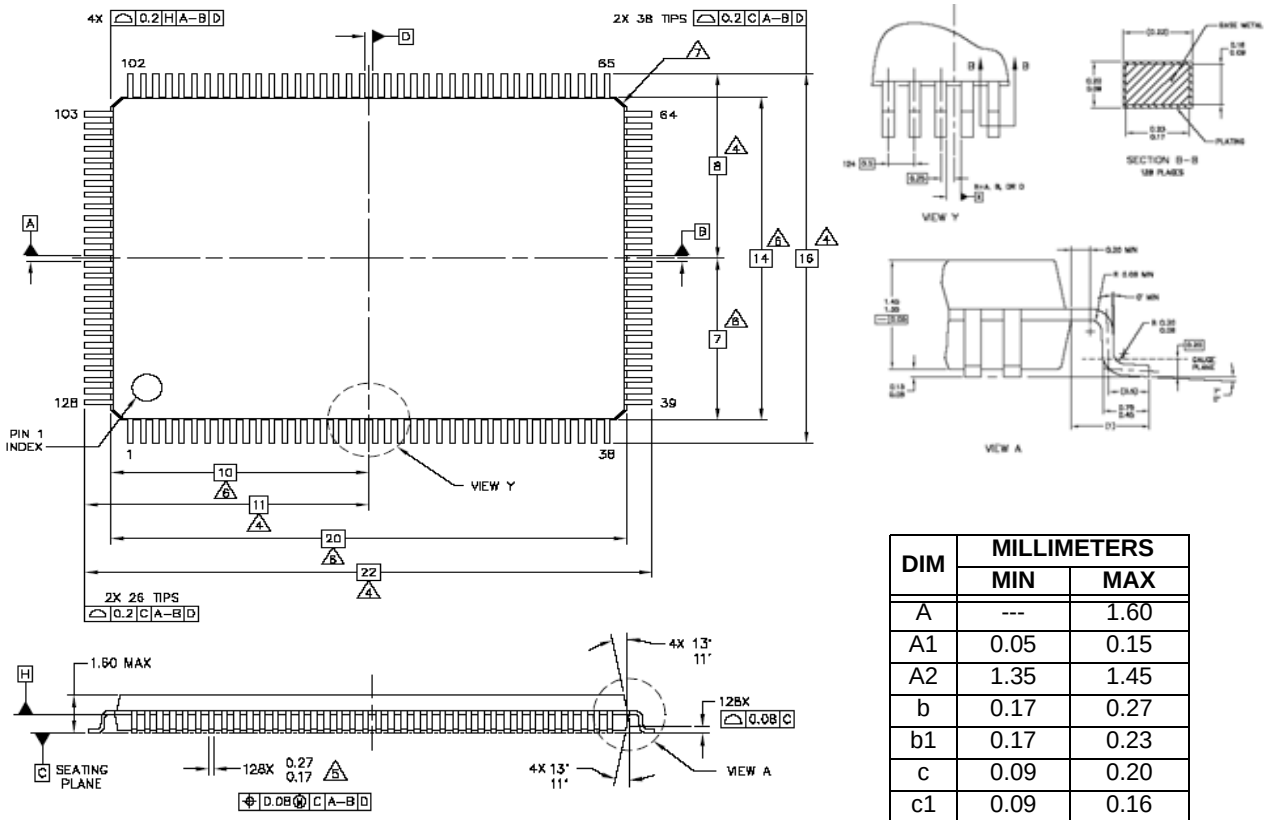
where:

- Summation is performed over all output pins with capacitive loads
- Total Power is expressed in mW
- Cload is expressed in pF

Because of the low duty cycle on most device pins, power dissipation due to capacitive loads was found to be fairly low when averaged over a period of time.

E, the external [static component], reflects the effects of placing resistive loads on the outputs of the device. Sum the total of all V^2/R or IV to arrive at the resistive load contribution to power. Assume V = 0.5 for the purposes of these rough calculations. For instance, if there is a total of eight PWM outputs driving 10mA into LEDs, then P = 8*.5*.01 = 40mW.

In previous discussions, power consumption due to parasitics associated with pure input pins is ignored, as it is assumed to be negligible.



DIM	MILLIMETERS	
	MIN	MAX
A	---	1.60
A1	0.05	0.15
A2	1.35	1.45
b	0.17	0.27
b1	0.17	0.23
c	0.09	0.20
c1	0.09	0.16
D	22.00 BSC	
D1	20.00BSC	
e	0.50 BSC	
E	16.00 BSC	
E1	14.00 BSC	
L	0.45	0.75
L1	1.00 REF	
L2	0.50 REF	
S	0.20	---
R1	0.08	---
R2	0.08	0.20
0	0°	7°
01	0°	---
02	11°	13°

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DATUM PLANE H IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.
4. DATUMS A, B, AND D TO BE DETERMINED AT DATUM PLANE H.
5. DIMENSIONS D AND E TO BE DETERMINED AT SEATING PLANE C.
6. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 PER SIDE. DIMENSIONS D1 AND E1 DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.
7. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. DAMBAR PROTRUSION SHALL NOT CAUSE THE b DIMENSION TO EXCEED 0.35.

Figure 11-3 128-pin LQFP Mechanical Information

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