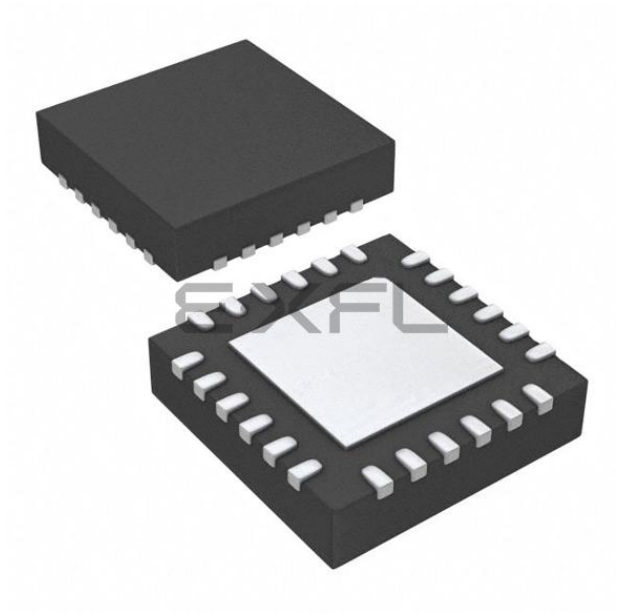

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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Discontinued at Digi-Key
Core Processor	ARM® Cortex®-M0+
Core Size	32-Bit Single-Core
Speed	25MHz
Connectivity	I²C, IrDA, SmartCard, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, I²S, POR, PWM, WDT
Number of I/O	17
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	1.98V ~ 3.8V
Data Converters	A/D 4x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	24-VQFN Exposed Pad
Supplier Device Package	24-QFN (5x5)
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/efm32hg108f32g-b-qfn24

There is also a read-only page in the information block containing system and device calibration data. Read and write operations are supported in the energy modes EM0 and EM1.

2.1.4 Direct Memory Access Controller (DMA)

The Direct Memory Access (DMA) controller performs memory operations independently of the CPU. This has the benefit of reducing the energy consumption and the workload of the CPU, and enables the system to stay in low energy modes when moving for instance data from the USART to RAM or from the External Bus Interface to a PWM-generating timer. The DMA controller uses the PL230 µDMA controller licensed from ARM.

2.1.5 Reset Management Unit (RMU)

The RMU is responsible for handling the reset functionality of the EFM32HG.

2.1.6 Energy Management Unit (EMU)

The Energy Management Unit (EMU) manage all the low energy modes (EM) in EFM32HG microcontrollers. Each energy mode manages if the CPU and the various peripherals are available. The EMU can also be used to turn off the power to unused SRAM blocks.

2.1.7 Clock Management Unit (CMU)

The Clock Management Unit (CMU) is responsible for controlling the oscillators and clocks on-board the EFM32HG. The CMU provides the capability to turn on and off the clock on an individual basis to all peripheral modules in addition to enable/disable and configure the available oscillators. The high degree of flexibility enables software to minimize energy consumption in any specific application by not wasting power on peripherals and oscillators that are inactive.

2.1.8 Watchdog (WDOG)

The purpose of the watchdog timer is to generate a reset in case of a system failure, to increase application reliability. The failure may e.g. be caused by an external event, such as an ESD pulse, or by a software failure.

2.1.9 Peripheral Reflex System (PRS)

The Peripheral Reflex System (PRS) system is a network which lets the different peripheral module communicate directly with each other without involving the CPU. Peripheral modules which send out Reflex signals are called producers. The PRS routes these reflex signals to consumer peripherals which apply actions depending on the data received. The format for the Reflex signals is not given, but edge triggers and other functionality can be applied by the PRS.

2.1.10 Inter-Integrated Circuit Interface (I2C)

The I^2C module provides an interface between the MCU and a serial I^2C-bus. It is capable of acting as both a master and a slave, and supports multi-master buses. Both standard-mode, fast-mode and fast-mode plus speeds are supported, allowing transmission rates all the way from 10 kbit/s up to 1 Mbit/s. Slave arbitration and timeouts are also provided to allow implementation of an SMBus compliant system. The interface provided to software by the I^2C module, allows both fine-grained control of the transmission process and close to automatic transfers. Automatic recognition of slave addresses is provided in all energy modes.

2.1.11 Universal Synchronous/Asynchronous Receiver/Transmitter (USART)

The Universal Synchronous Asynchronous serial Receiver and Transmitter (USART) is a very flexible serial I/O module. It supports full duplex asynchronous UART communication as well as RS-485, SPI, MicroWire and 3-wire. It can also interface with ISO7816 SmartCards, IrDA and I2S devices.

2.1.12 Pre-Programmed UART Bootloader

The bootloader presented in application note AN0003 is pre-programmed in the device at factory. Auto-baud and destructive write are supported. The autobaud feature, interface and commands are described further in the application note.

2.1.13 Low Energy Universal Asynchronous Receiver/Transmitter (LEUART)

The unique LEUART™, the Low Energy UART, is a UART that allows two-way UART communication on a strict power budget. Only a 32.768 kHz clock is needed to allow UART communication up to 9600 baud/s. The LEUART includes all necessary hardware support to make asynchronous serial communication possible with minimum of software intervention and energy consumption.

2.1.14 Timer/Counter (TIMER)

The 16-bit general purpose Timer has 3 compare/capture channels for input capture and compare/Pulse-Width Modulation (PWM) output. TIMER0 also includes a Dead-Time Insertion module suitable for motor control applications.

2.1.15 Real Time Counter (RTC)

The Real Time Counter (RTC) contains a 24-bit counter and is clocked either by a 32.768 kHz crystal oscillator, or a 32.768 kHz RC oscillator. In addition to energy modes EM0 and EM1, the RTC is also available in EM2. This makes it ideal for keeping track of time since the RTC is enabled in EM2 where most of the device is powered down.

2.1.16 Pulse Counter (PCNT)

The Pulse Counter (PCNT) can be used for counting pulses on a single input or to decode quadrature encoded inputs. It runs off either the internal LFACLK or the PCNTn_S0IN pin as external clock source. The module may operate in energy mode EM0 - EM3.

2.1.17 Analog Comparator (ACMP)

The Analog Comparator is used to compare the voltage of two analog inputs, with a digital output indicating which input voltage is higher. Inputs can either be one of the selectable internal references or from external pins. Response time and thereby also the current consumption can be configured by altering the current supply to the comparator.

2.1.18 Voltage Comparator (VCMP)

The Voltage Supply Comparator is used to monitor the supply voltage from software. An interrupt can be generated when the supply falls below or rises above a programmable threshold. Response time and thereby also the current consumption can be configured by altering the current supply to the comparator.

2.1.19 General Purpose Input/Output (GPIO)

In the EFM32HG108, there are 17 General Purpose Input/Output (GPIO) pins, which are divided into ports with up to 16 pins each. These pins can individually be configured as either an output or input. More advanced configurations like open-drain, filtering and drive strength can also be configured individually for the pins. The GPIO pins can also be overridden by peripheral pin connections, like Timer PWM outputs or USART communication, which can be routed to several locations on the device. The GPIO supports up to 11 asynchronous external pin interrupts, which enables interrupts from any pin on the device. Also, the input value of a pin can be routed through the Peripheral Reflex System to other peripherals.

Symbol	Parameter	Condition	Min	Typ	Max	Unit
		EM2 current with RTC prescaled to 1 Hz, 32.768 kHz LFRCO, V_{DD}= 3.0 V, T_{AMB}=85°C		1.6	3.50	µA
I_{EM3}	EM3 current	EM3 current (ULFRCO enabled, LFRCO/LFXO disabled), V_{DD}= 3.0 V, T_{AMB}=25°C		0.6	0.90	µA
		EM3 current (ULFRCO enabled, LFRCO/LFXO disabled), V_{DD}= 3.0 V, T_{AMB}=85°C		1.2	2.65	µA
I_{EM4}	EM4 current	V_{DD}= 3.0 V, T_{AMB}=25°C		0.02	0.035	µA
		V_{DD}= 3.0 V, T_{AMB}=85°C		0.18	0.480	µA

3.4.1 EM0 Current Consumption

Figure 3.1. EM0 Current consumption while executing prime number calculation code from flash with HFRCO running at 24 MHz

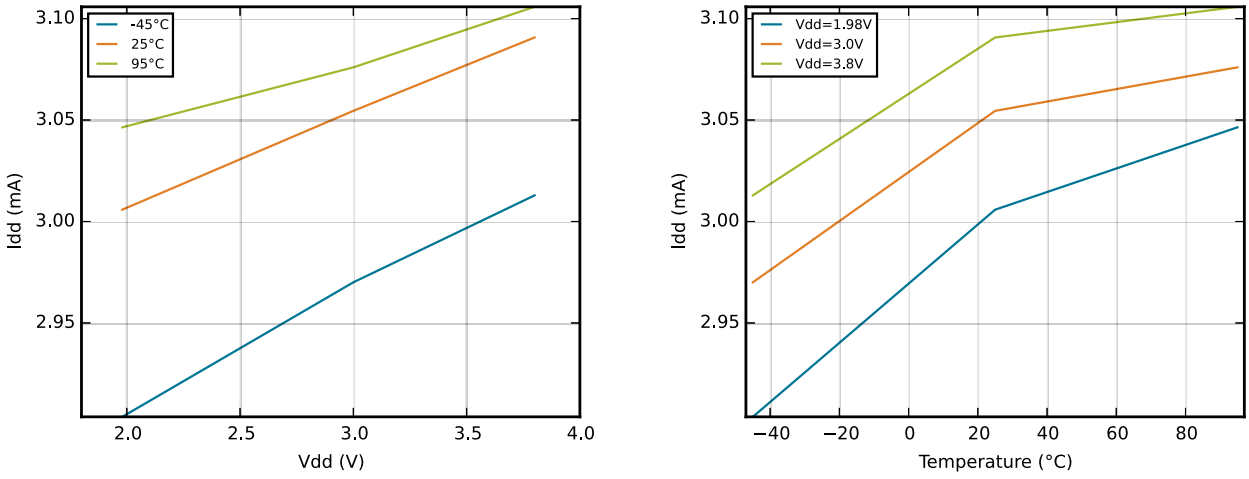
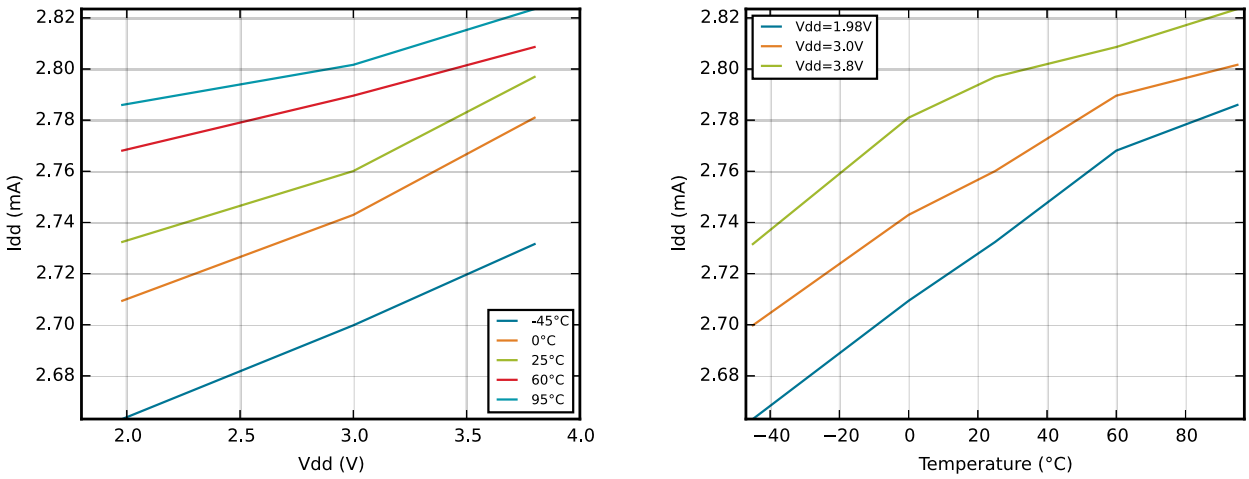
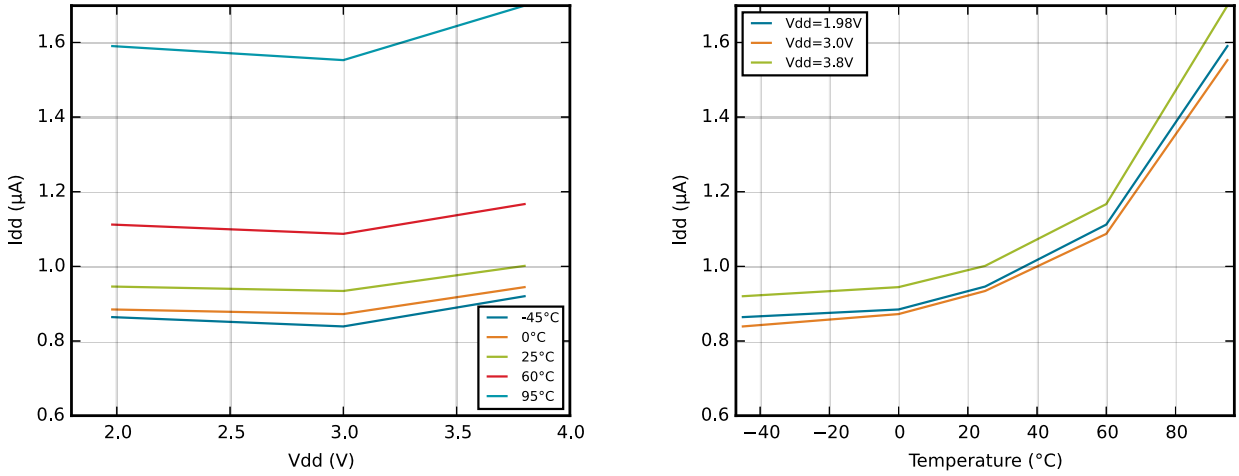


Figure 3.2. EM0 Current consumption while executing prime number calculation code from flash with HFRCO running at 21 MHz



3.4.3 EM2 Current Consumption

Figure 3.11. EM2 current consumption. RTC prescaled to 1kHz, 32.768 kHz LFRCO.



3.4.4 EM3 Current Consumption

Figure 3.12. EM3 current consumption.

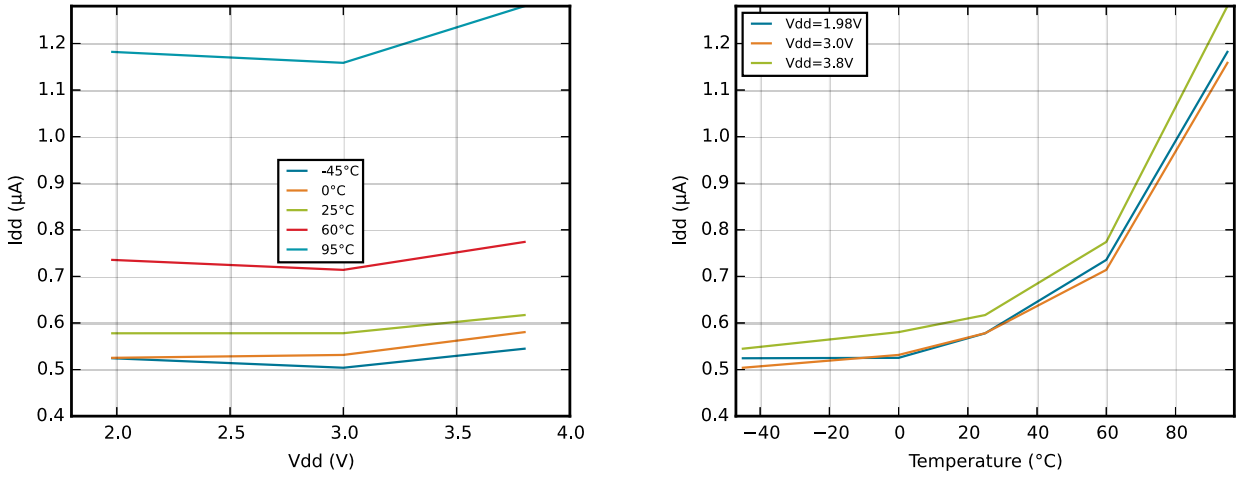


Table 3.5. Power Management

Symbol	Parameter	Condition	Min	Typ	Max	Unit
$V_{BODextthr-}$	BOD threshold on falling external supply voltage	EM0	1.74		1.96	V
		EM2	1.71	1.86	1.98	V
$V_{BODextthr+}$	BOD threshold on rising external supply voltage			1.85		V
t_{RESET}	Delay from reset is released until program execution starts	Applies to Power-on Reset, Brown-out Reset and pin reset.		163		µs
$C_{DECOUPLE}$	Voltage regulator decoupling capacitor.	X5R capacitor recommended. Apply between DECOUPLE pin and GROUND		1		µF

3.7 Flash

Table 3.6. Flash

Symbol	Parameter	Condition	Min	Typ	Max	Unit
EC_{FLASH}	Flash erase cycles before failure		20000			cycles
RET_{FLASH}	Flash data retention	T_{AMB}<150°C	10000			h
		T_{AMB}<85°C	10			years
		T_{AMB}<70°C	20			years
t_{W_PROG}	Word (32-bit) programming time		20			µs
t_{P_ERASE}	Page erase time		20	20.4	20.8	ms
t_{D_ERASE}	Device erase time		40	40.8	41.6	ms
I_{ERASE}	Erase current				7[1]	mA
I_{WRITE}	Write current				7[1]	mA
V_{FLASH}	Supply voltage during flash erase and write		1.98		3.8	V

[1]Measured at 25°C

3.8 General Purpose Input Output

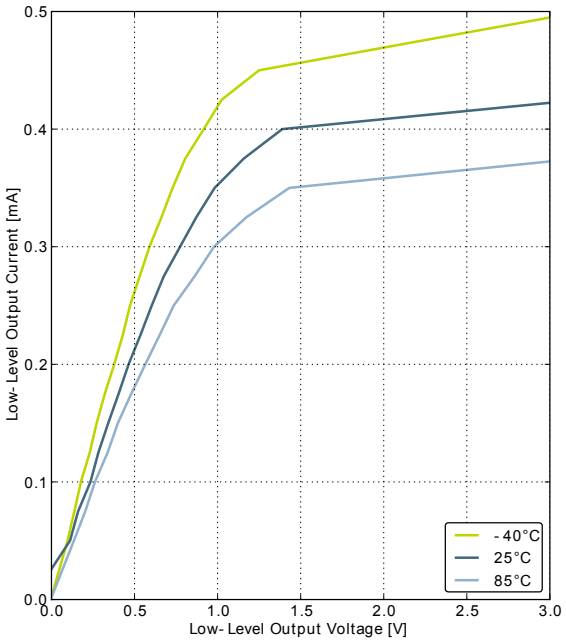
Table 3.7. GPIO

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{IOIL}	Input low voltage				$0.30V_{DD}$	V
V_{IOIH}	Input high voltage		$0.70V_{DD}$			V
V_{IOOH}	Output high voltage (Production test condition = 3.0V, DRIVEMODE = STANDARD)	Sourcing 0.1 mA, V_{DD}=1.98 V, GPIO_Px_CTRL DRIVEMODE = LOWEST		$0.80V_{DD}$		V
		Sourcing 0.1 mA, V_{DD}=3.0 V, GPIO_Px_CTRL DRIVEMODE = LOWEST		$0.90V_{DD}$		V

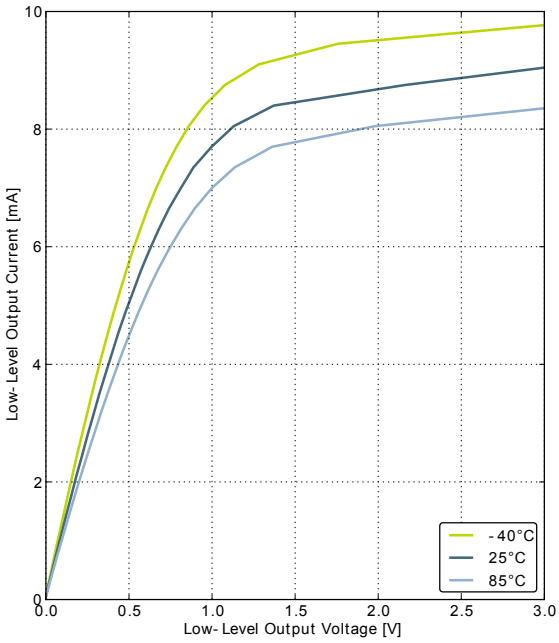
Symbol	Parameter	Condition	Min	Typ	Max	Unit
		Sourcing 1 mA, V_{DD}=1.98 V, GPIO_Px_CTRL DRIVEMODE = LOW		0.85V_{DD}		V
		Sourcing 1 mA, V_{DD}=3.0 V, GPIO_Px_CTRL DRIVEMODE = LOW		0.90V_{DD}		V
		Sourcing 6 mA, V_{DD}=1.98 V, GPIO_Px_CTRL DRIVEMODE = STANDARD	0.75V_{DD}			V
		Sourcing 6 mA, V_{DD}=3.0 V, GPIO_Px_CTRL DRIVEMODE = STANDARD	0.85V_{DD}			V
		Sourcing 20 mA, V_{DD}=1.98 V, GPIO_Px_CTRL DRIVEMODE = HIGH	0.60V_{DD}			V
		Sourcing 20 mA, V_{DD}=3.0 V, GPIO_Px_CTRL DRIVEMODE = HIGH	0.80V_{DD}			V
V_{IOOL}	Output low voltage (Production test condition = 3.0V, DRIVEMODE = STANDARD)	Sinking 0.1 mA, V_{DD}=1.98 V, GPIO_Px_CTRL DRIVEMODE = LOWEST		0.20V_{DD}		V
		Sinking 0.1 mA, V_{DD}=3.0 V, GPIO_Px_CTRL DRIVEMODE = LOWEST		0.10V_{DD}		V
		Sinking 1 mA, V_{DD}=1.98 V, GPIO_Px_CTRL DRIVEMODE = LOW		0.10V_{DD}		V
		Sinking 1 mA, V_{DD}=3.0 V, GPIO_Px_CTRL DRIVEMODE = LOW		0.05V_{DD}		V
		Sinking 6 mA, V_{DD}=1.98 V, GPIO_Px_CTRL DRIVEMODE = STANDARD			0.30V_{DD}	V
		Sinking 6 mA, V_{DD}=3.0 V, GPIO_Px_CTRL DRIVEMODE = STANDARD			0.20V_{DD}	V
		Sinking 20 mA, V_{DD}=1.98 V, GPIO_Px_CTRL DRIVEMODE = HIGH			0.35V_{DD}	V
		Sinking 20 mA, V_{DD}=3.0 V, GPIO_Px_CTRL DRIVEMODE = HIGH			0.25V_{DD}	V
I_{IOLEAK}	Input leakage current	High Impedance IO connected to GROUND or Vdd		±0.1	±40	nA
R_{PU}	I/O pin pull-up resistor			40		kOhm
R_{PD}	I/O pin pull-down resistor			40		kOhm
R_{IOESD}	Internal ESD series resistor			200		Ohm
$t_{IOGLITCH}$	Pulse width of pulses to be removed		10		50	ns

Symbol	Parameter	Condition	Min	Typ	Max	Unit
	by the glitch suppression filter					
t_{IOOF}	Output fall time	GPIO_Px_CTRL DRIVEMODE = LOWEST and load capacitance C_L=12.5-25pF.	20+0.1C_L		250	ns
		GPIO_Px_CTRL DRIVEMODE = LOW and load capacitance C_L=350-600pF	20+0.1C_L		250	ns
V_{IOHYST}	I/O pin hysteresis (V_{IOTHR+} - V_{IOTHR-})	V_{DD} = 1.98 - 3.8 V	0.1V_{DD}			V

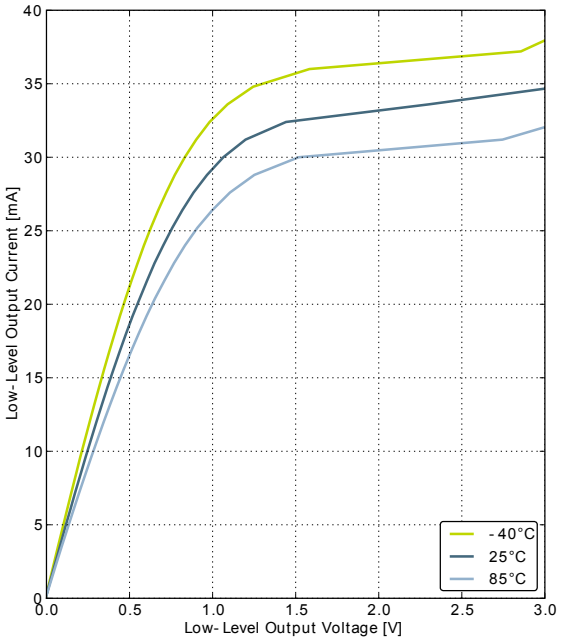
Figure 3.16. Typical Low-Level Output Current, 3V Supply Voltage



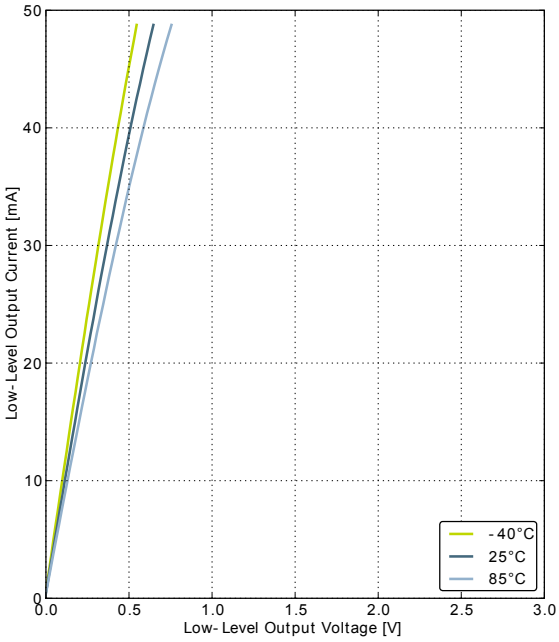
GPIO_Px_CTRL DRIVEMODE = LOWEST



GPIO_Px_CTRL DRIVEMODE = LOW

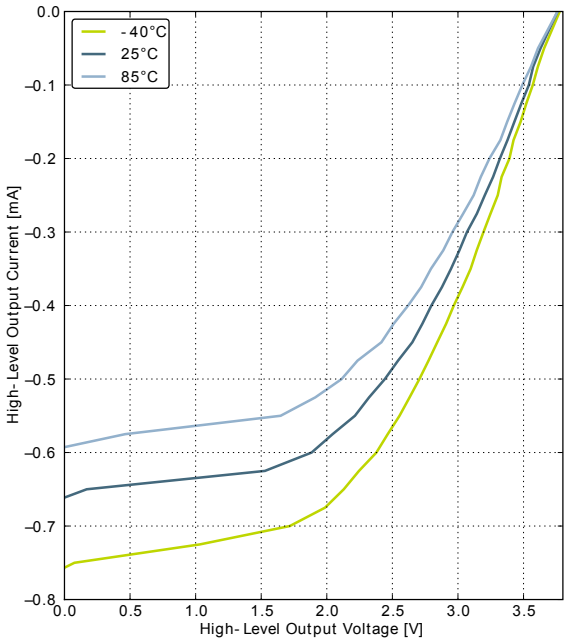


GPIO_Px_CTRL DRIVEMODE = STANDARD

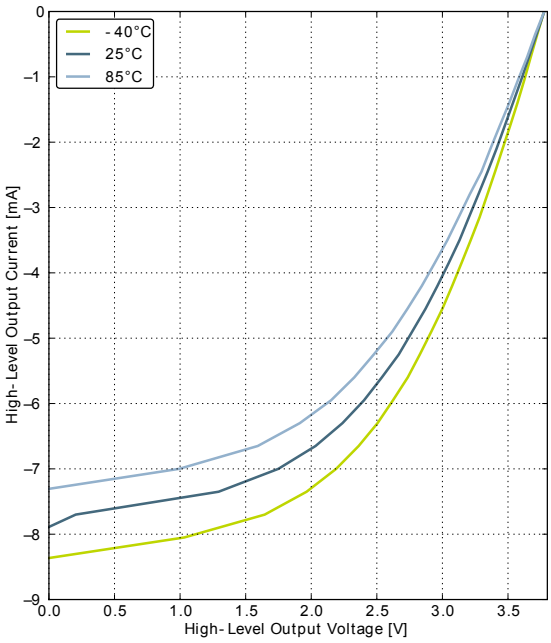


GPIO_Px_CTRL DRIVEMODE = HIGH

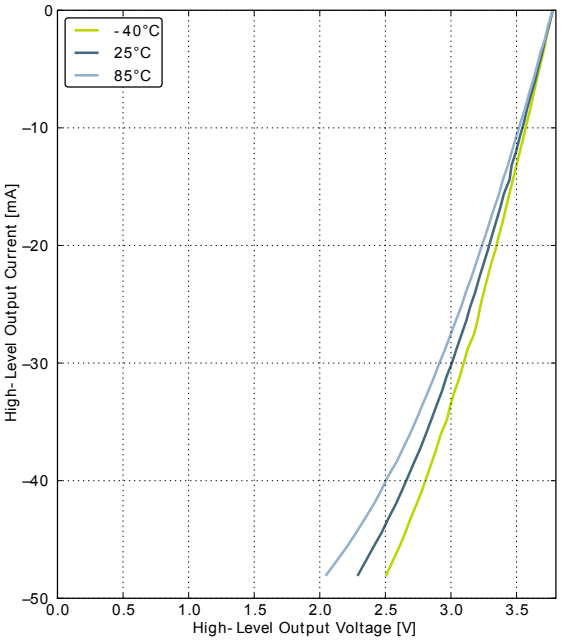
Figure 3.19. Typical High-Level Output Current, 3.8V Supply Voltage



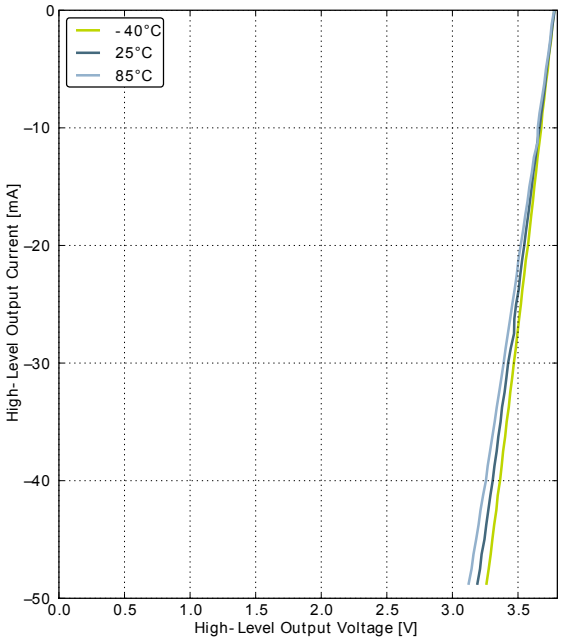
GPIO_Px_CTRL DRIVEMODE = LOWEST



GPIO_Px_CTRL DRIVEMODE = LOW



GPIO_Px_CTRL DRIVEMODE = STANDARD



GPIO_Px_CTRL DRIVEMODE = HIGH

3.9 Oscillators

3.9.1 LFXO

Table 3.8. LFXO

Symbol	Parameter	Condition	Min	Typ	Max	Unit
f_{LFXO}	Supported nominal crystal frequency			32.768		kHz
ESR_{LFXO}	Supported crystal equivalent series resistance (ESR)			30	120	kOhm
C_{LFXOL}	Supported crystal external load range		5		25	pF
I_{LFXO}	Current consumption for core and buffer after startup.	ESR=30 kOhm, C_L=10 pF, LFXOBOOST in CMU_CTRL is 1		190		nA
t_{LFXO}	Start- up time.	ESR=30 kOhm, C_L=10 pF, 40% - 60% duty cycle has been reached, LFXOBOOST in CMU_CTRL is 1		1100		ms

For safe startup of a given crystal, the Configurator tool in Simplicity Studio contains a tool to help users configure both load capacitance and software settings for using the LFXO. For details regarding the crystal configuration, the reader is referred to application note "AN0016 EFM32 Oscillator Design Consideration".

3.9.2 HFXO

Table 3.9. HFXO

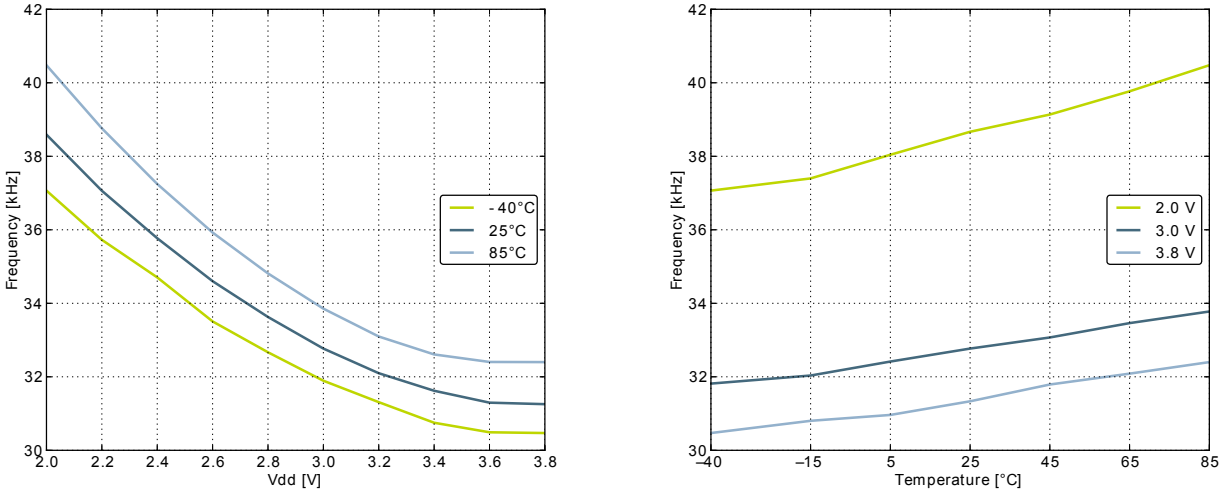
Symbol	Parameter	Condition	Min	Typ	Max	Unit
f_{HFXO}	Supported frequency, any mode		4		25	MHz
ESR_{HFXO}	Supported crystal equivalent series resistance (ESR)	Crystal frequency 25 MHz		30	100	Ohm
		Crystal frequency 4 MHz		400	1500	Ohm
g_{mHFXO}	The transconductance of the HFXO input transistor at crystal startup	HFXOBOOST in CMU_CTRL equals 0b11	20			mS
C_{HFXOL}	Supported crystal external load range		5		25	pF
I_{HFXO}	Current consumption for HFXO after startup	4 MHz: ESR=400 Ohm, C_L=20 pF, HFXOBOOST in CMU_CTRL equals 0b11		85		µA
		25 MHz: ESR=30 Ohm, C_L=10 pF, HFXOBOOST in CMU_CTRL equals 0b11		165		µA
t_{HFXO}	Startup time	25 MHz: ESR=30 Ohm, C_L=10 pF, HFXOBOOST in CMU_CTRL equals 0b11		785		µs

3.9.3 LFRCO

Table 3.10. LFRCO

Symbol	Parameter	Condition	Min	Typ	Max	Unit
f_{LFRCO}	Oscillation frequency , V_{DD}= 3.0 V, T_{AMB}=25°C		31.3	32.768	34.3	kHz
t_{LFRCO}	Startup time not including software calibration			150		µs
I_{LFRCO}	Current consumption			361	492	nA
$TUNESTEP_{LFRCO}$	Frequency step for LSB change in TUNING value			202		Hz

Figure 3.20. Calibrated LFRCO Frequency vs Temperature and Supply Voltage



3.9.4 HFRCO

Table 3.11. HFRCO

Symbol	Parameter	Condition	Min	Typ	Max	Unit
f_{HFRCO}	Oscillation frequency, V_{DD}= 3.0 V, T_{AMB}=25°C	24 MHz frequency band	23.28	24.0	24.72	MHz
		21 MHz frequency band	20.37	21.0	21.63	MHz
		14 MHz frequency band	13.58	14.0	14.42	MHz
		11 MHz frequency band	10.67	11.0	11.33	MHz
		7 MHz frequency band	6.40	6.60	6.80	MHz
		1 MHz frequency band	1.15	1.20	1.25	MHz
$t_{HFRCO\_settling}$	Settling time after start-up	f_{HFRCO} = 14 MHz		0.6		Cycles
I_{HFRCO}	Current consumption	f_{HFRCO} = 24 MHz		158	184	µA
		f_{HFRCO} = 21 MHz		143	175	µA
		f_{HFRCO} = 14 MHz		113	140	µA
		f_{HFRCO} = 11 MHz		101	125	µA
		f_{HFRCO} = 6.6 MHz		84	105	µA
		f_{HFRCO} = 1.2 MHz		27	40	µA
$TUNESTEP_{H-FRCO}$	Frequency step for LSB change in TUNING value	24 MHz frequency band		66.8[1]		kHz
		21 MHz frequency band		52.8[1]		kHz
		14 MHz frequency band		36.9[1]		kHz
		11 MHz frequency band		30.1[1]		kHz
		7 MHz frequency band		18.0[1]		kHz
		1 MHz frequency band		3.4		kHz

[1]The TUNING field in the CMU_HFRCOCTRL register may be used to adjust the HFRCO frequency. There is enough adjustment range to ensure that the frequency bands above 7 MHz will always have some overlap across supply voltage and temperature. By using a stable frequency reference such as the LFXO or HFXO, a firmware calibration routine can vary the TUNING bits and the frequency band to maintain the HFRCO frequency at any arbitrary value between 7 MHz and 21 MHz across operating conditions.

Figure 3.21. Calibrated HFRCO 1 MHz Band Frequency vs Supply Voltage and Temperature

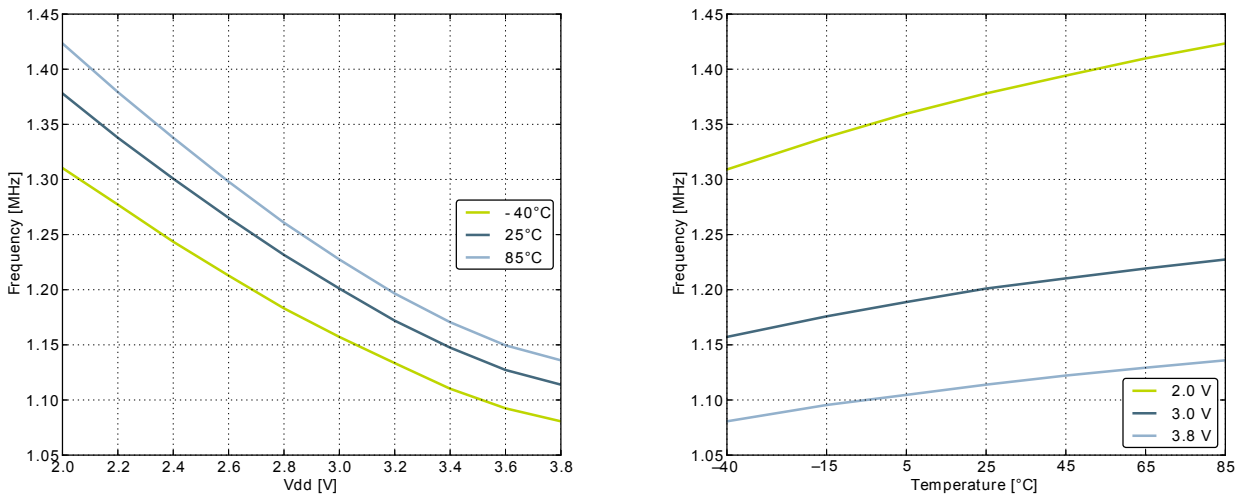


Table 3.18. I2C Fast-mode (Fm)

Symbol	Parameter	Min	Typ	Max	Unit
f_{SCL}	SCL clock frequency	0		400[1]	kHz
t_{LOW}	SCL clock low time	1.3			µs
t_{HIGH}	SCL clock high time	0.6			µs
$t_{SU,DAT}$	SDA set-up time	100			ns
$t_{HD,DAT}$	SDA hold time	8		900[2,3]	ns
$t_{SU,STA}$	Repeated START condition set-up time	0.6			µs
$t_{HD,STA}$	(Repeated) START condition hold time	0.6			µs
$t_{SU,STO}$	STOP condition set-up time	0.6			µs
t_{BUF}	Bus free time between a STOP and START condition	1.3			µs

[1]For the minimum HFPERCLK frequency required in Fast-mode, see the I2C chapter in the EFM32HG Reference Manual.
[2]The maximum SDA hold time ($t_{HD,DAT}$) needs to be met only when the device does not stretch the low time of SCL (t_{LOW}).
[3]When transmitting data, this number is guaranteed only when I2Cn_CLKDIV < ((900*10^{-9} [s] * $f_{HFPERCLK}$ [Hz]) - 5).

Table 3.19. I2C Fast-mode Plus (Fm+)

Symbol	Parameter	Min	Typ	Max	Unit
f_{SCL}	SCL clock frequency	0		1000[1]	kHz
t_{LOW}	SCL clock low time	0.5			µs
t_{HIGH}	SCL clock high time	0.26			µs
$t_{SU,DAT}$	SDA set-up time	50			ns
$t_{HD,DAT}$	SDA hold time	8			ns
$t_{SU,STA}$	Repeated START condition set-up time	0.26			µs
$t_{HD,STA}$	(Repeated) START condition hold time	0.26			µs
$t_{SU,STO}$	STOP condition set-up time	0.26			µs
t_{BUF}	Bus free time between a STOP and START condition	0.5			µs

[1]For the minimum HFPERCLK frequency required in Fast-mode Plus, see the I2C chapter in the EFM32HG Reference Manual.

3.13 Digital Peripherals

Table 3.20. Digital Peripherals

Symbol	Parameter	Condition	Min	Typ	Max	Unit
I_{USART}	USART current	USART idle current, clock enabled		7.5		µA/MHz
I_{LEUART}	LEUART current	LEUART idle current, clock enabled		150		nA
I_{I2C}	I2C current	I2C idle current, clock enabled		6.25		µA/MHz
I_{TIMER}	TIMER current	TIMER_0 idle current, clock enabled		8.75		µA/MHz
I_{PCNT}	PCNT current	PCNT idle current, clock enabled		100		nA
I_{RTC}	RTC current	RTC idle current, clock enabled		100		nA

4.2 Alternate Functionality Pinout

A wide selection of alternate functionality is available for multiplexing to various pins. This is shown in Table 4.2 (p. 40). The table shows the name of the alternate functionality in the first column, followed by columns showing the possible LOCATION bitfield settings.

Note

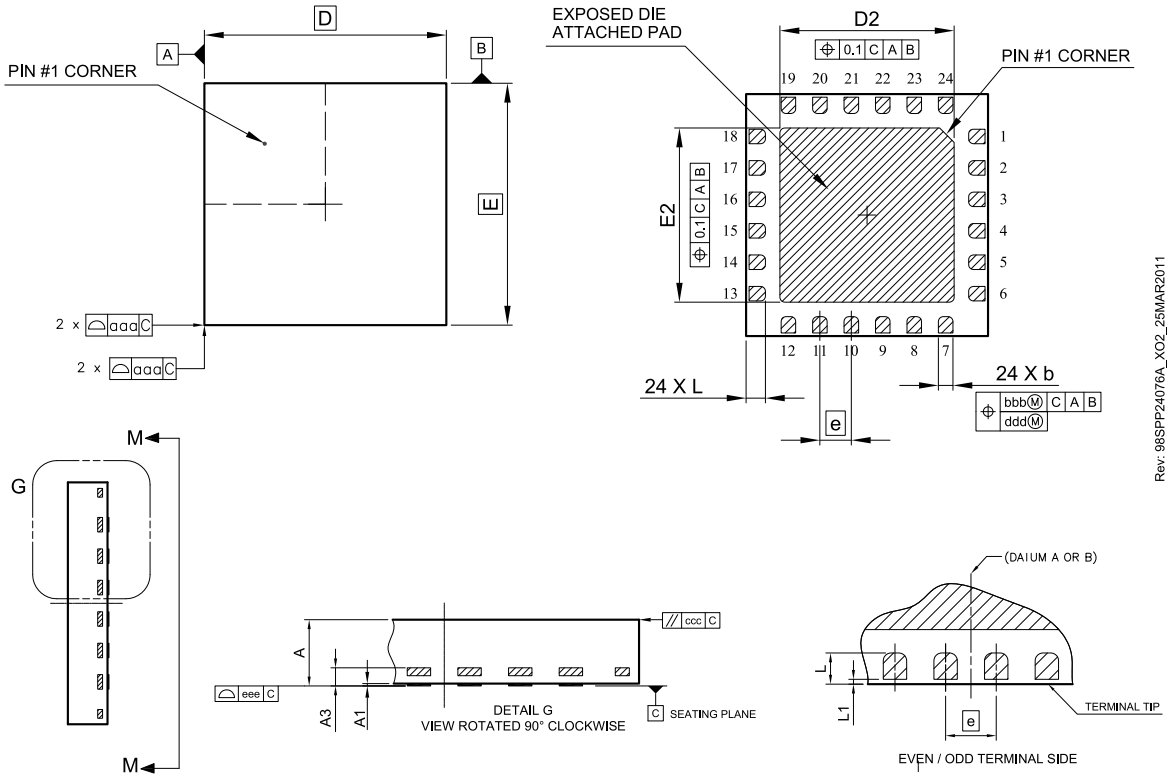
Some functionality, such as analog interfaces, do not have alternate settings or a LOCATION bitfield. In these cases, the pinout is shown in the column corresponding to LOCATION 0.

Table 4.2. Alternate functionality overview

Alternate	LOCATION							
Functionality	0	1	2	3	4	5	6	Description
ACMP0_CH0	PC0							Analog comparator ACMP0, channel 0.
ACMP0_CH1	PC1							Analog comparator ACMP0, channel 1.
ACMP0_O	PE13		PD6	PB11				Analog comparator ACMP0, digital output.
BOOT_RX	PF1							Bootloader RX.
BOOT_TX	PF0							Bootloader TX.
CMU_CLK0			PD7	PF2				Clock Management Unit, clock output number 0.
CMU_CLK1			PE12	PB11				Clock Management Unit, clock output number 1.
DBG_SWCLK	PF0							Debug-interface Serial Wire clock input. Note that this function is enabled to pin out of reset, and has a built-in pull down.
DBG_SWDIO	PF1							Debug-interface Serial Wire data input / output. Note that this function is enabled to pin out of reset, and has a built-in pull up.
GPIO_EM4WU0	PA0							Pin can be used to wake the system up from EM4
GPIO_EM4WU3	PF1							Pin can be used to wake the system up from EM4
GPIO_EM4WU4	PF2							Pin can be used to wake the system up from EM4
GPIO_EM4WU5	PE13							Pin can be used to wake the system up from EM4
HFXTAL_N	PB14							High Frequency Crystal negative pin. Also used as external optional clock input pin.
HFXTAL_P	PB13							High Frequency Crystal positive pin.
I2C0_SCL		PD7			PC1	PF1	PE13	I2C0 Serial Clock Line input / output.
I2C0_SDA	PA0	PD6			PC0	PF0	PE12	I2C0 Serial Data input / output.
LEU0_RX		PB14		PF1	PA0	PC15		LEUART0 Receive input.
LEU0_TX		PB13		PF0	PF2	PC14		LEUART0 Transmit output. Also used as receive input in half duplex communication.
LFXTAL_N	PB8							Low Frequency Crystal (typically 32.768 kHz) negative pin. Also used as an optional external clock input pin.
LFXTAL_P	PB7							Low Frequency Crystal (typically 32.768 kHz) positive pin.
PCNT0_S0IN			PC0	PD6	PA0			Pulse Counter PCNT0 input number 0.
PCNT0_S1IN	PC14		PC1	PD7	PB11			Pulse Counter PCNT0 input number 1.
PRS_CH0	PA0		PC14	PF2				Peripheral Reflex System PRS, channel 0.
PRS_CH1			PC15	PE12				Peripheral Reflex System PRS, channel 1.
PRS_CH2	PC0			PE13				Peripheral Reflex System PRS, channel 2.

4.4 QFN24 Package

Figure 4.2. QFN24



Note:

1. Dimensioning & tolerancing confirm to ASME Y14.5M-1994.
2. All dimensions are in millimeters. Angles are in degrees.
3. Dimension 'b' applies to metallized terminal and is measured between 0.25 mm and 0.30 mm from the terminal tip. Dimension L1 represents terminal full back from package edge up to 0.1 mm is acceptable.
4. Coplanarity applies to the exposed heat slug as well as the terminal.
5. Radius on terminal is optional

Table 4.4. QFN24 (Dimensions in mm)

Symbol	A	A1	A3	b	D	E	D2	E2	e	L	L1	aaa	bbb	ccc	ddd	eee
Min	0.80	0.00	0.203 REF	0.25	5.00 BSC	5.00 BSC	3.50	3.50	0.65 BSC	0.35	0.00	0.10	0.10	0.10	0.05	0.08
Nom	0.85	-		0.30			3.60	3.60		0.40						
Max	0.90	0.05		0.35			3.70	3.70		0.45	0.10					

The QFN24 package uses matte-Sn post plated leadframe.

All EFM32 packages are RoHS compliant and free of Bromine (Br) and Antimony (Sb).

For additional Quality and Environmental information, please see:
http://www.silabs.com/support/quality/pages/default.aspx

5 PCB Layout and Soldering

5.1 Recommended PCB Layout

Figure 5.1. QFN24 PCB Land Pattern

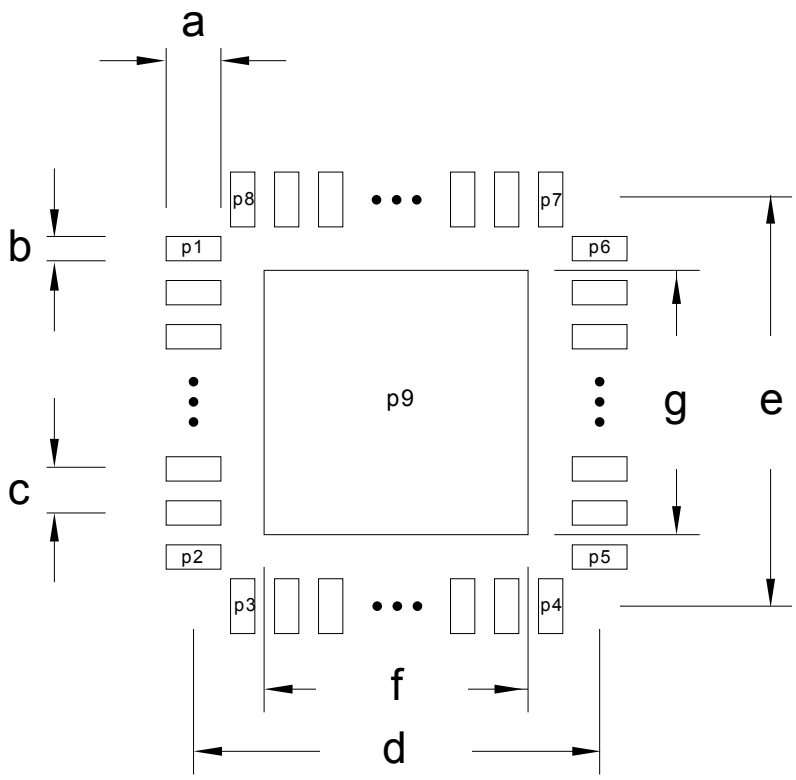


Table 5.1. QFN24 PCB Land Pattern Dimensions (Dimensions in mm)

Symbol	Dim. (mm)	Symbol	Pin number	Symbol	Pin number
a	0.80	P1	1	P8	24
b	0.30	P2	6	P9	25
c	0.65	P3	7	-	-
d	5.00	P4	12	-	-
e	5.00	P5	13	-	-
f	3.60	P6	18	-	-
g	3.60	P7	19	-	-

Figure 5.2. QFN24 PCB Solder Mask

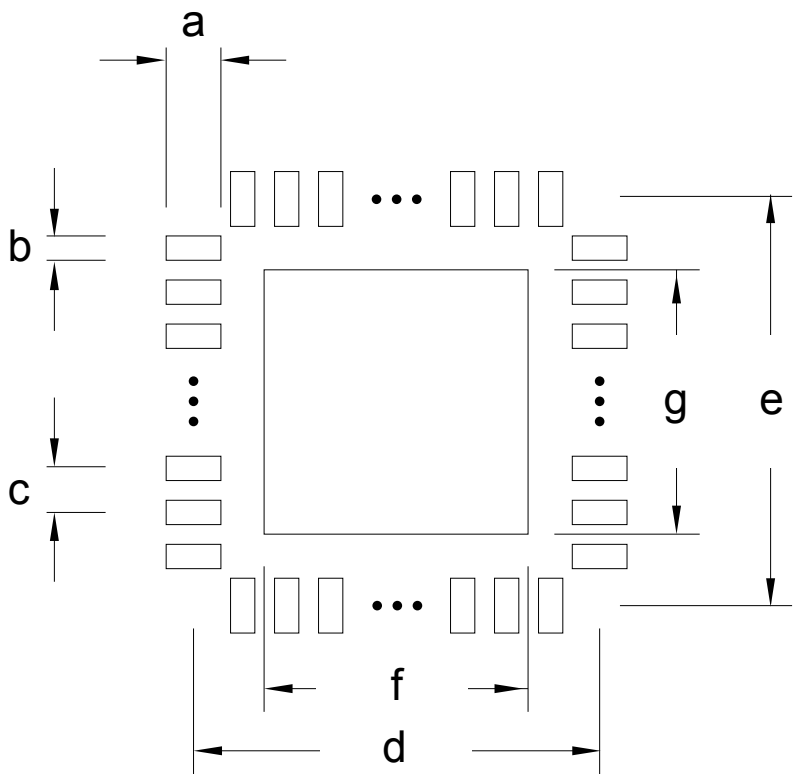


Table 5.2. QFN24 PCB Solder Mask Dimensions (Dimensions in mm)

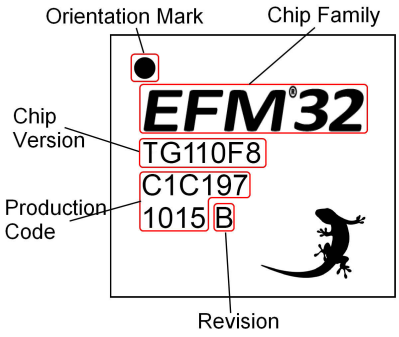
Symbol	Dim. (mm)	Symbol	Dim. (mm)
a	0.92	e	5.00
b	0.42	f	3.72
c	0.65	g	3.72
d	5.00	-	-

6 Chip Marking, Revision and Errata

6.1 Chip Marking

In the illustration below package fields and position are shown.

Figure 6.1. Example Chip Marking (top view)



6.2 Revision

The revision of a chip can be determined from the "Revision" field in Figure 6.1 (p. 46) .

6.3 Errata

Please see the errata document for EFM32HG108 for description and resolution of device erratas. This document is available in Simplicity Studio and online at:
http://www.silabs.com/support/pages/document-library.aspx?p=MCUs--32-bit

7.4 Revision 0.20

December 11th, 2014

Preliminary Release.

List of Tables