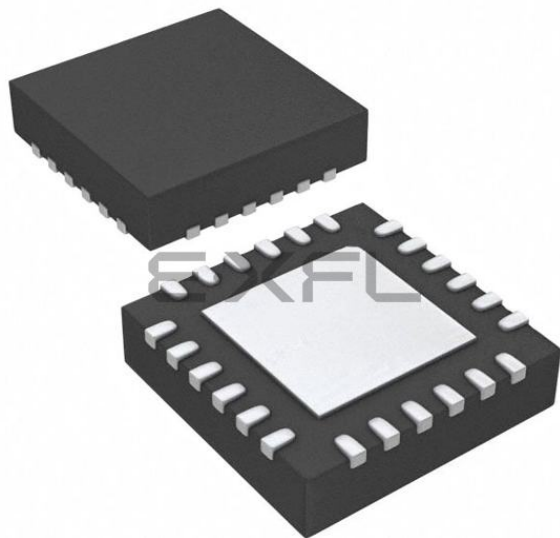




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Details

Product Status	Discontinued at Digi-Key
Core Processor	ARM® Cortex®-M0+
Core Size	32-Bit Single-Core
Speed	25MHz
Connectivity	I ² C, IrDA, SmartCard, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, I ² S, POR, PWM, WDT
Number of I/O	17
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	1.98V ~ 3.8V
Data Converters	A/D 4x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	24-VQFN Exposed Pad
Supplier Device Package	24-QFN (5x5)
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/efm32hg108f32g-b-qfn24r

2.2 Configuration Summary

The features of the EFM32HG108 is a subset of the feature set described in the EFM32HG Reference Manual. Table 2.1 (p. 6) describes device specific implementation of the features.

Table 2.1. Configuration Summary

Module	Configuration	Pin Connections
Cortex-M0+	Full configuration	NA
DBG	Full configuration	DBG_SWCLK, DBG_SWDIO,
MSC	Full configuration	NA
DMA	Full configuration	NA
RMU	Full configuration	NA
EMU	Full configuration	NA
CMU	Full configuration	CMU_OUT0, CMU_OUT1
WDOG	Full configuration	NA
PRS	Full configuration	NA
I2C0	Full configuration	I2C0_SDA, I2C0_SCL
USART0	Full configuration with IrDA and I2S	US0_TX, US0_RX, US0_CLK, US0_CS
USART1	Full configuration with I2S and IrDA	US1_TX, US1_RX, US1_CLK, US1_CS
LEUART0	Full configuration	LEU0_TX, LEU0_RX
TIMER0	Full configuration with DTI	TIM0_CC[2:0], TIM0_CDTI[2:0]
TIMER1	Full configuration	TIM1_CC[2:0]
TIMER2	Full configuration	TIM2_CC[2:0]
RTC	Full configuration	NA
PCNT0	Full configuration, 16-bit count register	PCNT0_S[1:0]
ACMP0	Full configuration	ACMP0_CH[1:0], ACMP0_O
VCMP	Full configuration	NA
GPIO	17 pins	Available pins are shown in Table 4.3 (p. 41)

2.3 Memory Map

The *EFM32HG108* memory map is shown in Figure 2.2 (p. 7), with RAM and Flash sizes for the largest memory configuration.

3 Electrical Characteristics

3.1 Test Conditions

3.1.1 Typical Values

The typical data are based on $T_{AMB}=25^{\circ}\text{C}$ and $V_{DD}=3.0\text{ V}$, as defined in Table 3.2 (p. 8), unless otherwise specified.

3.1.2 Minimum and Maximum Values

The minimum and maximum values represent the worst conditions of ambient temperature, supply voltage and frequencies, as defined in Table 3.2 (p. 8), unless otherwise specified.

3.2 Absolute Maximum Ratings

The absolute maximum ratings are stress ratings, and functional operation under such conditions are not guaranteed. Stress beyond the limits specified in Table 3.1 (p. 8) may affect the device reliability or cause permanent damage to the device. Functional operating conditions are given in Table 3.2 (p. 8).

Table 3.1. Absolute Maximum Ratings

Symbol	Parameter	Condition	Min	Typ	Max	Unit
T_{STG}	Storage temperature range		-40		150 ¹	$^{\circ}\text{C}$
T_S	Maximum soldering temperature	Latest IPC/JEDEC J-STD-020 Standard			260	$^{\circ}\text{C}$
V_{DDMAX}	External main supply voltage		0		3.8	V
V_{IOPIN}	Voltage on any I/O pin		-0.3		$V_{DD}+0.3$	V

¹Based on programmed devices tested for 10000 hours at 150°C . Storage temperature affects retention of preprogrammed calibration values stored in flash. Please refer to the Flash section in the Electrical Characteristics for information on flash data retention for different temperatures.

3.3 General Operating Conditions

3.3.1 General Operating Conditions

Table 3.2. General Operating Conditions

Symbol	Parameter	Min	Typ	Max	Unit
T_{AMB}	Ambient temperature range	-40		85	$^{\circ}\text{C}$
V_{DDOP}	Operating supply voltage	1.98		3.8	V
f_{APB}	Internal APB clock frequency			25	MHz
f_{AHB}	Internal AHB clock frequency			25	MHz

Symbol	Parameter	Condition	Min	Typ	Max	Unit
I _{EM1}	EM1 current	24 MHz HFXO, all peripheral clocks disabled, V _{DD} = 3.0 V, T _{AMB} =25°C		64	68	μA/ MHz
		24 MHz HFXO, all peripheral clocks disabled, V _{DD} = 3.0 V, T _{AMB} =85°C		67	71	μA/ MHz
		24 MHz USHFRCO, all peripheral clocks disabled, V _{DD} = 3.0 V, T _{AMB} =25°C		85	91	μA/ MHz
		24 MHz USHFRCO, all peripheral clocks disabled, V _{DD} = 3.0 V, T _{AMB} =85°C		86	92	μA/ MHz
		24 MHz HFRCO, all peripheral clocks disabled, V _{DD} = 3.0 V, T _{AMB} =25°C		51	55	μA/ MHz
		24 MHz HFRCO, all peripheral clocks disabled, V _{DD} = 3.0 V, T _{AMB} =85°C		52	56	μA/ MHz
		21 MHz HFRCO, all peripheral clocks disabled, V _{DD} = 3.0 V, T _{AMB} =25°C		53	57	μA/ MHz
		21 MHz HFRCO, all peripheral clocks disabled, V _{DD} = 3.0 V, T _{AMB} =85°C		54	58	μA/ MHz
		14 MHz HFRCO, all peripheral clocks disabled, V _{DD} = 3.0 V, T _{AMB} =25°C		56	59	μA/ MHz
		14 MHz HFRCO, all peripheral clocks disabled, V _{DD} = 3.0 V, T _{AMB} =85°C		57	61	μA/ MHz
		11 MHz HFRCO, all peripheral clocks disabled, V _{DD} = 3.0 V, T _{AMB} =25°C		58	61	μA/ MHz
		11 MHz HFRCO, all peripheral clocks disabled, V _{DD} = 3.0 V, T _{AMB} =85°C		59	63	μA/ MHz
		6.6 MHz HFRCO, all peripheral clocks disabled, V _{DD} = 3.0 V, T _{AMB} =25°C		64	68	μA/ MHz
		6.6 MHz HFRCO, all peripheral clocks disabled, V _{DD} = 3.0 V, T _{AMB} =85°C		67	71	μA/ MHz
		1.2 MHz HFRCO. all peripheral clocks disabled, V _{DD} = 3.0 V, T _{AMB} =25°C		106	114	μA/ MHz
		1.2 MHz HFRCO. all peripheral clocks disabled, V _{DD} = 3.0 V, T _{AMB} =85°C		114	126	μA/ MHz
I _{EM2}	EM2 current	EM2 current with RTC prescaled to 1 Hz, 32.768 kHz LFRCO, V _{DD} = 3.0 V, T _{AMB} =25°C		0.9	1.35	μA

Symbol	Parameter	Condition	Min	Typ	Max	Unit
		EM2 current with RTC prescaled to 1 Hz, 32.768 kHz LFRCO, $V_{DD}=3.0\text{ V}$, $T_{AMB}=85^{\circ}\text{C}$		1.6	3.50	μA
I_{EM3}	EM3 current	EM3 current (ULFRCO enabled, LFRCO/LFXO disabled), $V_{DD}=3.0\text{ V}$, $T_{AMB}=25^{\circ}\text{C}$		0.6	0.90	μA
		EM3 current (ULFRCO enabled, LFRCO/LFXO disabled), $V_{DD}=3.0\text{ V}$, $T_{AMB}=85^{\circ}\text{C}$		1.2	2.65	μA
I_{EM4}	EM4 current	$V_{DD}=3.0\text{ V}$, $T_{AMB}=25^{\circ}\text{C}$		0.02	0.035	μA
		$V_{DD}=3.0\text{ V}$, $T_{AMB}=85^{\circ}\text{C}$		0.18	0.480	μA

3.4.1 EM0 Current Consumption

Figure 3.1. EM0 Current consumption while executing prime number calculation code from flash with HFRCO running at 24 MHz

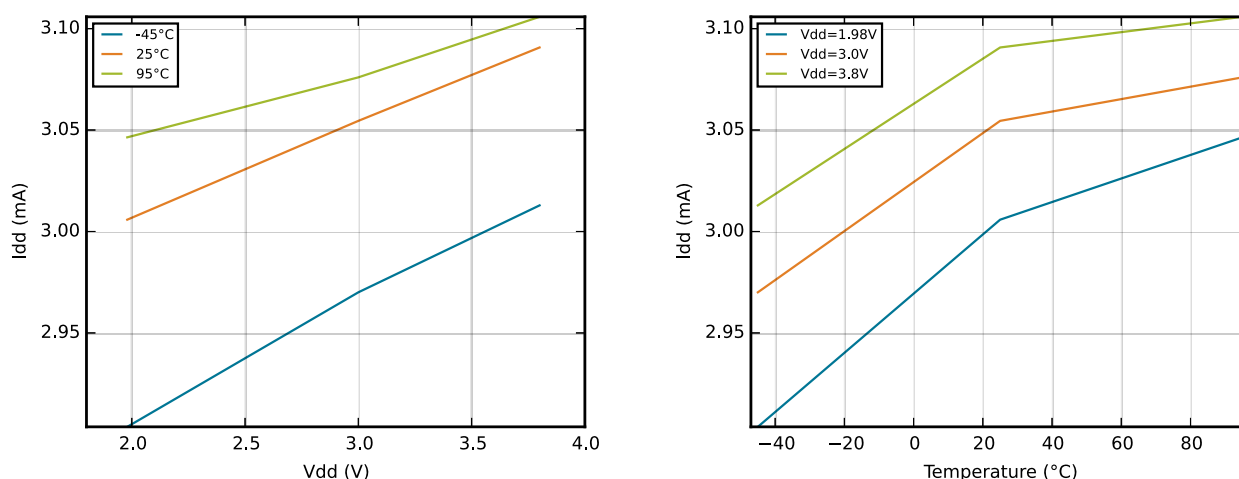


Figure 3.2. EM0 Current consumption while executing prime number calculation code from flash with HFRCO running at 21 MHz

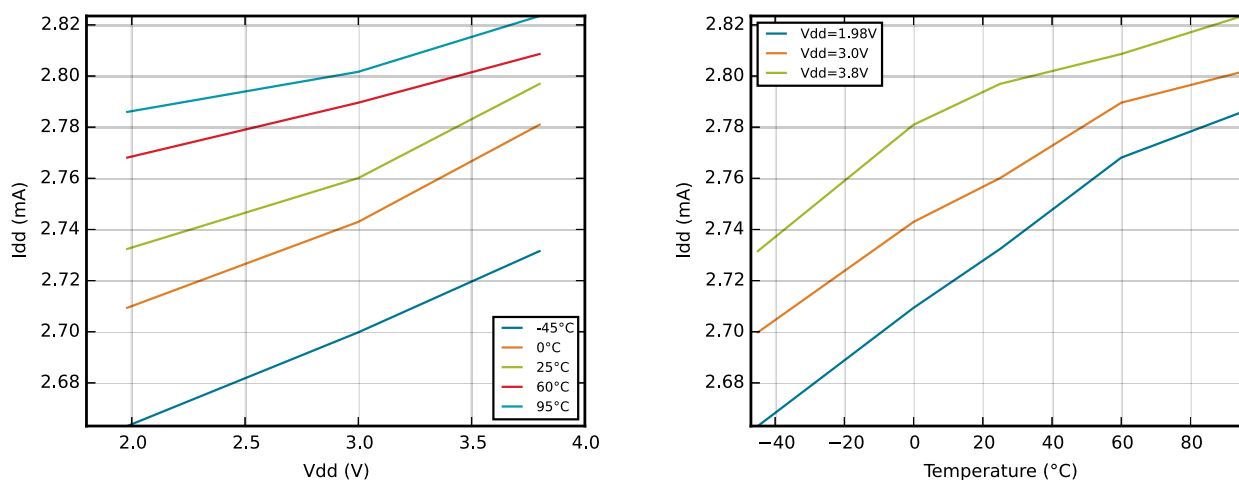


Figure 3.7. EM1 Current consumption with all peripheral clocks disabled and HFRCO running at 21 MHz

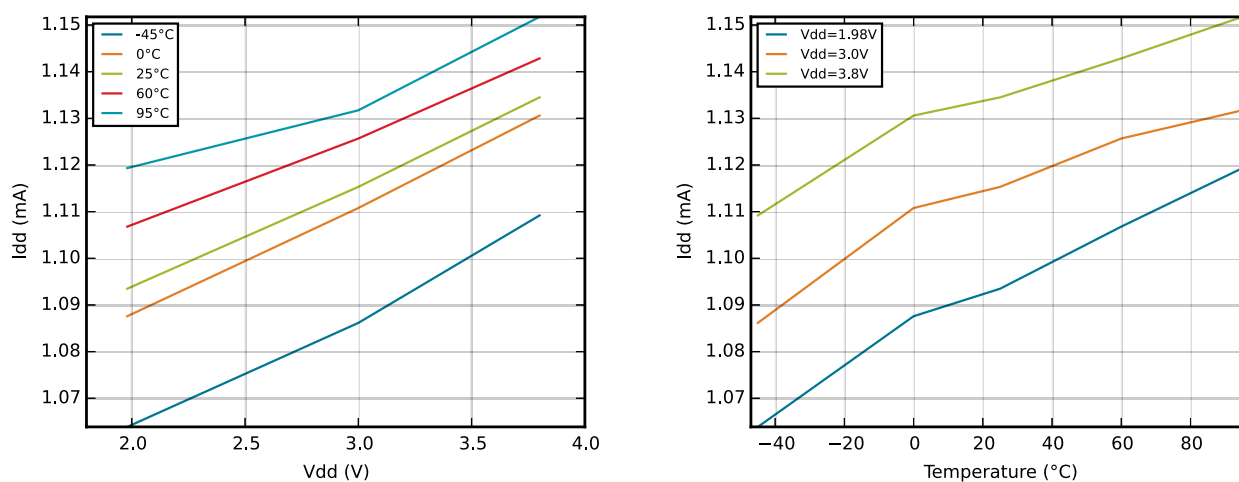
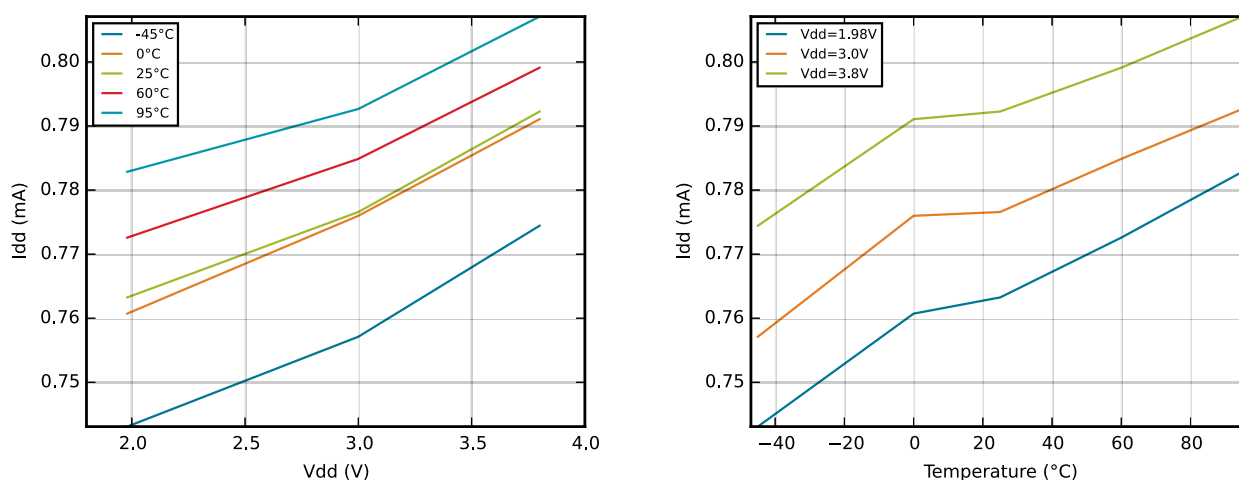
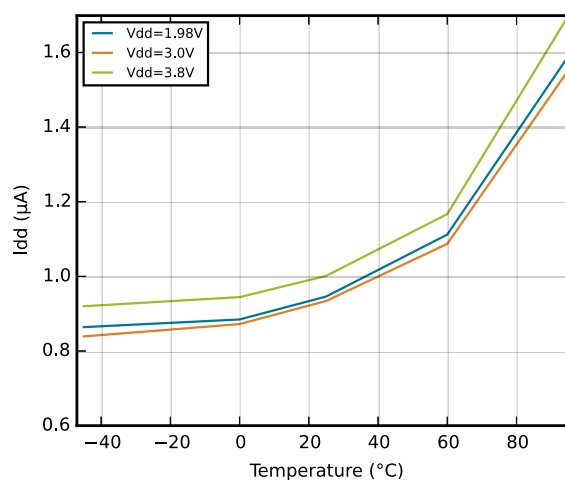
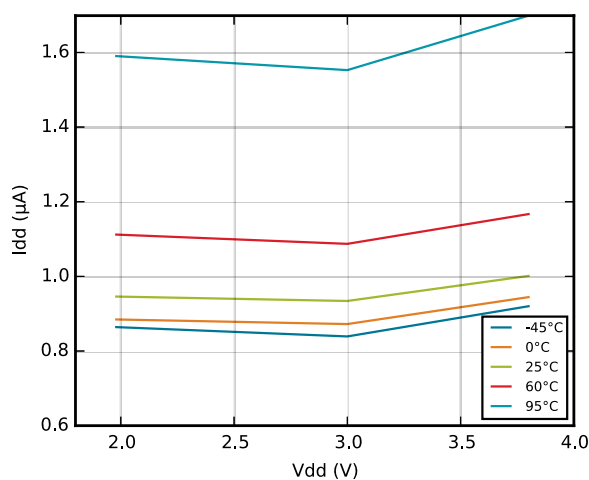


Figure 3.8. EM1 Current consumption with all peripheral clocks disabled and HFRCO running at 14 MHz



3.4.3 EM2 Current Consumption

Figure 3.11. EM2 current consumption. RTC prescaled to 1kHz, 32.768 kHz LFRCO.



3.4.4 EM3 Current Consumption

Figure 3.12. EM3 current consumption.

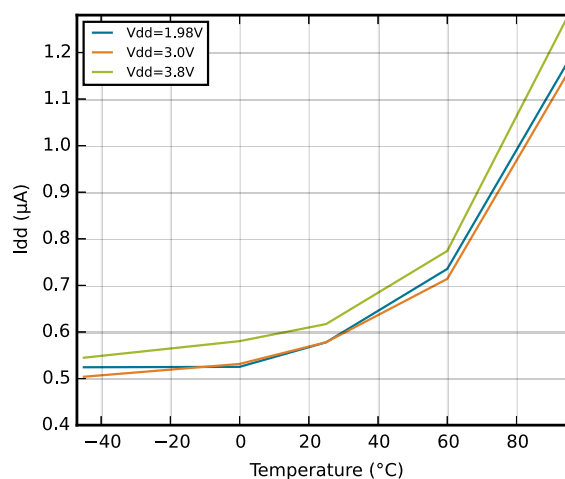
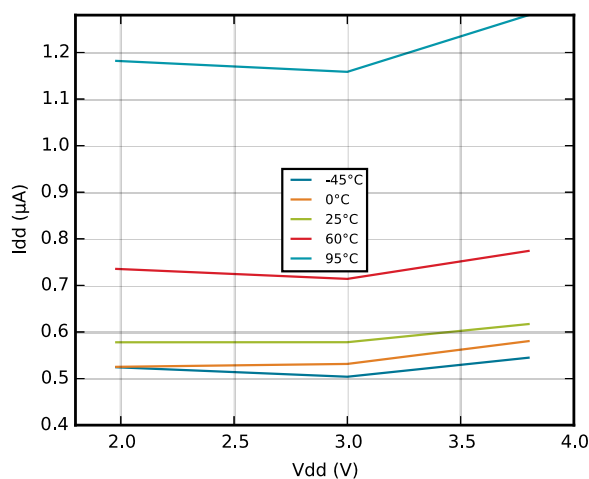


Table 3.5. Power Management

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V _{BODextthr-}	BOD threshold on falling external supply voltage	EM0	1.74		1.96	V
		EM2	1.71	1.86	1.98	V
V _{BODextthr+}	BOD threshold on rising external supply voltage			1.85		V
t _{RESET}	Delay from reset is released until program execution starts	Applies to Power-on Reset, Brown-out Reset and pin reset.		163		μs
C _{DECOUPLE}	Voltage regulator decoupling capacitor.	X5R capacitor recommended. Apply between DECOUPLE pin and GROUND		1		μF

3.7 Flash

Table 3.6. Flash

Symbol	Parameter	Condition	Min	Typ	Max	Unit
EC _{FLASH}	Flash erase cycles before failure		20000			cycles
RET _{FLASH}	Flash data retention	T _{AMB} <150°C	10000			h
		T _{AMB} <85°C	10			years
		T _{AMB} <70°C	20			years
t _{W_PROG}	Word (32-bit) programming time		20			μs
t _{P_ERASE}	Page erase time		20	20.4	20.8	ms
t _{D_ERASE}	Device erase time		40	40.8	41.6	ms
I _{ERASE}	Erase current				7 ¹	mA
I _{WRITE}	Write current				7 ¹	mA
V _{FLASH}	Supply voltage during flash erase and write		1.98		3.8	V

¹Measured at 25°C

3.8 General Purpose Input Output

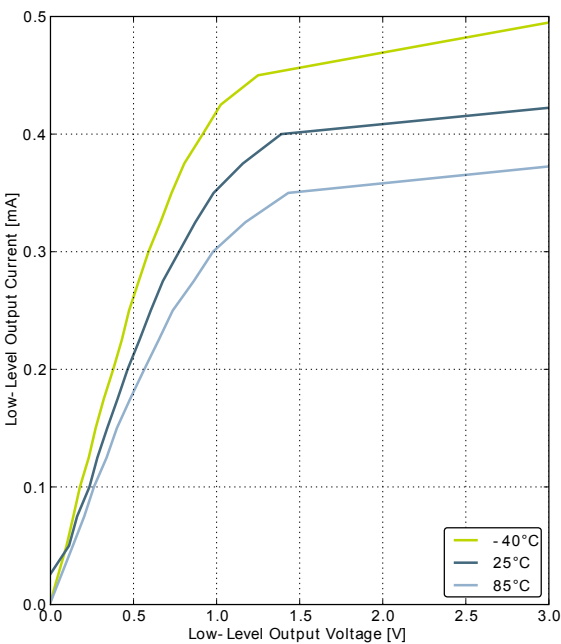
Table 3.7. GPIO

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V _{IOIL}	Input low voltage				0.30V _{DD}	V
V _{IOIH}	Input high voltage		0.70V _{DD}			V
V _{IOOH}	Output high voltage (Production test condition = 3.0V, DRIVEMODE = STANDARD)	Sourcing 0.1 mA, V _{DD} =1.98 V, GPIO_Px_CTRL DRIVEMODE = LOWEST		0.80V _{DD}		V
		Sourcing 0.1 mA, V _{DD} =3.0 V, GPIO_Px_CTRL DRIVEMODE = LOWEST		0.90V _{DD}		V

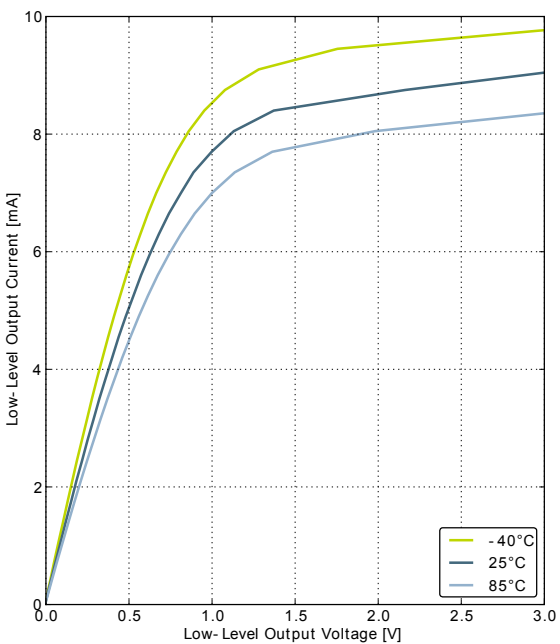
Symbol	Parameter	Condition	Min	Typ	Max	Unit
		Sourcing 1 mA, $V_{DD}=1.98$ V, GPIO_Px_CTRL DRIVEMODE = LOW		$0.85V_{DD}$		V
		Sourcing 1 mA, $V_{DD}=3.0$ V, GPIO_Px_CTRL DRIVEMODE = LOW		$0.90V_{DD}$		V
		Sourcing 6 mA, $V_{DD}=1.98$ V, GPIO_Px_CTRL DRIVEMODE = STANDARD	$0.75V_{DD}$			V
		Sourcing 6 mA, $V_{DD}=3.0$ V, GPIO_Px_CTRL DRIVEMODE = STANDARD	$0.85V_{DD}$			V
		Sourcing 20 mA, $V_{DD}=1.98$ V, GPIO_Px_CTRL DRIVEMODE = HIGH	$0.60V_{DD}$			V
		Sourcing 20 mA, $V_{DD}=3.0$ V, GPIO_Px_CTRL DRIVEMODE = HIGH	$0.80V_{DD}$			V
V_{IOOL}	Output low voltage (Production test condition = 3.0V, DRIVEMODE = STANDARD)	Sinking 0.1 mA, $V_{DD}=1.98$ V, GPIO_Px_CTRL DRIVEMODE = LOWEST		$0.20V_{DD}$		V
		Sinking 0.1 mA, $V_{DD}=3.0$ V, GPIO_Px_CTRL DRIVEMODE = LOWEST		$0.10V_{DD}$		V
		Sinking 1 mA, $V_{DD}=1.98$ V, GPIO_Px_CTRL DRIVEMODE = LOW		$0.10V_{DD}$		V
		Sinking 1 mA, $V_{DD}=3.0$ V, GPIO_Px_CTRL DRIVEMODE = LOW		$0.05V_{DD}$		V
		Sinking 6 mA, $V_{DD}=1.98$ V, GPIO_Px_CTRL DRIVEMODE = STANDARD			$0.30V_{DD}$	V
		Sinking 6 mA, $V_{DD}=3.0$ V, GPIO_Px_CTRL DRIVEMODE = STANDARD			$0.20V_{DD}$	V
		Sinking 20 mA, $V_{DD}=1.98$ V, GPIO_Px_CTRL DRIVEMODE = HIGH			$0.35V_{DD}$	V
		Sinking 20 mA, $V_{DD}=3.0$ V, GPIO_Px_CTRL DRIVEMODE = HIGH			$0.25V_{DD}$	V
I_{IOLEAK}	Input leakage current	High Impedance IO connected to GROUND or Vdd		± 0.1	± 40	nA
R_{PU}	I/O pin pull-up resistor			40		kOhm
R_{PD}	I/O pin pull-down resistor			40		kOhm
R_{IOESD}	Internal ESD series resistor			200		Ohm
$t_{IOGLITCH}$	Pulse width of pulses to be removed		10		50	ns

Symbol	Parameter	Condition	Min	Typ	Max	Unit
	by the glitch suppression filter					
t_{IOOF}	Output fall time	GPIO_Px_CTRL DRIVEMODE = LOWEST and load capacitance $C_L=12.5-25pF$.	$20+0.1C_L$		250	ns
		GPIO_Px_CTRL DRIVEMODE = LOW and load capacitance $C_L=350-600pF$	$20+0.1C_L$		250	ns
V_{IOHYST}	I/O pin hysteresis ($V_{IOTHR+} - V_{IOTHR-}$)	$V_{DD} = 1.98 - 3.8 V$	$0.1V_{DD}$			V

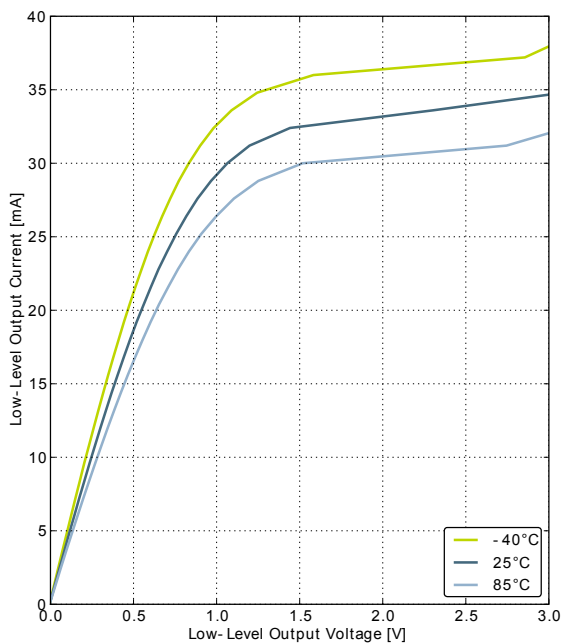
Figure 3.16. Typical Low-Level Output Current, 3V Supply Voltage



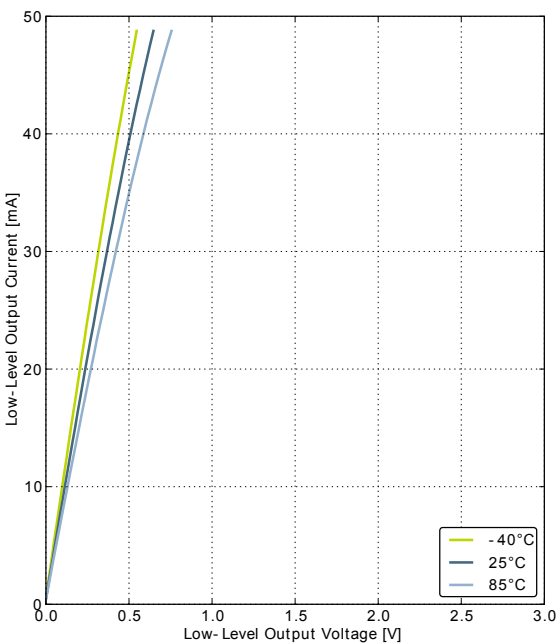
GPIO_Px_CTRL DRIVEMODE = LOWEST



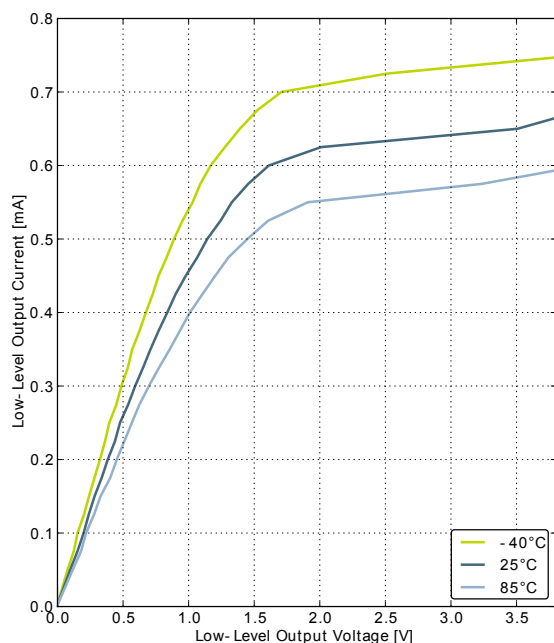
GPIO_Px_CTRL DRIVEMODE = LOW



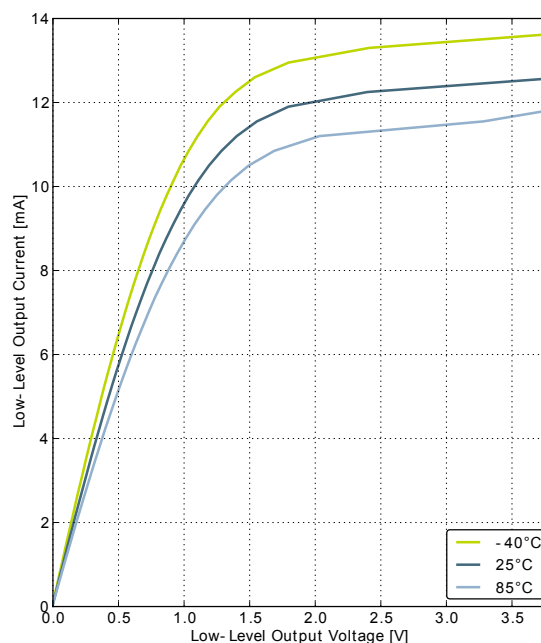
GPIO_Px_CTRL DRIVEMODE = STANDARD



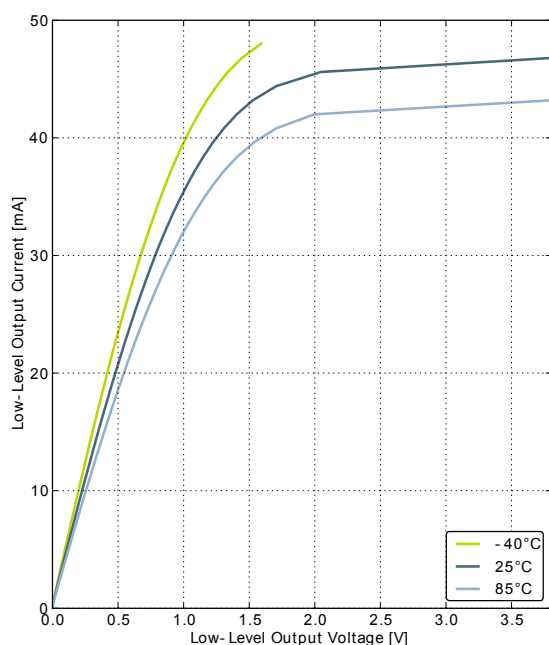
GPIO_Px_CTRL DRIVEMODE = HIGH

Figure 3.18. Typical Low-Level Output Current, 3.8V Supply Voltage

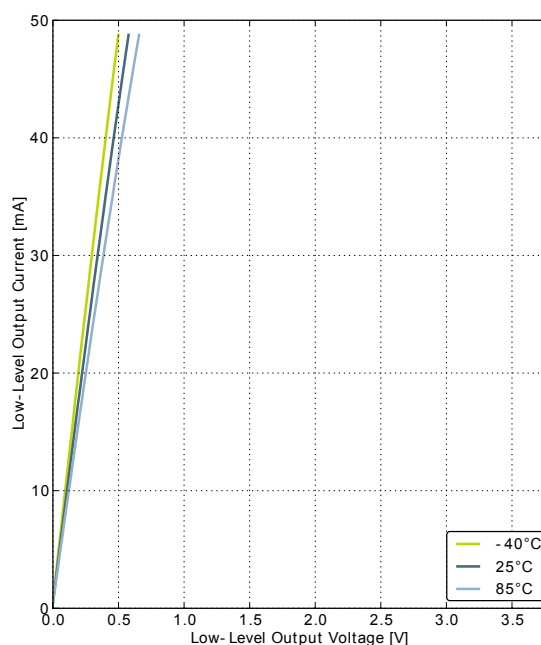
GPIO_Px_CTRL DRIVEMODE = LOWEST



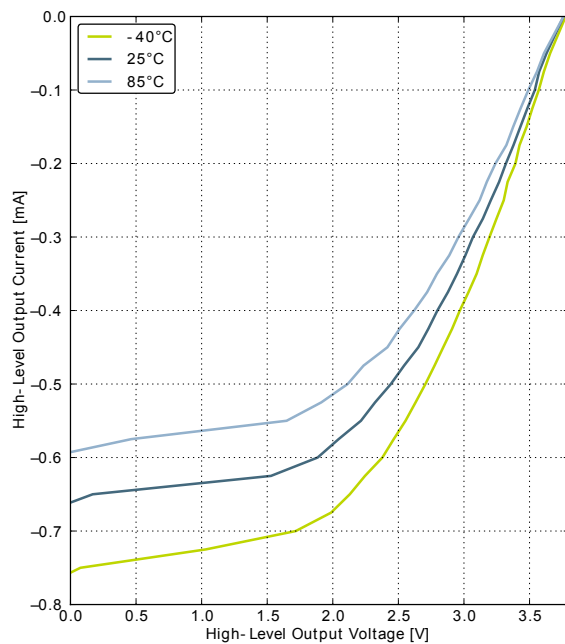
GPIO_Px_CTRL DRIVEMODE = LOW



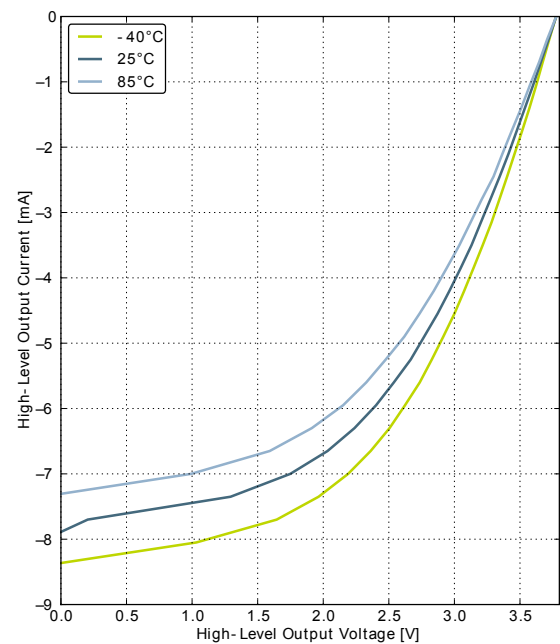
GPIO_Px_CTRL DRIVEMODE = STANDARD



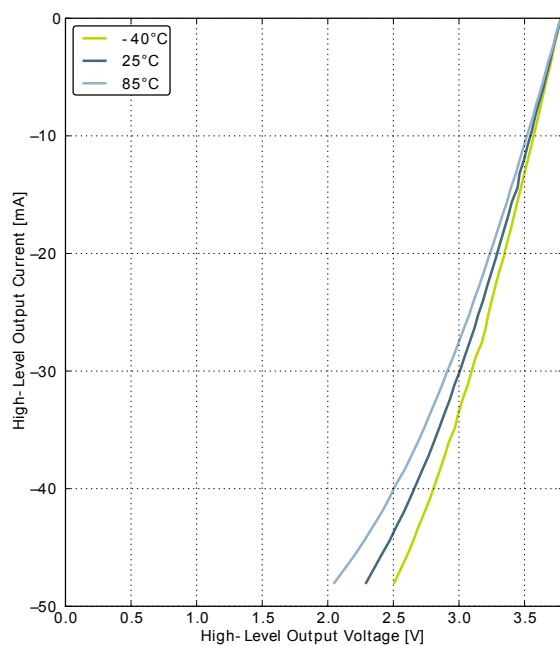
GPIO_Px_CTRL DRIVEMODE = HIGH

Figure 3.19. Typical High-Level Output Current, 3.8V Supply Voltage

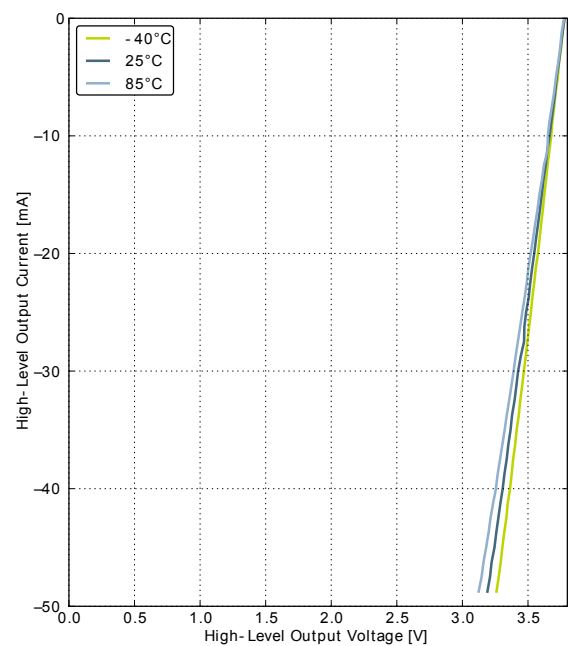
GPIO_Px_CTRL DRIVEMODE = LOWEST



GPIO_Px_CTRL DRIVEMODE = LOW



GPIO_Px_CTRL DRIVEMODE = STANDARD



GPIO_Px_CTRL DRIVEMODE = HIGH

3.9.3 LFRCO

Table 3.10. LFRCO

Symbol	Parameter	Condition	Min	Typ	Max	Unit
f_{LFRCO}	Oscillation frequency, $V_{\text{DD}} = 3.0 \text{ V}$, $T_{\text{AMB}} = 25^\circ\text{C}$		31.3	32.768	34.3	kHz
t_{LFRCO}	Startup time not including software calibration			150		μs
I_{LFRCO}	Current consumption			361	492	nA
TUNESTEP _{LFRCO}	Frequency step for LSB change in TUNING value			202		Hz

Figure 3.20. Calibrated LFRCO Frequency vs Temperature and Supply Voltage

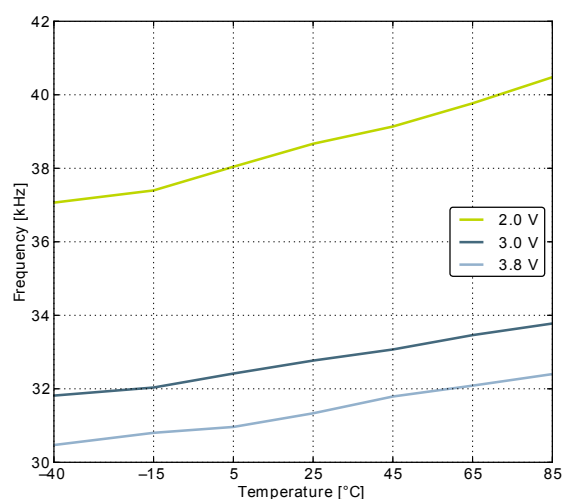
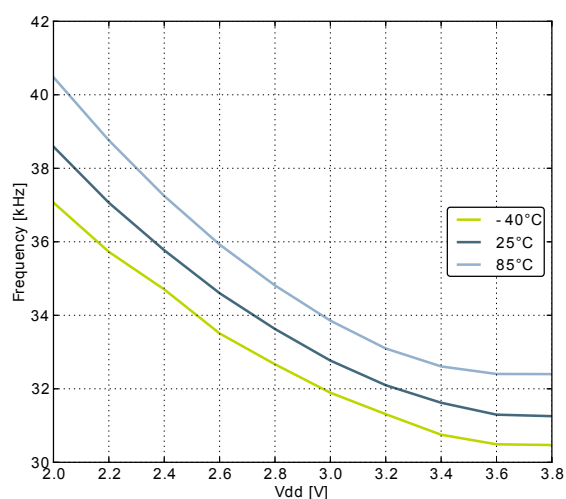
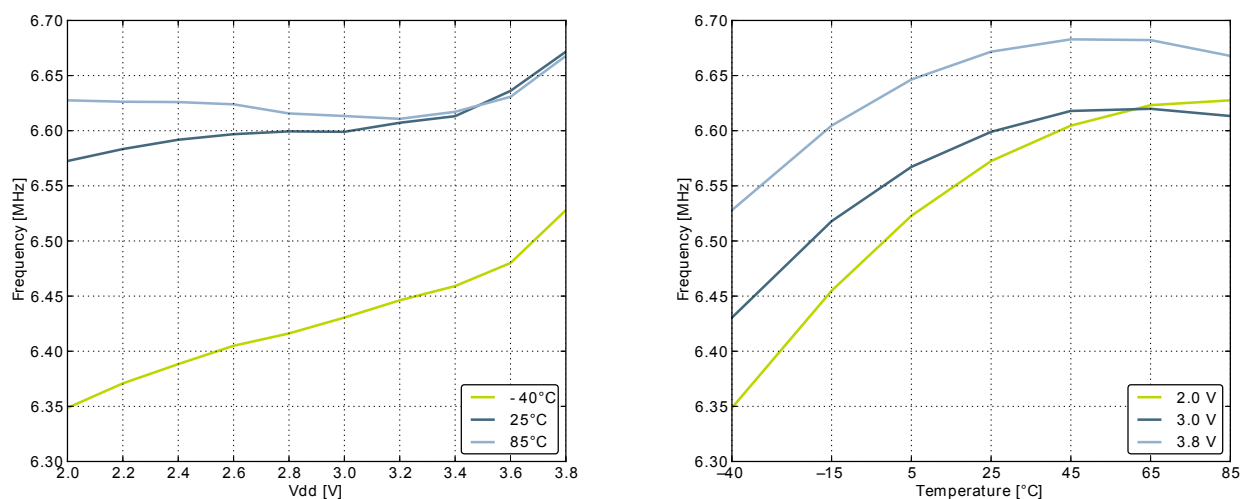
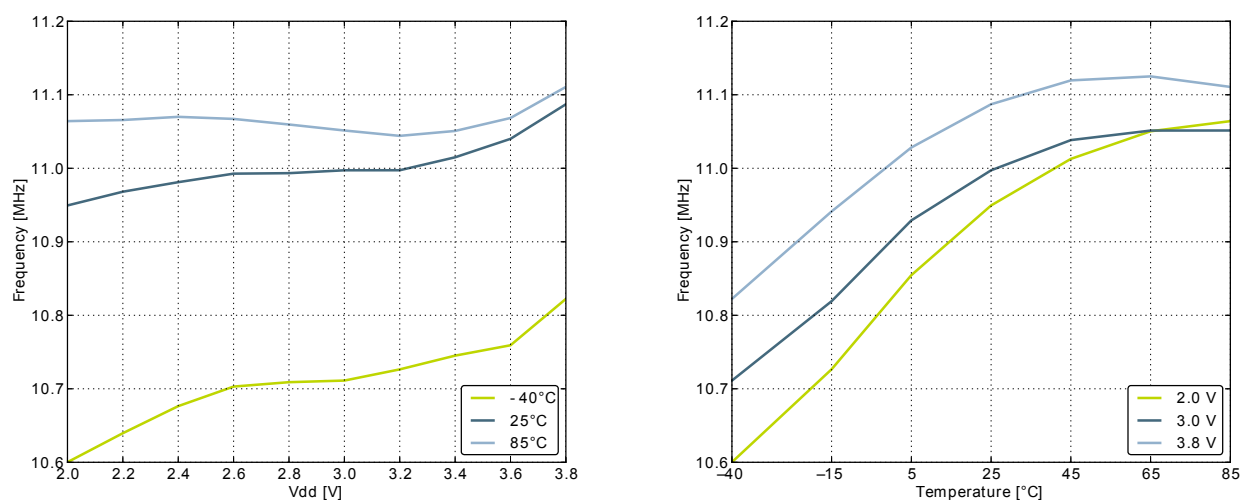
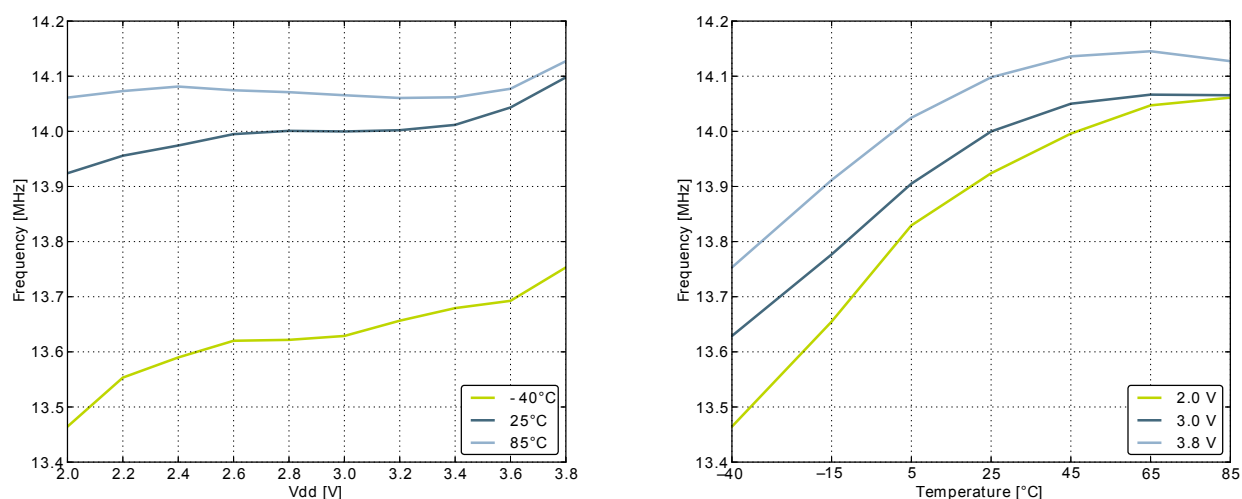


Figure 3.22. Calibrated HFRCO 7 MHz Band Frequency vs Supply Voltage and Temperature**Figure 3.23. Calibrated HFRCO 11 MHz Band Frequency vs Supply Voltage and Temperature****Figure 3.24. Calibrated HFRCO 14 MHz Band Frequency vs Supply Voltage and Temperature**

3.10 Analog Comparator (ACMP)

Table 3.15. ACMP

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{ACMPIN}	Input voltage range		0		V_{DD}	V
V_{ACMPCM}	ACMP Common Mode voltage range		0		V_{DD}	V
I_{ACMP}	Active current	BIASPROG=0b0000, FULL-BIAS=0 and HALFBIAS=1 in ACMPn_CTRL register		0.1	0.4	μA
		BIASPROG=0b1111, FULL-BIAS=0 and HALFBIAS=0 in ACMPn_CTRL register		2.87	15	μA
		BIASPROG=0b1111, FULL-BIAS=1 and HALFBIAS=0 in ACMPn_CTRL register		195	520	μA
$I_{ACMPREF}$	Current consumption of internal voltage reference	Internal voltage reference off. Using external voltage reference		0		μA
		Internal voltage reference		5		μA
$V_{ACMPOFFSET}$	Offset voltage	BIASPROG= 0b1010, FULL-BIAS=0 and HALFBIAS=0 in ACMPn_CTRL register	-12	0	12	mV
$V_{ACMPHYST}$	ACMP hysteresis	Programmable		17		mV
R_{CSRES}	Capacitive Sense Internal Resistance	CSRESSEL=0b00 in ACMPn_INPUTSEL		40		kOhm
		CSRESSEL=0b01 in ACMPn_INPUTSEL		70		kOhm
		CSRESSEL=0b10 in ACMPn_INPUTSEL		101		kOhm
		CSRESSEL=0b11 in ACMPn_INPUTSEL		132		kOhm
$t_{ACMPSTART}$	Startup time				10	μs

The total ACMP current is the sum of the contributions from the ACMP and its internal voltage reference as given in Equation 3.1 (p. 33) . $I_{ACMPREF}$ is zero if an external voltage reference is used.

Total ACMP Active Current

$$I_{ACMPTOTAL} = I_{ACMP} + I_{ACMPREF} \quad (3.1)$$

4.2 Alternate Functionality Pinout

A wide selection of alternate functionality is available for multiplexing to various pins. This is shown in Table 4.2 (p. 40). The table shows the name of the alternate functionality in the first column, followed by columns showing the possible LOCATION bitfield settings.

Note

Some functionality, such as analog interfaces, do not have alternate settings or a LOCATION bitfield. In these cases, the pinout is shown in the column corresponding to LOCATION 0.

Table 4.2. Alternate functionality overview

Alternate	LOCATION							Description
Functionality	0	1	2	3	4	5	6	
ACMP0_CH0	PC0							Analog comparator ACMP0, channel 0.
ACMP0_CH1	PC1							Analog comparator ACMP0, channel 1.
ACMP0_O	PE13		PD6	PB11				Analog comparator ACMP0, digital output.
BOOT_RX	PF1							Bootloader RX.
BOOT_TX	PF0							Bootloader TX.
CMU_CLK0			PD7	PF2				Clock Management Unit, clock output number 0.
CMU_CLK1			PE12	PB11				Clock Management Unit, clock output number 1.
DBG_SWCLK	PF0							Debug-interface Serial Wire clock input. Note that this function is enabled to pin out of reset, and has a built-in pull down.
DBG_SWDIO	PF1							Debug-interface Serial Wire data input / output. Note that this function is enabled to pin out of reset, and has a built-in pull up.
GPIO_EM4WU0	PA0							Pin can be used to wake the system up from EM4
GPIO_EM4WU3	PF1							Pin can be used to wake the system up from EM4
GPIO_EM4WU4	PF2							Pin can be used to wake the system up from EM4
GPIO_EM4WU5	PE13							Pin can be used to wake the system up from EM4
HFX TAL_N	PB14							High Frequency Crystal negative pin. Also used as external optional clock input pin.
HFX TAL_P	PB13							High Frequency Crystal positive pin.
I2C0_SCL		PD7			PC1	PF1	PE13	I2C0 Serial Clock Line input / output.
I2C0_SDA	PA0	PD6			PC0	PF0	PE12	I2C0 Serial Data input / output.
LEU0_RX		PB14		PF1	PA0	PC15		LEUART0 Receive input.
LEU0_TX		PB13		PF0	PF2	PC14		LEUART0 Transmit output. Also used as receive input in half duplex communication.
LFXTAL_N	PB8							Low Frequency Crystal (typically 32.768 kHz) negative pin. Also used as an optional external clock input pin.
LFXTAL_P	PB7							Low Frequency Crystal (typically 32.768 kHz) positive pin.
PCNT0_S0IN			PC0	PD6	PA0			Pulse Counter PCNT0 input number 0.
PCNT0_S1IN	PC14		PC1	PD7	PB11			Pulse Counter PCNT0 input number 1.
PRS_CH0	PA0		PC14	PF2				Peripheral Reflex System PRS, channel 0.
PRS_CH1			PC15	PE12				Peripheral Reflex System PRS, channel 1.
PRS_CH2	PC0			PE13				Peripheral Reflex System PRS, channel 2.

Alternate	LOCATION							Description
Functionality	0	1	2	3	4	5	6	
PRS_CH3	PC1			PA0				Peripheral Reflex System PRS, channel 3.
TIM0_CC0	PA0	PA0			PA0	PF0		Timer 0 Capture Compare input / output channel 0.
TIM0_CC1					PC0	PF1	PA0	Timer 0 Capture Compare input / output channel 1.
TIM0_CC2					PC1	PF2	PF2	Timer 0 Capture Compare input / output channel 2.
TIM0_CDTI1		PC14					PC14	Timer 0 Complimentary Deat Time Insertion channel 1.
TIM0_CDTI2		PC15					PC15	Timer 0 Complimentary Deat Time Insertion channel 2.
TIM1_CC0				PB7	PD6			Timer 1 Capture Compare input / output channel 0.
TIM1_CC1	PC14			PB8	PD7			Timer 1 Capture Compare input / output channel 1.
TIM1_CC2	PC15	PE12		PB11				Timer 1 Capture Compare input / output channel 2.
TIM2_CC0				PF2				Timer 2 Capture Compare input / output channel 0.
TIM2_CC1				PE12				Timer 2 Capture Compare input / output channel 1.
TIM2_CC2				PE13				Timer 2 Capture Compare input / output channel 2.
US0_CLK	PE12			PC15	PB13	PB13	PE12	USART0 clock input / output.
US0_CS	PE13			PC14	PB14	PB14	PE13	USART0 chip select input / output.
US0_RX				PE12	PB8	PC1	PC1	USART0 Asynchronous Receive. USART0 Synchronous mode Master Input / Slave Output (MISO).
US0_TX				PE13	PB7	PC0	PC0	USART0 Asynchronous Transmit. Also used as receive input in half duplex communication. USART0 Synchronous mode Master Output / Slave Input (MOSI).
US1_CLK	PB7		PF0	PC15	PB11			USART1 clock input / output.
US1_CS	PB8		PF1	PC14	PC14	PC0		USART1 chip select input / output.
US1_RX	PC1		PD6	PD6	PA0			USART1 Asynchronous Receive. USART1 Synchronous mode Master Input / Slave Output (MISO).
US1_TX	PC0		PD7	PD7	PF2	PC1		USART1 Asynchronous Transmit. Also used as receive input in half duplex communication. USART1 Synchronous mode Master Output / Slave Input (MOSI).

4.3 GPIO Pinout Overview

The specific GPIO pins available in *EFM32HG108* is shown in Table 4.3 (p. 41) . Each GPIO port is organized as 16-bit ports indicated by letters A through F, and the individual pin on this port is indicated by a number from 15 down to 0.

Table 4.3. GPIO Pinout

Port	Pin 15	Pin 14	Pin 13	Pin 12	Pin 11	Pin 10	Pin 9	Pin 8	Pin 7	Pin 6	Pin 5	Pin 4	Pin 3	Pin 2	Pin 1	Pin 0
Port A	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	PA0
Port B	-	PB14	PB13	-	PB11	-	-	PB8	PB7	-	-	-	-	-	-	-
Port C	PC15	PC14	-	-	-	-	-	-	-	-	-	-	-	-	PC1	PC0
Port D	-	-	-	-	-	-	-	-	PD7	PD6	-	-	-	-	-	-
Port E	-	-	PE13	PE12	-	-	-	-	-	-	-	-	-	-	-	-
Port F	-	-	-	-	-	-	-	-	-	-	-	-	-	PF2	PF1	PF0

7 Revision History

7.1 Revision 1.00

December 4th, 2015

Updated all specs with results of full characterization.

Updated part number to revision B.

7.2 Revision 0.91

May 6th, 2015

Updated current consumption table for energy modes.

Updated GPIO max leakage current.

Updated startup time for HFXO and LFXO.

Updated current consumption for HFRCO and LFRCO.

Updated ADC current consumption.

Updated IDAC characteristics tables.

Updated ACMP internal resistance.

Updated VCMP current consumption.

7.3 Revision 0.90

March 16th, 2015

Note

This datasheet revision applies to a product under development. It's characteristics and specifications are subject to change without notice.

Corrected EM2 current consumption condition in Electrical Characteristics section.

Updated GPIO electrical characteristics.

Updated Max ESR_{HFXO} value for Crystal Frequency of 25 MHz.

Updated LFRCO plots.

Updated HFRCO table and plots.

Updated ADC table and temp sensor plot.

Added DMA current in Digital Peripherals section.

Updated block diagram.

Updated Package dimensions table.

Corrected leadframe type to matte-Sn.

List of Equations

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3.2. VCMP Trigger Level as a Function of Level Setting 35

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