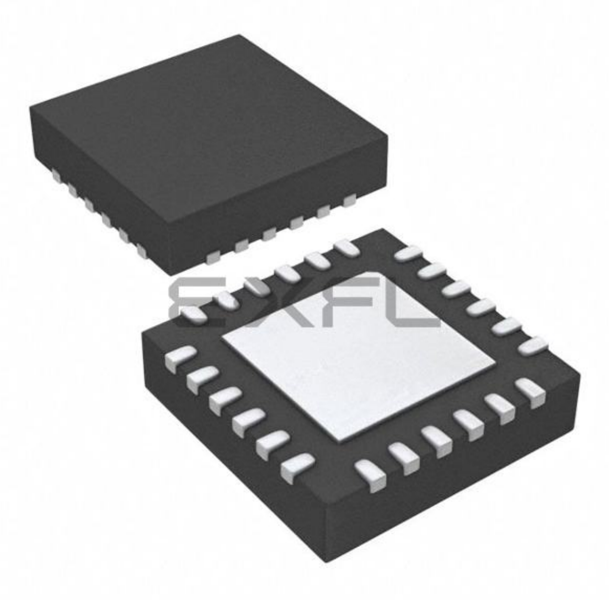




## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Discontinued at Digi-Key |
| Core Processor | ARM® Cortex®-M0+ |
| Core Size | 32-Bit Single-Core |
| Speed | 25MHz |
| Connectivity | I²C, IrDA, SmartCard, SPI, UART/USART |
| Peripherals | Brown-out Detect/Reset, DMA, I²S, POR, PWM, WDT |
| Number of I/O | 17 |
| Program Memory Size | 64KB (64K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 8K x 8 |
| Voltage - Supply (Vcc/Vdd) | 1.98V ~ 3.8V |
| Data Converters | A/D 4x12b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 24-VQFN Exposed Pad |
| Supplier Device Package | 24-QFN (5x5) |
| Purchase URL | https://www.e-xfl.com/product-detail/silicon-labs/efm32hg108f64g-b-qfn24 |

# 1 Ordering Information

Table 1.1 (p. 2) shows the available EFM32HG108 devices.

***Table 1.1. Ordering Information***

| Ordering Code | Flash (kB) | RAM (kB) | Max Speed (MHz) | Supply Voltage (V) | Temperature (ºC) | Package |
|---|---|---|---|---|---|---|
| EFM32HG108F32G-B-QFN24 | 32 | 4 | 25 | 1.98 - 3.8 | -40 - 85 | QFN24 |
| EFM32HG108F64G-B-QFN24 | 64 | 8 | 25 | 1.98 - 3.8 | -40 - 85 | QFN24 |

Adding the suffix 'R' to the part number (e.g. EFM32HG108F32G-B-QFN24R) denotes tape and reel.

Visit **www.silabs.com** for information on global distributors and representatives.

### 2.1.12 Pre-Programmed UART Bootloader

The bootloader presented in application note AN0003 is pre-programmed in the device at factory. Autobaud and destructive write are supported. The autobaud feature, interface and commands are described further in the application note.

### 2.1.13 Low Energy Universal Asynchronous Receiver/Transmitter (LEUART)

The unique LEUART$^{TM}$, the Low Energy UART, is a UART that allows two-way UART communication on a strict power budget. Only a 32.768 kHz clock is needed to allow UART communication up to 9600 baud/s. The LEUART includes all necessary hardware support to make asynchronous serial communication possible with minimum of software intervention and energy consumption.

### 2.1.14 Timer/Counter (TIMER)

The 16-bit general purpose Timer has 3 compare/capture channels for input capture and compare/Pulse-Width Modulation (PWM) output. TIMER0 also includes a Dead-Time Insertion module suitable for motor control applications.

### 2.1.15 Real Time Counter (RTC)

The Real Time Counter (RTC) contains a 24-bit counter and is clocked either by a 32.768 kHz crystal oscillator, or a 32.768 kHz RC oscillator. In addition to energy modes EM0 and EM1, the RTC is also available in EM2. This makes it ideal for keeping track of time since the RTC is enabled in EM2 where most of the device is powered down.

### 2.1.16 Pulse Counter (PCNT)

The Pulse Counter (PCNT) can be used for counting pulses on a single input or to decode quadrature encoded inputs. It runs off either the internal LFACLK or the PCNTn_S0IN pin as external clock source. The module may operate in energy mode EM0 - EM3.

### 2.1.17 Analog Comparator (ACMP)

The Analog Comparator is used to compare the voltage of two analog inputs, with a digital output indicating which input voltage is higher. Inputs can either be one of the selectable internal references or from external pins. Response time and thereby also the current consumption can be configured by altering the current supply to the comparator.

### 2.1.18 Voltage Comparator (VCMP)

The Voltage Supply Comparator is used to monitor the supply voltage from software. An interrupt can be generated when the supply falls below or rises above a programmable threshold. Response time and thereby also the current consumption can be configured by altering the current supply to the comparator.

### 2.1.19 General Purpose Input/Output (GPIO)

In the EFM32HG108, there are 17 General Purpose Input/Output (GPIO) pins, which are divided into ports with up to 16 pins each. These pins can individually be configured as either an output or input. More advanced configurations like open-drain, filtering and drive strength can also be configured individually for the pins. The GPIO pins can also be overridden by peripheral pin connections, like Timer PWM outputs or USART communication, which can be routed to several locations on the device. The GPIO supports up to 11 asynchronous external pin interrupts, which enables interrupts from any pin on the device. Also, the input value of a pin can be routed through the Peripheral Reflex System to other peripherals.

*Figure 2.2. EFM32HG108 Memory Map with largest RAM and Flash sizes*

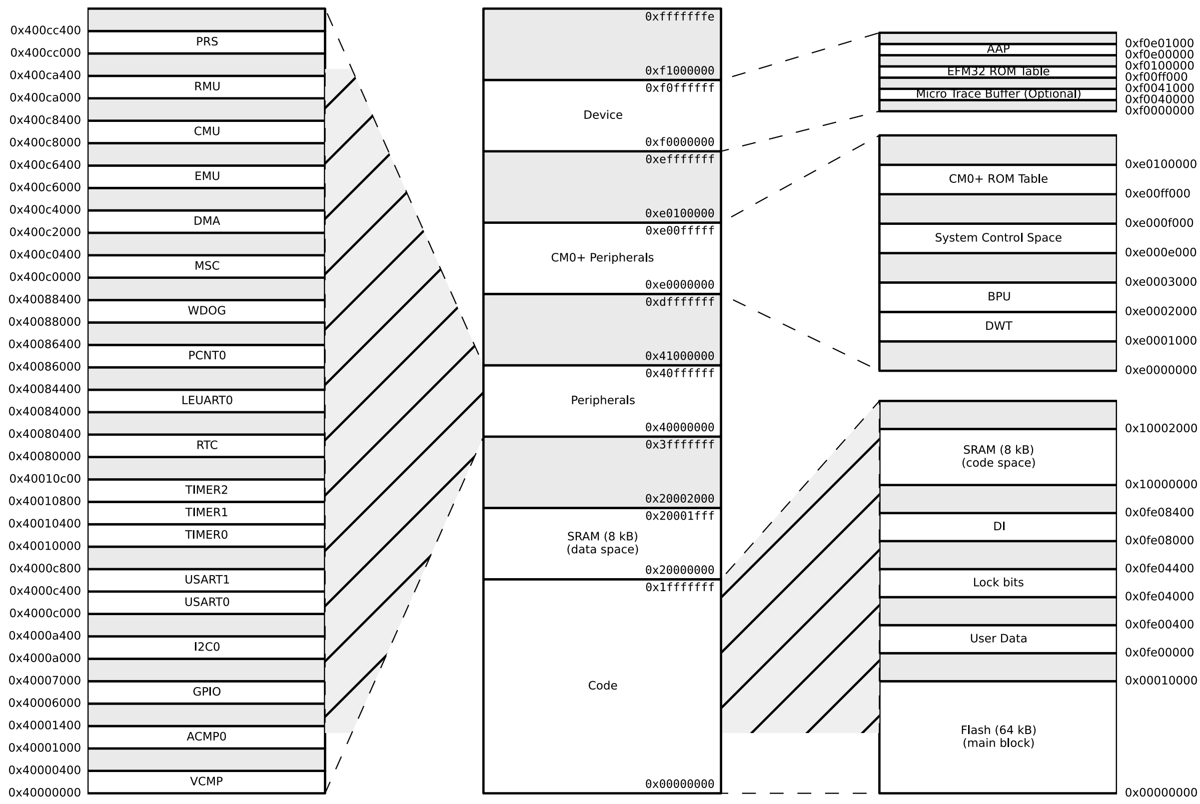


**Figure 3.3. EM0 Current consumption while executing prime number calculation code from flash with HFRCO running at 14 MHz**

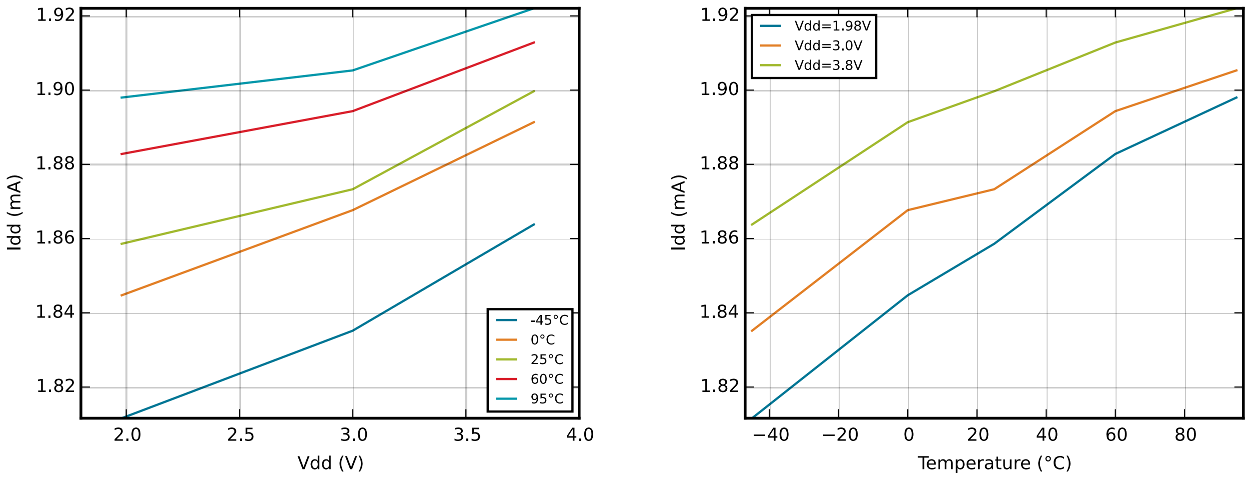



**Figure 3.4. EM0 Current consumption while executing prime number calculation code from flash with HFRCO running at 11 MHz**

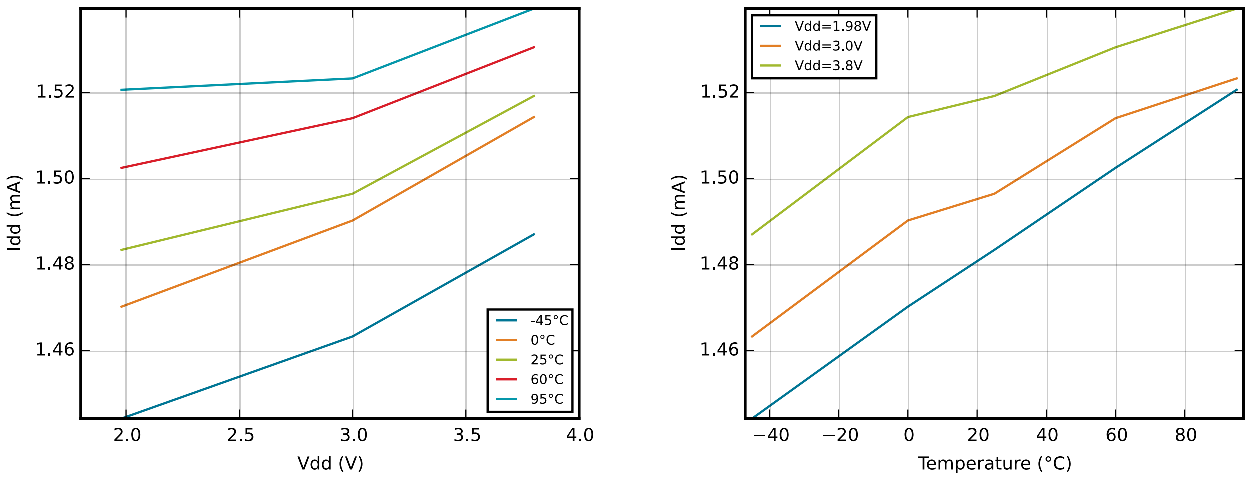


**Figure 3.7. EM1 Current consumption with all peripheral clocks disabled and HFRCO running at 21 MHz**

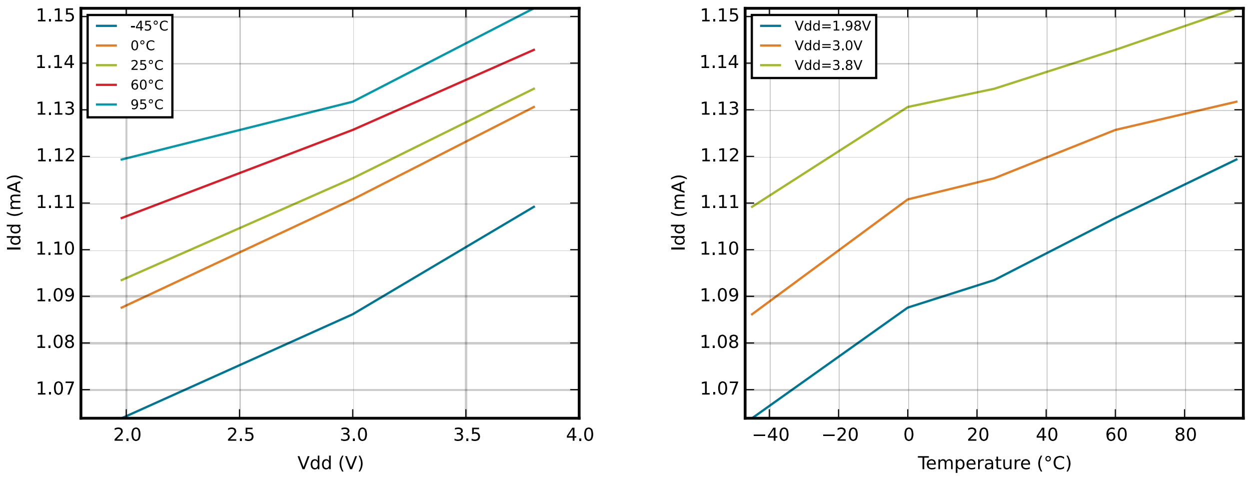
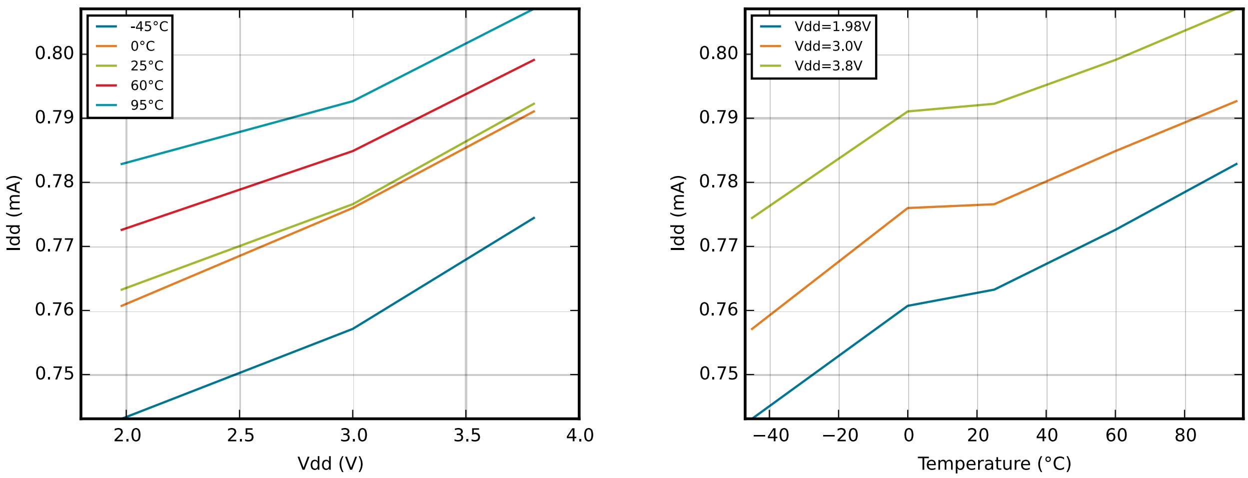
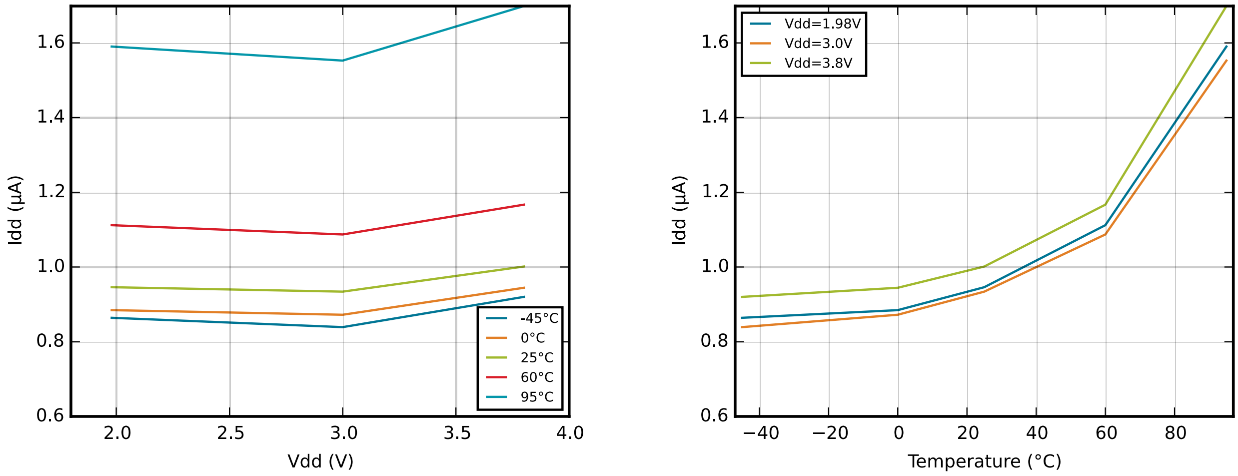



**Figure 3.8. EM1 Current consumption with all peripheral clocks disabled and HFRCO running at 14 MHz**



### 3.4.3 EM2 Current Consumption

***Figure 3.11. EM2 current consumption. RTC prescaled to 1kHz, 32.768 kHz LFRCO.***




### 3.4.4 EM3 Current Consumption

***Figure 3.12. EM3 current consumption.***

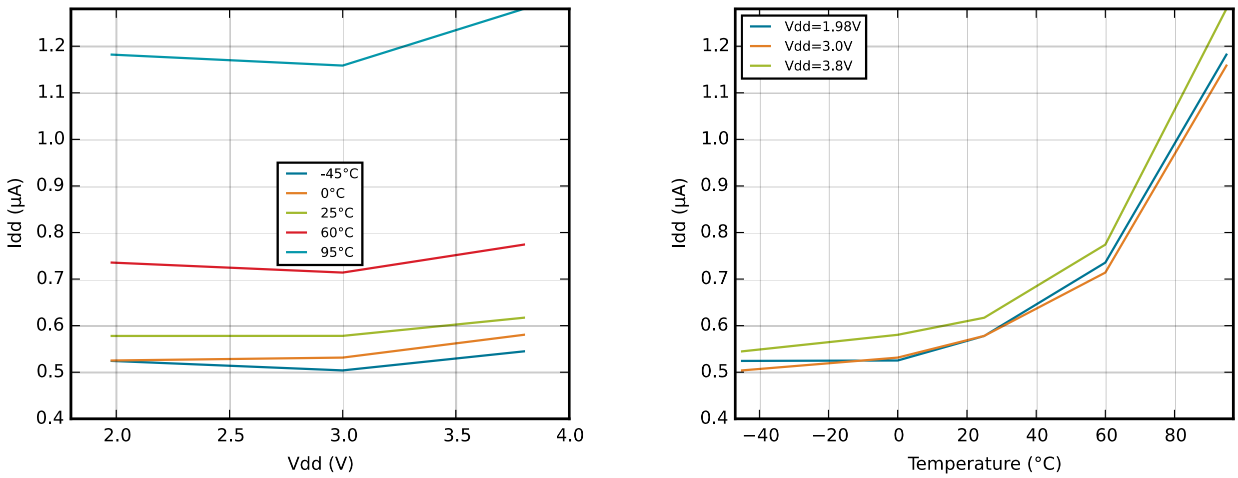


**Table 3.5. Power Management**

| Symbol | Parameter | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{BODextthr-}$ | BOD threshold on falling external supply voltage | EM0 | 1.74 | | 1.96 | V |
| | | EM2 | 1.71 | 1.86 | 1.98 | V |
| $V_{BODextthr+}$ | BOD threshold on rising external supply voltage | | | 1.85 | | V |
| $t_{RESET}$ | Delay from reset is released until program execution starts | Applies to Power-on Reset, Brown-out Reset and pin reset. | | 163 | | µs |
| $C_{DECOUPLE}$ | Voltage regulator decoupling capacitor. | X5R capacitor recommended. Apply between DECOUPLE pin and GROUND | | 1 | | µF |

## 3.7 Flash

**Table 3.6. Flash**

| Symbol | Parameter | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $EC_{FLASH}$ | Flash erase cycles before failure | | 20000 | | | cycles |
| $RET_{FLASH}$ | Flash data retention | $T_{AMB}$<150°C | 10000 | | | h |
| | | $T_{AMB}$<85°C | 10 | | | years |
| | | $T_{AMB}$<70°C | 20 | | | years |
| $t_{W\_PROG}$ | Word (32-bit) programming time | | 20 | | | µs |
| $t_{P\_ERASE}$ | Page erase time | | 20 | 20.4 | 20.8 | ms |
| $t_{D\_ERASE}$ | Device erase time | | 40 | 40.8 | 41.6 | ms |
| $I_{ERASE}$ | Erase current | | | | 7[1] | mA |
| $I_{WRITE}$ | Write current | | | | 7[1] | mA |
| $V_{FLASH}$ | Supply voltage during flash erase and write | | 1.98 | | 3.8 | V |

[1]Measured at 25°C

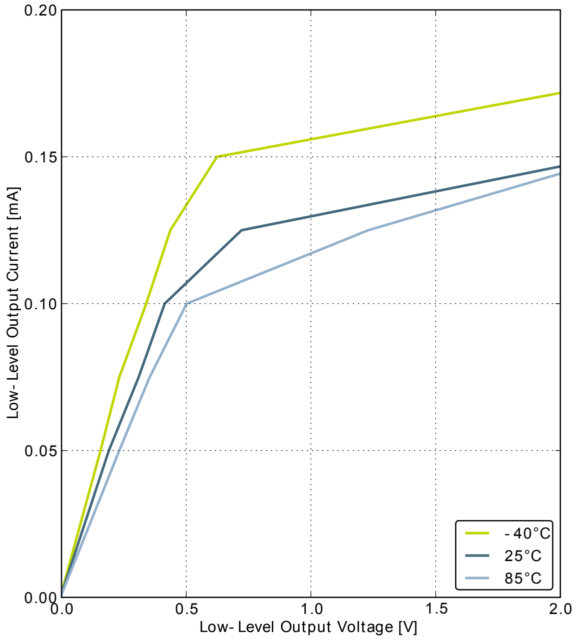
## 3.8 General Purpose Input Output

**Table 3.7. GPIO**

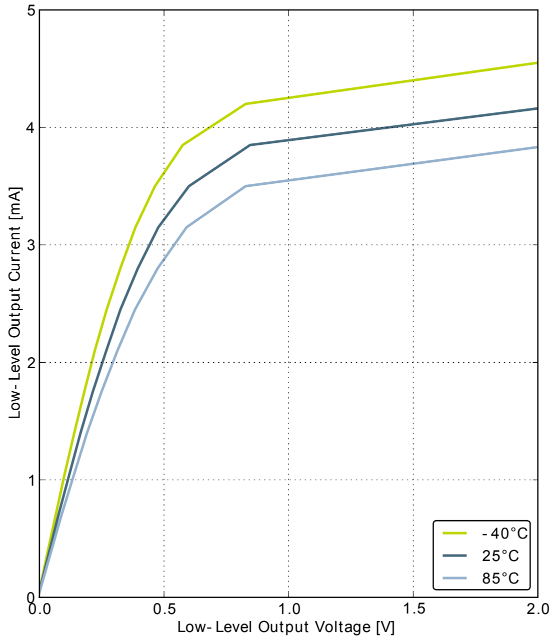
| Symbol | Parameter | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{IOIL}$ | Input low voltage | | | | $0.30V_{DD}$ | V |
| $V_{IOIH}$ | Input high voltage | | $0.70V_{DD}$ | | | V |
| $V_{IOOH}$ | Output high voltage (Production test condition = 3.0V, DRIVEMODE = STANDARD) | Sourcing 0.1 mA, $V_{DD}$=1.98 V, GPIO_Px_CTRL DRIVEMODE = LOWEST | | $0.80V_{DD}$ | | V |
| | | Sourcing 0.1 mA, $V_{DD}$=3.0 V, GPIO_Px_CTRL DRIVEMODE = LOWEST | | $0.90V_{DD}$ | | V |

| Symbol | Parameter | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| | by the glitch suppression filter | | | | | |
| $t_{IOOF}$ | Output fall time | GPIO_Px_CTRL DRIVEMODE = LOWEST and load capacitance $C_L$=12.5-25pF. | 20+0.1$C_L$ | | 250 | ns |
| | | GPIO_Px_CTRL DRIVEMODE = LOW and load capacitance $C_L$=350-600pF | 20+0.1$C_L$ | | 250 | ns |
| $V_{IOHYST}$ | I/O pin hysteresis ($V_{IOTHR+}$ - $V_{IOTHR-}$) | $V_{DD}$ = 1.98 - 3.8 V | 0.1$V_{DD}$ | | | V |

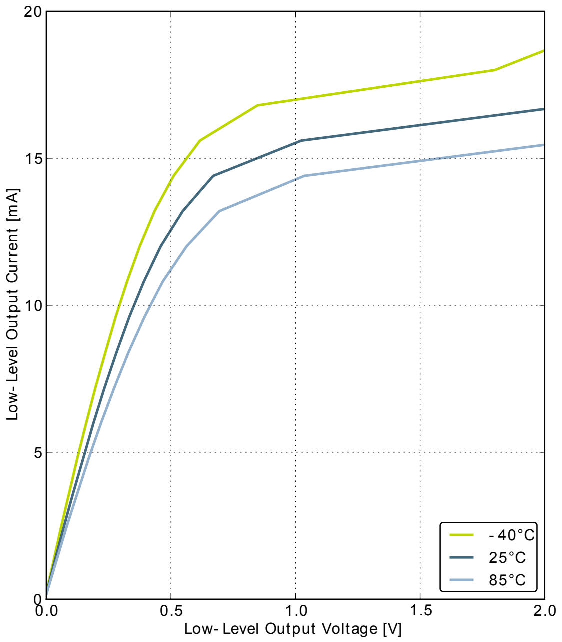
***Figure 3.14. Typical Low-Level Output Current, 2V Supply Voltage***



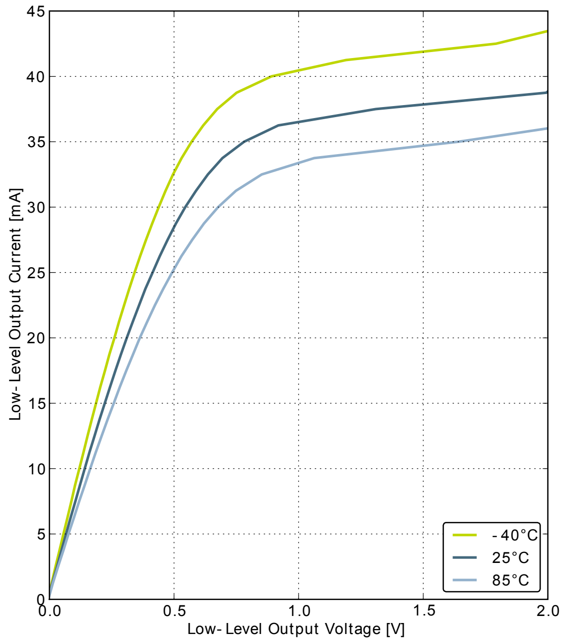

GPIO_Px_CTRL DRIVEMODE = LOWEST




GPIO_Px_CTRL DRIVEMODE = LOW




GPIO_Px_CTRL DRIVEMODE = STANDARD




GPIO_Px_CTRL DRIVEMODE = HIGH

*Figure 3.17. Typical High-Level Output Current, 3V Supply Voltage*

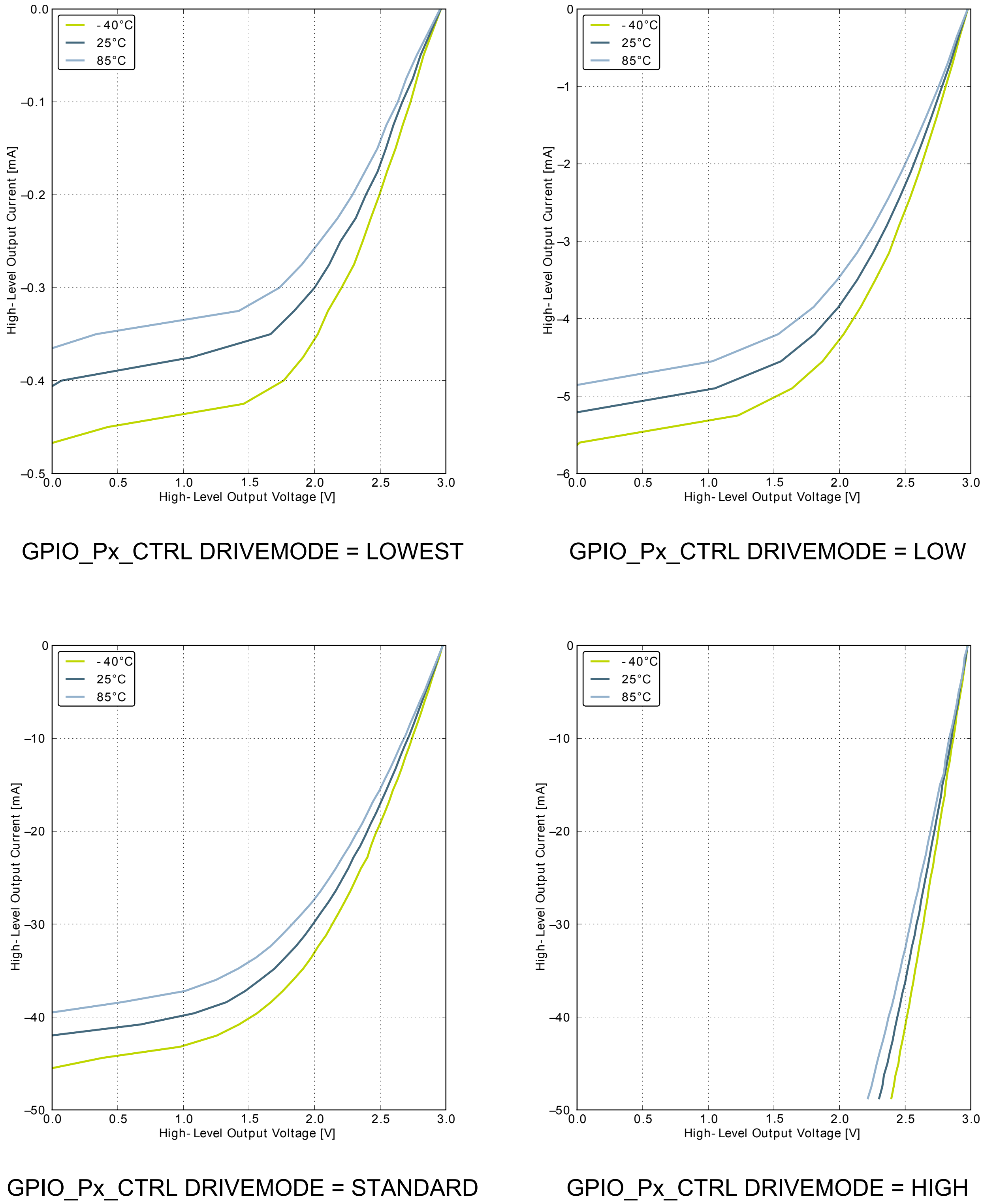
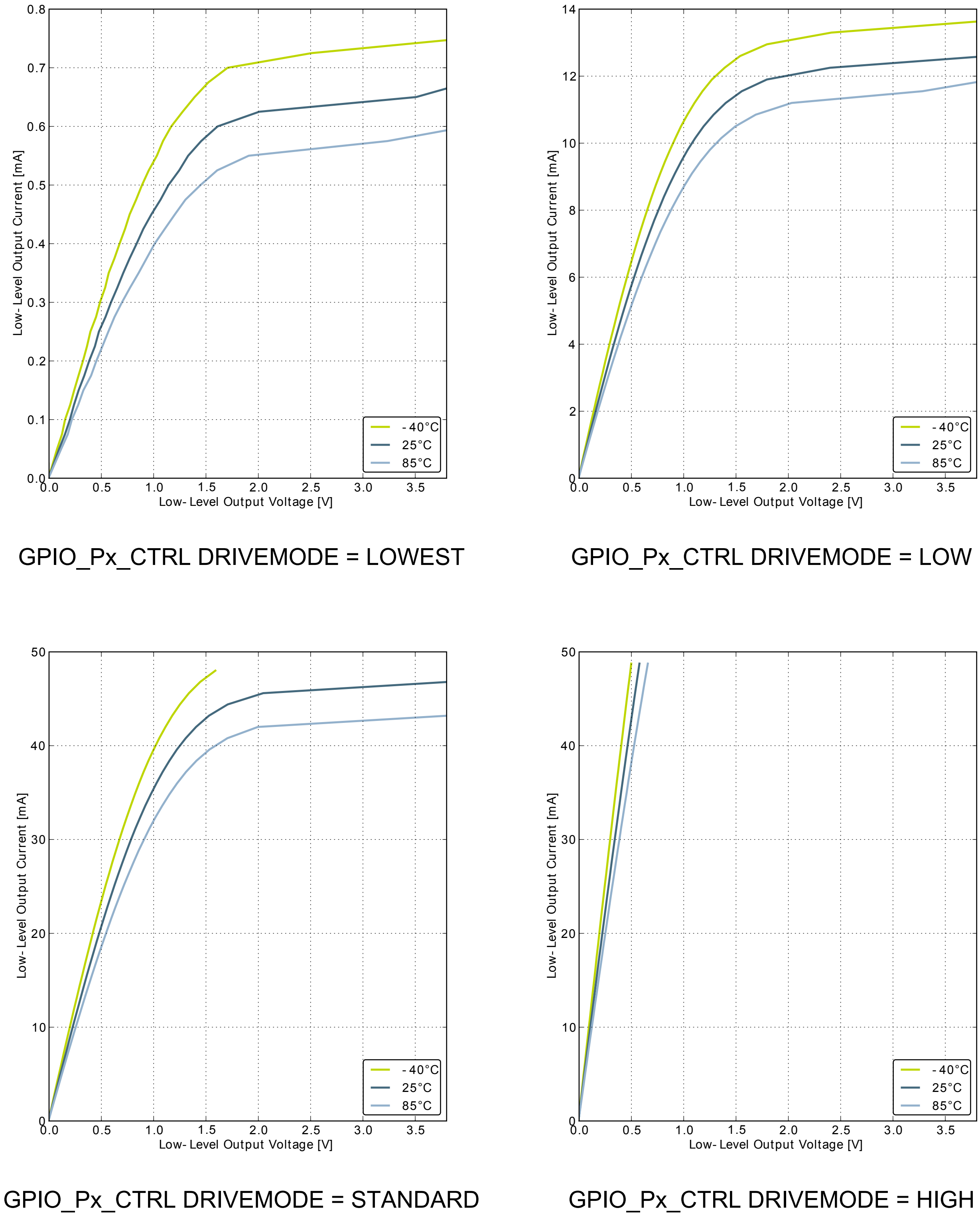
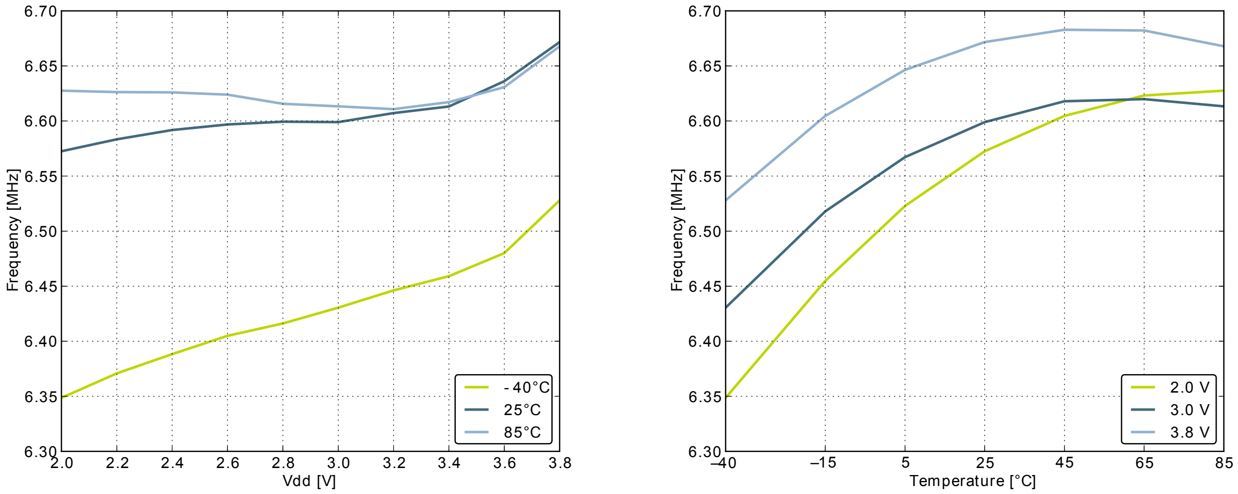


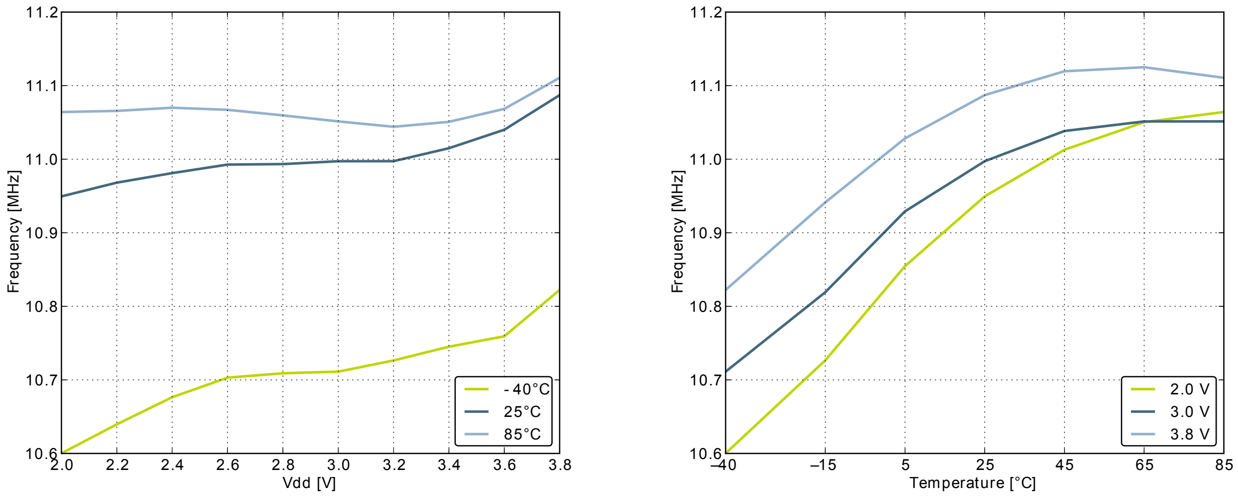
*Figure 3.18. Typical Low-Level Output Current, 3.8V Supply Voltage*



### Figure 3.22. Calibrated HFRCO 7 MHz Band Frequency vs Supply Voltage and Temperature




### Figure 3.23. Calibrated HFRCO 11 MHz Band Frequency vs Supply Voltage and Temperature




### Figure 3.24. Calibrated HFRCO 14 MHz Band Frequency vs Supply Voltage and Temperature

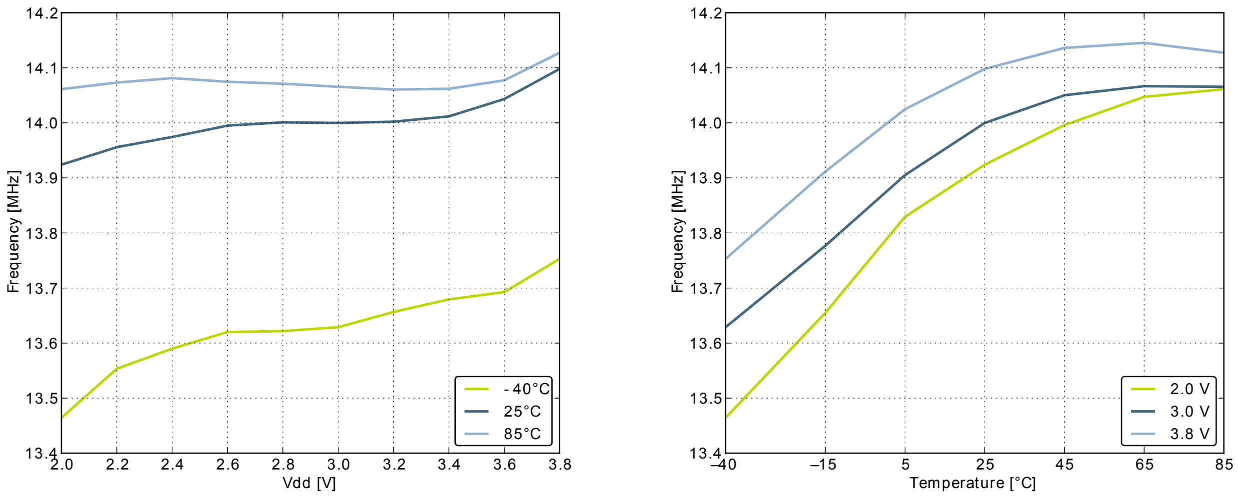
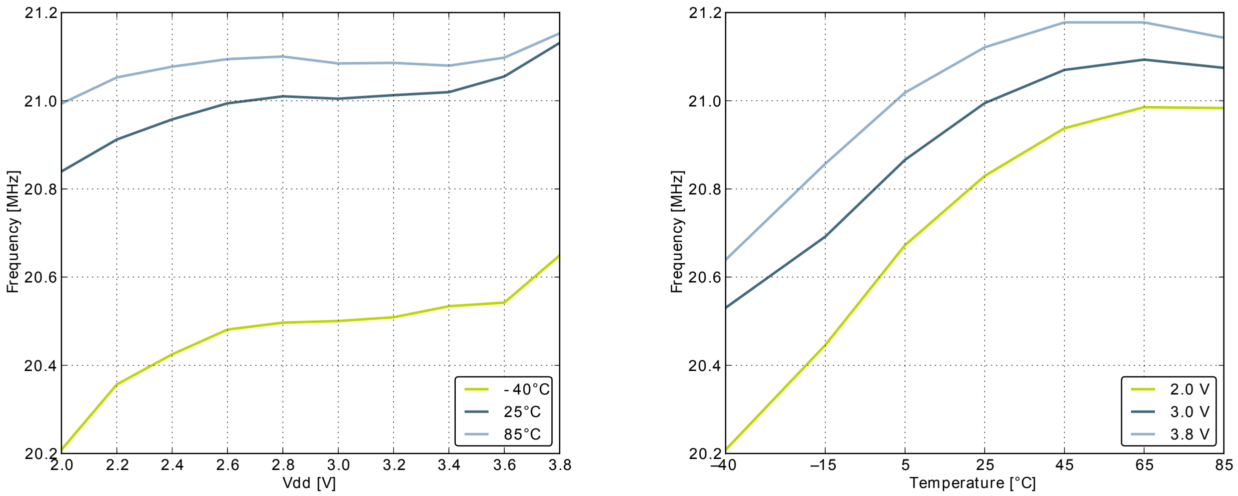


*Figure 3.25. Calibrated HFRCO 21 MHz Band Frequency vs Supply Voltage and Temperature*

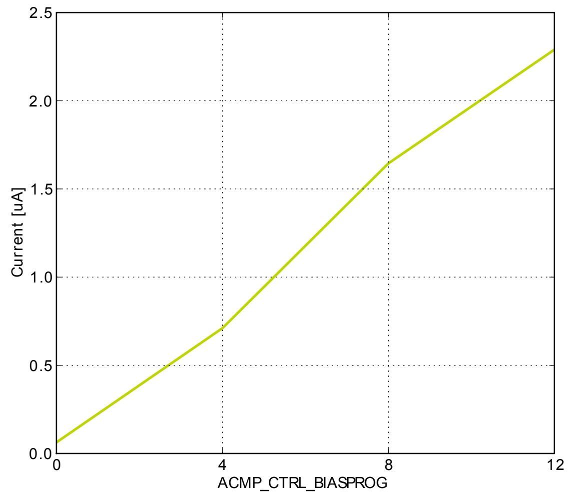



## 3.9.5 AUXHFRCO

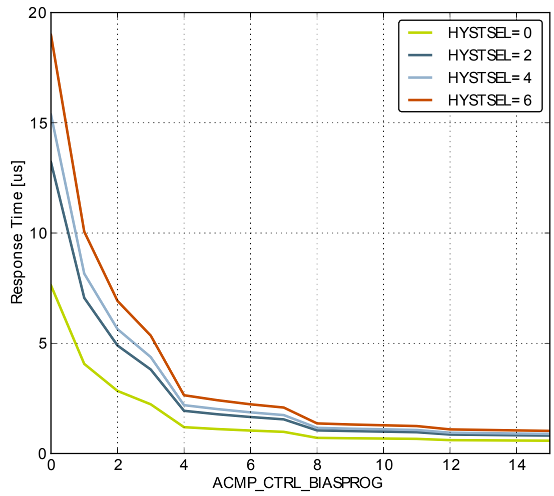
*Table 3.12. AUXHFRCO*

| Symbol | Parameter | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $f_{AUXHFRCO}$ | Oscillation frequency, $V_{DD}$= 3.0 V, $T_{AMB}$=25°C | 21 MHz frequency band | 20.37 | 21.0 | 21.63 | MHz |
| | | 14 MHz frequency band | 13.58 | 14.0 | 14.42 | MHz |
| | | 11 MHz frequency band | 10.67 | 11.0 | 11.33 | MHz |
| | | 7 MHz frequency band | 6.40 | 6.60 | 6.80 | MHz |
| | | 1 MHz frequency band | 1.15 | 1.20 | 1.25 | MHz |
| $t_{AUXHFRCO\_settling}$ | Settling time after start-up | $f_{AUXHFRCO}$ = 14 MHz | | 0.6 | | Cycles |
| $TUNESTEP_{AUXHFRCO}$ | Frequency step for LSB change in TUNING value | 21 MHz frequency band | | 52.8 | | kHz |
| | | 14 MHz frequency band | | 36.9 | | kHz |
| | | 11 MHz frequency band | | 30.1 | | kHz |
| | | 7 MHz frequency band | | 18.0 | | kHz |
| | | 1 MHz frequency band | | 3.4 | | kHz |

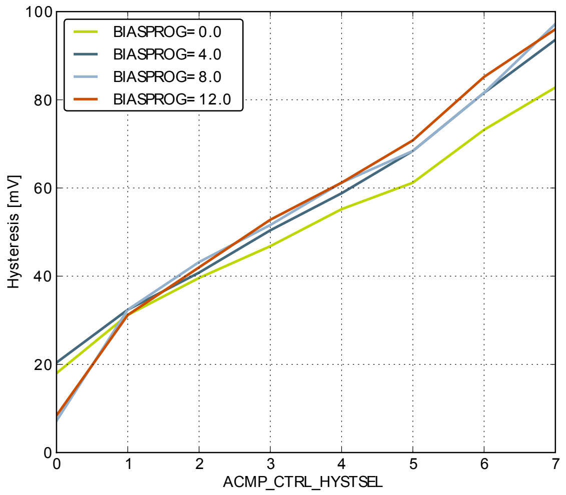
*Figure 3.26. ACMP Characteristics, Vdd = 3V, Temp = 25°C, FULLBIAS = 0, HALFBIAS = 1*




Current consumption, HYSTSEL = 4




Response time , $V_{cm}$ = 1.25V, CP+ to CP- = 100mV




Hysteresis

**Table 3.18. I2C Fast-mode (Fm)**

| Symbol | Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $f_{SCL}$ | SCL clock frequency | 0 | | 400[1] | kHz |
| $t_{LOW}$ | SCL clock low time | 1.3 | | | µs |
| $t_{HIGH}$ | SCL clock high time | 0.6 | | | µs |
| $t_{SU,DAT}$ | SDA set-up time | 100 | | | ns |
| $t_{HD,DAT}$ | SDA hold time | 8 | | 900[2,3] | ns |
| $t_{SU,STA}$ | Repeated START condition set-up time | 0.6 | | | µs |
| $t_{HD,STA}$ | (Repeated) START condition hold time | 0.6 | | | µs |
| $t_{SU,STO}$ | STOP condition set-up time | 0.6 | | | µs |
| $t_{BUF}$ | Bus free time between a STOP and START condition | 1.3 | | | µs |

[1]For the minimum HFPERCLK frequency required in Fast-mode, see the I2C chapter in the EFM32HG Reference Manual.
[2]The maximum SDA hold time ($t_{HD,DAT}$) needs to be met only when the device does not stretch the low time of SCL ($t_{LOW}$).
[3]When transmitting data, this number is guaranteed only when I2Cn_CLKDIV < ((900*$10^{-9}$ [s] * $f_{HFPERCLK}$ [Hz]) - 5).

**Table 3.19. I2C Fast-mode Plus (Fm+)**

| Symbol | Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $f_{SCL}$ | SCL clock frequency | 0 | | 1000[1] | kHz |
| $t_{LOW}$ | SCL clock low time | 0.5 | | | µs |
| $t_{HIGH}$ | SCL clock high time | 0.26 | | | µs |
| $t_{SU,DAT}$ | SDA set-up time | 50 | | | ns |
| $t_{HD,DAT}$ | SDA hold time | 8 | | | ns |
| $t_{SU,STA}$ | Repeated START condition set-up time | 0.26 | | | µs |
| $t_{HD,STA}$ | (Repeated) START condition hold time | 0.26 | | | µs |
| $t_{SU,STO}$ | STOP condition set-up time | 0.26 | | | µs |
| $t_{BUF}$ | Bus free time between a STOP and START condition | 0.5 | | | µs |

[1]For the minimum HFPERCLK frequency required in Fast-mode Plus, see the I2C chapter in the EFM32HG Reference Manual.

## 3.13 Digital Peripherals

**Table 3.20. Digital Peripherals**

| Symbol | Parameter | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $I_{USART}$ | USART current | USART idle current, clock enabled | | 7.5 | | µA/MHz |
| $I_{LEUART}$ | LEUART current | LEUART idle current, clock enabled | | 150 | | nA |
| $I_{I2C}$ | I2C current | I2C idle current, clock enabled | | 6.25 | | µA/MHz |
| $I_{TIMER}$ | TIMER current | TIMER_0 idle current, clock enabled | | 8.75 | | µA/MHz |
| $I_{PCNT}$ | PCNT current | PCNT idle current, clock enabled | | 100 | | nA |
| $I_{RTC}$ | RTC current | RTC idle current, clock enabled | | 100 | | nA |

# 4.2 Alternate Functionality Pinout

A wide selection of alternate functionality is available for multiplexing to various pins. This is shown in Table 4.2 (p. 40). The table shows the name of the alternate functionality in the first column, followed by columns showing the possible LOCATION bitfield settings.

**Note**

Some functionality, such as analog interfaces, do not have alternate settings or a LOCATION bitfield. In these cases, the pinout is shown in the column corresponding to LOCATION 0.

***Table 4.2. Alternate functionality overview***

| Alternate | LOCATION | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Functionality | 0 | 1 | 2 | 3 | 4 | 5 | 6 | Description |
| ACMP0_CH0 | PC0 | | | | | | | Analog comparator ACMP0, channel 0. |
| ACMP0_CH1 | PC1 | | | | | | | Analog comparator ACMP0, channel 1. |
| ACMP0_O | PE13 | | PD6 | PB11 | | | | Analog comparator ACMP0, digital output. |
| BOOT_RX | PF1 | | | | | | | Bootloader RX. |
| BOOT_TX | PF0 | | | | | | | Bootloader TX. |
| CMU_CLK0 | | | PD7 | PF2 | | | | Clock Management Unit, clock output number 0. |
| CMU_CLK1 | | | PE12 | PB11 | | | | Clock Management Unit, clock output number 1. |
| DBG_SWCLK | PF0 | | | | | | | Debug-interface Serial Wire clock input.<br><br>Note that this function is enabled to pin out of reset, and has a built-in pull down. |
| DBG_SWDIO | PF1 | | | | | | | Debug-interface Serial Wire data input / output.<br><br>Note that this function is enabled to pin out of reset, and has a built-in pull up. |
| GPIO_EM4WU0 | PA0 | | | | | | | Pin can be used to wake the system up from EM4 |
| GPIO_EM4WU3 | PF1 | | | | | | | Pin can be used to wake the system up from EM4 |
| GPIO_EM4WU4 | PF2 | | | | | | | Pin can be used to wake the system up from EM4 |
| GPIO_EM4WU5 | PE13 | | | | | | | Pin can be used to wake the system up from EM4 |
| HFXTAL_N | PB14 | | | | | | | High Frequency Crystal negative pin. Also used as external optional clock input pin. |
| HFXTAL_P | PB13 | | | | | | | High Frequency Crystal positive pin. |
| I2C0_SCL | | PD7 | | | PC1 | PF1 | PE13 | I2C0 Serial Clock Line input / output. |
| I2C0_SDA | PA0 | PD6 | | | PC0 | PF0 | PE12 | I2C0 Serial Data input / output. |
| LEU0_RX | | PB14 | | PF1 | PA0 | PC15 | | LEUART0 Receive input. |
| LEU0_TX | | PB13 | | PF0 | PF2 | PC14 | | LEUART0 Transmit output. Also used as receive input in half duplex communication. |
| LFXTAL_N | PB8 | | | | | | | Low Frequency Crystal (typically 32.768 kHz) negative pin. Also used as an optional external clock input pin. |
| LFXTAL_P | PB7 | | | | | | | Low Frequency Crystal (typically 32.768 kHz) positive pin. |
| PCNT0_S0IN | | | PC0 | PD6 | PA0 | | | Pulse Counter PCNT0 input number 0. |
| PCNT0_S1IN | PC14 | | PC1 | PD7 | PB11 | | | Pulse Counter PCNT0 input number 1. |
| PRS_CH0 | PA0 | | PC14 | PF2 | | | | Peripheral Reflex System PRS, channel 0. |
| PRS_CH1 | | | PC15 | PE12 | | | | Peripheral Reflex System PRS, channel 1. |
| PRS_CH2 | PC0 | | | PE13 | | | | Peripheral Reflex System PRS, channel 2. |

| Alternate | LOCATION | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Functionality | 0 | 1 | 2 | 3 | 4 | 5 | 6 | Description |
| PRS_CH3 | PC1 | | | PA0 | | | | Peripheral Reflex System PRS, channel 3. |
| TIM0_CC0 | PA0 | PA0 | | | PA0 | PF0 | | Timer 0 Capture Compare input / output channel 0. |
| TIM0_CC1 | | | | | PC0 | PF1 | PA0 | Timer 0 Capture Compare input / output channel 1. |
| TIM0_CC2 | | | | | PC1 | PF2 | PF2 | Timer 0 Capture Compare input / output channel 2. |
| TIM0_CDTI1 | | PC14 | | | | | PC14 | Timer 0 Complimentary Deat Time Insertion channel 1. |
| TIM0_CDTI2 | | PC15 | | | | | PC15 | Timer 0 Complimentary Deat Time Insertion channel 2. |
| TIM1_CC0 | | | | PB7 | PD6 | | | Timer 1 Capture Compare input / output channel 0. |
| TIM1_CC1 | PC14 | | | PB8 | PD7 | | | Timer 1 Capture Compare input / output channel 1. |
| TIM1_CC2 | PC15 | PE12 | | PB11 | | | | Timer 1 Capture Compare input / output channel 2. |
| TIM2_CC0 | | | | PF2 | | | | Timer 2 Capture Compare input / output channel 0. |
| TIM2_CC1 | | | | PE12 | | | | Timer 2 Capture Compare input / output channel 1. |
| TIM2_CC2 | | | | PE13 | | | | Timer 2 Capture Compare input / output channel 2. |
| US0_CLK | PE12 | | | PC15 | PB13 | PB13 | PE12 | USART0 clock input / output. |
| US0_CS | PE13 | | | PC14 | PB14 | PB14 | PE13 | USART0 chip select input / output. |
| US0_RX | | | | PE12 | PB8 | PC1 | PC1 | USART0 Asynchronous Receive.<br>USART0 Synchronous mode Master Input / Slave Output (MISO). |
| US0_TX | | | | PE13 | PB7 | PC0 | PC0 | USART0 Asynchronous Transmit.Also used as receive input in half duplex communication.<br>USART0 Synchronous mode Master Output / Slave Input (MOSI). |
| US1_CLK | PB7 | | PF0 | PC15 | PB11 | | | USART1 clock input / output. |
| US1_CS | PB8 | | PF1 | PC14 | PC14 | PC0 | | USART1 chip select input / output. |
| US1_RX | PC1 | | PD6 | PD6 | PA0 | | | USART1 Asynchronous Receive.<br>USART1 Synchronous mode Master Input / Slave Output (MISO). |
| US1_TX | PC0 | | PD7 | PD7 | PF2 | PC1 | | USART1 Asynchronous Transmit.Also used as receive input in half duplex communication.<br>USART1 Synchronous mode Master Output / Slave Input (MOSI). |

## 4.3 GPIO Pinout Overview

The specific GPIO pins available in *EFM32HG108* is shown in Table 4.3 (p. 41) . Each GPIO port is organized as 16-bit ports indicated by letters A through F, and the individual pin on this port is indicated by a number from 15 down to 0.

***Table 4.3. GPIO Pinout***

| Port | Pin 15 | Pin 14 | Pin 13 | Pin 12 | Pin 11 | Pin 10 | Pin 9 | Pin 8 | Pin 7 | Pin 6 | Pin 5 | Pin 4 | Pin 3 | Pin 2 | Pin 1 | Pin 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Port A | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | PA0 |
| Port B | - | PB14 | PB13 | - | PB11 | - | - | PB8 | PB7 | - | - | - | - | - | - | - |
| Port C | PC15 | PC14 | - | - | - | - | - | - | - | - | - | - | - | - | PC1 | PC0 |
| Port D | - | - | - | - | - | - | - | - | PD7 | PD6 | - | - | - | - | - | - |
| Port E | - | - | PE13 | PE12 | - | - | - | - | - | - | - | - | - | - | - | - |
| Port F | - | - | - | - | - | - | - | - | - | - | - | - | - | PF2 | PF1 | PF0 |

*Figure 5.3. QFN24 PCB Stencil Design*

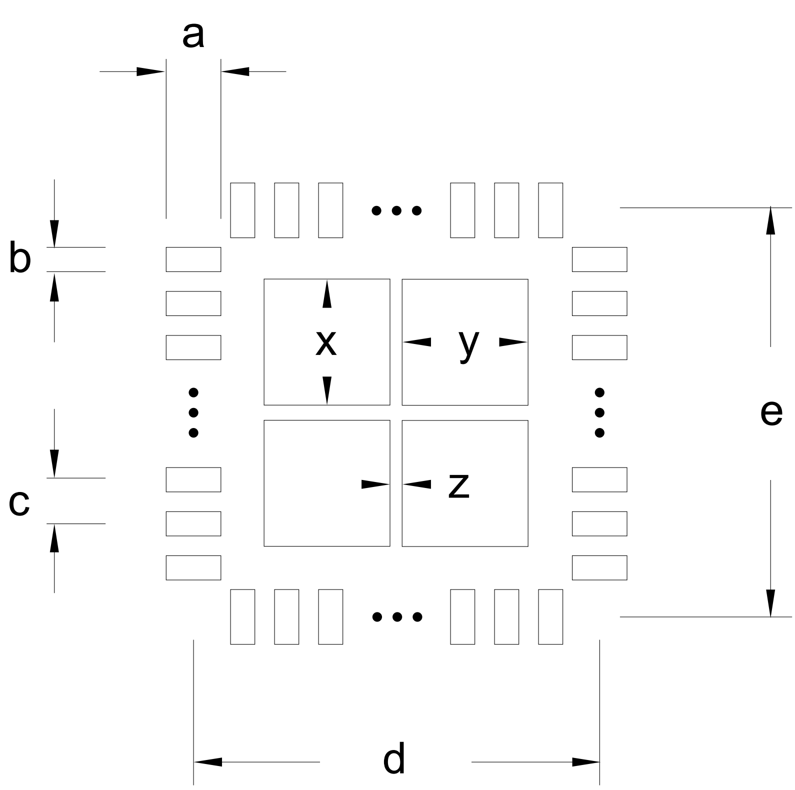



*Table 5.3. QFN24 PCB Stencil Design Dimensions (Dimensions in mm)*

| Symbol | Dim. (mm) | Symbol | Dim. (mm) |
|---|---|---|---|
| a | 0.60 | e | 5.00 |
| b | 0.25 | x | 1.00 |
| c | 0.65 | y | 1.00 |
| d | 5.00 | z | 0.50 |

1. The drawings are not to scale.
2. All dimensions are in millimeters.
3. All drawings are subject to change without notice.
4. The PCB Land Pattern drawing is in compliance with IPC-7351B.
5. Stencil thickness 0.125 mm.
6. For detailed pin-positioning, see Figure 4.2 (p. 42) .

## 5.2 Soldering Information

The latest IPC/JEDEC J-STD-020 recommendations for Pb-Free reflow soldering should be followed.

Place as many and as small as possible vias underneath each of the solder patches under the ground pad.

# List of Equations

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ZERO
ARM Cortex-M0+

TINY
ARM Cortex-M3

GECKO
ARM Cortex-M3

LEOPARD
ARM Cortex-M3

GIANT
ARM Cortex-M3

WONDER
ARM Cortex-M4