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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	F²MC-16LX
Core Size	16-Bit
Speed	16MHz
Connectivity	CANbus, EBI/EMI, SCI, Serial I/O, UART/USART
Peripherals	POR, PWM, WDT
Number of I/O	78
Program Memory Size	256KB (256K x 8)
Program Memory Type	Mask ROM
EEPROM Size	-
RAM Size	6K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 8x8/10b
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-BQFP
Supplier Device Package	100-QFP (14x20)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/mb90594gpf-g-127-bnde1

1. Product Lineup

Features		MB90591G/594G	MB90F591G/F594G	MB90V590G
Classification		Mask ROM product	Flash ROM product	Evaluation product
ROM size		384/256 Kbytes	384/256 Kbytes Boot block Hard-wired reset vector	None
RAM size		8/6 Kbytes	8/6 Kbytes	8 Kbytes
Emulator-specific power supply *1		—		None
CPU functions		The number of instructions : 340 Instruction bit length : 8 bits, 16 bits Instruction length : 1 byte to 7 bytes Data bit length : 1 bit, 8 bits, 16 bits Minimum execution time : 62.5 ns (at machine clock frequency of 16 MHz) Interrupt processing time : 1.5 μs (at machine clock frequency of 16 MHz, minimum value)		
UART (3 channels)		Clock synchronized transmission (500 Kbps / 1 Mbps / 2 Mbps) Clock asynchronized transmission (4808/5208/9615/10417/19230/38460/62500 /500000 bps at machine clock frequency of 16 MHz) Transmission can be performed by bi-directional serial transmission or by master/slave connection.		
8/10-bit A/D converter		Conversion precision : 8/10-bit can be selectively used. Number of inputs : 8 One-shot conversion mode (converts selected channel once only) Scan conversion mode (converts two or more successive channels and can program up to 8 channels) Continuous conversion mode (converts selected channel continuously) Stop conversion mode (converts selected channel and stop operation repeatedly)		
8/16-bit PPG timers (6 channels)		Number of channels : 6 (8/16-bit × 6 channels) PPG operation of 8-bit or 16-bit A pulse wave of given intervals and given duty ratios can be output. Pulse interval : fsys, fsys/2^1, fsys/2^2, fsys/2^3, fsys/2^4, 128μs (at oscillation of 4 MHz, fsys = system clock frequency of 16 MHz, fosc = oscillation clock frequency)		
16-bit Reload timer		Number of channels : 2 Operation clock frequency : fsys/2^1, fsys/2^3, fsys/2^5 (fsys = System clock frequency) Supports External Event Count function		
16-bit I/O timer	16-bit Output compares	Number of channels : 6 (8/16-bit × 6 channels) Pin input factor : A match signal of compare register		
	Input captures	Number of channels : 6 Rewriting a register value upon a pin input (rising, falling, or both edges)		

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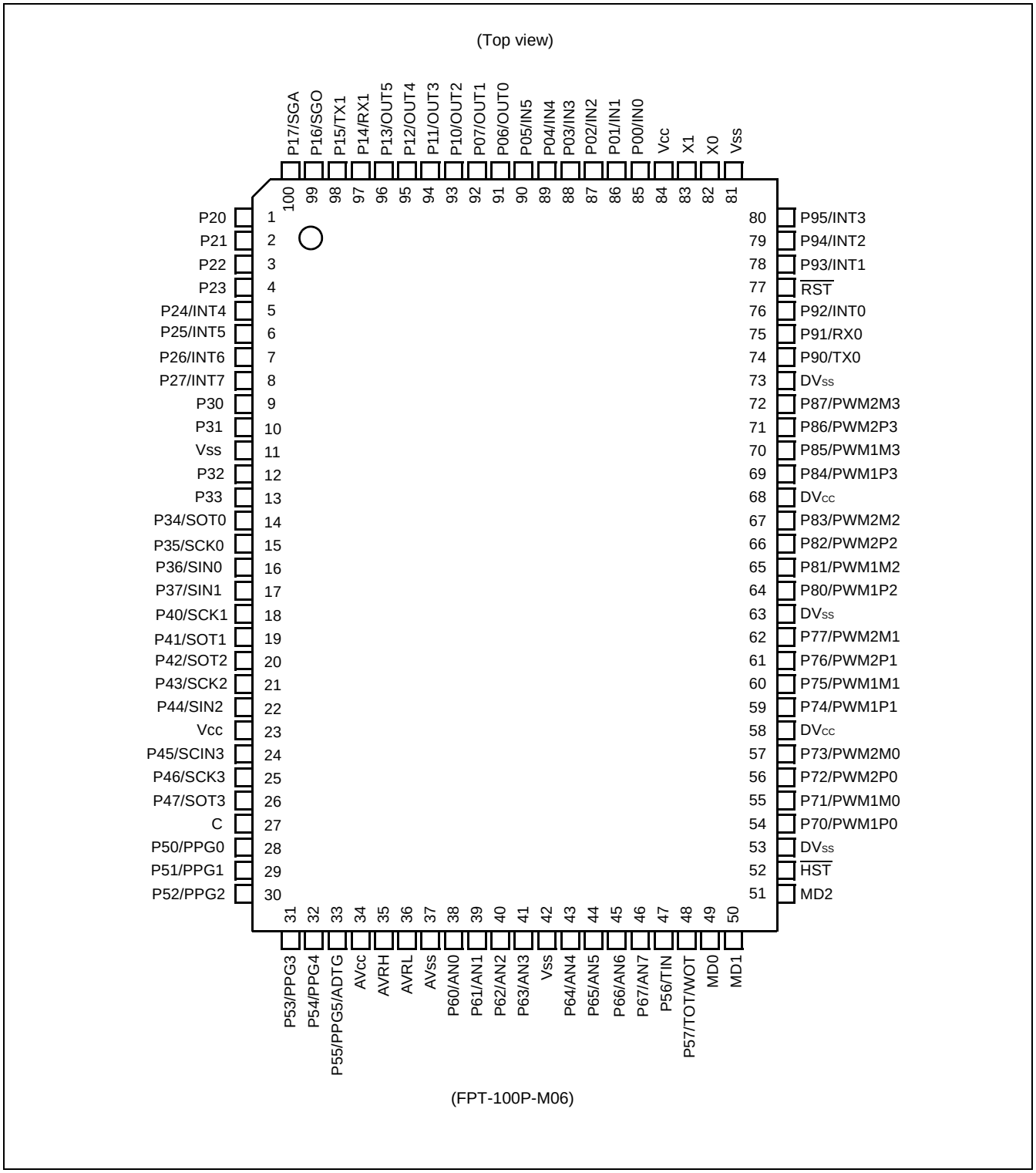
Features	MB90591G/594G	MB90F591G/F594G	MB90V590G
CAN Interface	Number of channels : 2 Conforms to CAN Specification Version 2.0 Part A and B Automatic re-transmission in case of error Automatic transmission responding to Remote Frame Prioritized 16 message buffers for data and ID's Supports multiple messages Flexible configuration of acceptance filtering : Full bit compare / Full bit mask / Two partial bit masks Supports up to 1Mbps CAN bit timing setting : MB90(F)59xG : TSEG2 ≥ RSJW		
Stepping motor controller (4 channels)	Four high current outputs for each channel Synchronized two 8-bit PWM's for each channel		
External interrupt circuit	Number of inputs : 8 Started by a rising edge, a falling edge, an "H" level input, or an "L" level input.		
Sound generator	8-bit PWM signal is mixed with tone frequency from 8-bit reload counter PWM frequency : 62.5K, 31.2K, 15.6K, 7.8KHz (at System clock = 16MHz) Tone frequency : PWM frequency / 2 / (reload value + 1)		
Extended I/O serial interface	Clock synchronized transmission (31.25K/62.5K/125K/500K/1Mbps at machine clock frequency of 16 MHz) LSB first/MSB first		
Watch timer	Directly operates with the system clock Read/Write accessible Second/Minute/Hour registers		
Watchdog timer	Reset generation interval : 3.58 ms, 14.33 ms, 57.23 ms, 458.75 ms (at oscillation of 4 MHz, minimum value)		
Flash Memory	Supports automatic programming, Embedded Algorithm and Write/Erase/Erase-Suspend/Resume commands A flag indicating completion of the algorithm Hard-wired reset vector available in order to point to a fixed boot sector in Flash Memory Boot block configuration Erase can be performed on each block Block protection with external programming voltage Flash Writer from Minato Electronics Inc.		
Low-power consumption (stand-by) mode	Sleep/stop/CPU intermittent operation/watch timer/hardware stand-by		
Process	CMOS		
Power supply voltage for operation*2	5 V±10 % (MB90V590G, MB90F594G, MB90594G) 5 V±5 % (MB90F591G, MB90591G)		
Package	QFP-100		PGA-256

*1 : It is setting of DIP switch S2 when Emulation pod (MB2145-507) is used.
Please refer to the MB2145-507 hardware manual (2.7 Emulator-specific Power Pin) about details.

*2 : Varies with conditions such as the operating frequency. (See section "Electrical Characteristics.")

2. Pin Assignment



(FPT-100P-M06)

3. Pin Description

No.	Pin name	Circuit type	Function
82	X0	A	Oscillator pin
83	X1		
77	$\overline{RST}$	B	Reset input
52	$\overline{HST}$	C	Hardware standby input
85 to 90	P00 to P05	D	General purpose I/O
	IN0 to IN5		Inputs for the Input Captures
91 to 96	P06, P07, P10 to P13	D	General purpose I/O
	OUT0 to OUT5		Outputs for the Output Compares. To enable the signal outputs, the corresponding bits of the Port Direction registers should be set to “1”.
97	P14	D	General purpose I/O
	RX1		RX input for CAN Interface 1
98	P15	D	General purpose I/O
	TX1		TX output for CAN Interface 1. To enable the signal output, the corresponding bit of the Port Direction register should be set to “1”.
99	P16	D	General purpose I/O
	SGO		SGO output for the Sound Generator. To enable the signal output, the corresponding bit of the Port Direction register should be set to “1”.
100	P17	D	General purpose I/O
	SGA		SGA output for the Sound Generator. To enable the signal output, the corresponding bit of the Port Direction register should be set to “1”.
1 to 4	P20 to P23	D	General purpose I/O
5 to 8	P24 to P27	D	General purpose I/O
	INT4 to INT7		External interrupt input for INT4 to INT7
9, 10	P30, P31	D	General purpose I/O
12, 13	P32, P33	D	General purpose I/O
14	P34	D	General purpose I/O
	SOT0		SOT output for UART 0. To enable the signal output, the corresponding bit of the Port Direction register should be set to “1”.
15	P35	D	General purpose I/O
	SCK0		SCK input/output for UART 0. To enable the signal output, the corresponding bit of the Port Direction register should be set to “1”.

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No.	Pin name	Circuit type	Function
54 to 57	P70 to P73	F	General purpose I/O
	PWM1P0, PWM1M0, PWM2P0, PWM2M0		Output for Stepping Motor Controller channel 0.
59 to 62	P74 to P77	F	General purpose I/O
	PWM1P1, PWM1M1, PWM2P1, PWM2M1		Output for Stepping Motor Controller channel 1.
64 to 67	P80 to P83	F	General purpose I/O
	PWM1P2, PWM1M2, PWM2P2, PWM2M2		Output for Stepping Motor Controller channel 2.
69 to 72	P84 to P87	F	General purpose I/O
	PWM1P3, PWM1M3, PWM2P3, PWM2M3		Output for Stepping Motor Controller channel 3.
74	P90	D	General purpose I/O
	TX0		TX output for CAN Interface 0
75	P91	D	General purpose I/O
	RX0		RX input for CAN Interface 0
76	P92	D	General purpose I/O
	INT0		External interrupt input for INT0
78	P93	D	General purpose I/O
	INT1		External interrupt input for INT1
79	P94	D	General purpose I/O
	INT2		External interrupt input for INT2
80	P95	D	General purpose I/O
	INT3		External interrupt input for INT3
58, 68	DV_{CC}	—	Dedicated power supply pins for the high current output buffers (Pin No. 54 to 72)
53, 63, 73	DV_{SS}	—	Dedicated ground pins for the high current output buffers (Pin No. 54 to 72)
34	AV_{CC}	Power supply	Power supply for analog circuit pin When turning this power supply on or off, always be sure to first apply electric potential equal to or greater than AV_{CC} to V_{CC}.
37	AV_{SS}	Power supply	Ground level for analog circuit

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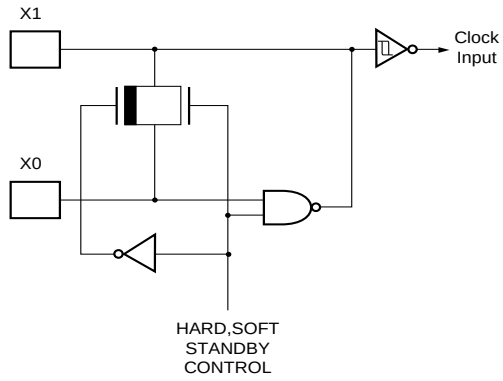
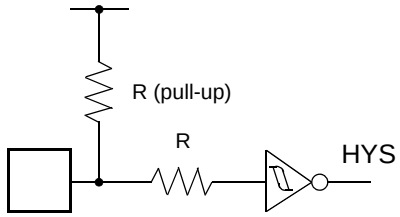
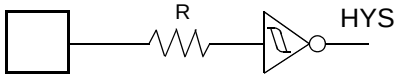
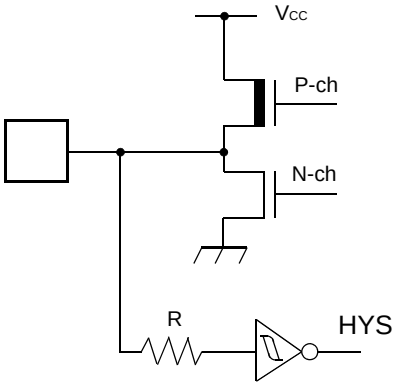
4. I/O Circuit Type

Circuit Type	Circuit	Remarks
A		■ Oscillation feedback resistor : 1 MΩ approx.
B		■ Hysteresis input with pull-up resistor : 50 kΩ approx.
C		■ Hysteresis input
D		■ CMOS output ■ Hysteresis input

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5. Handling Devices

(1) Preventing latch-up
CMOS IC chips may suffer latch-up under the following conditions :

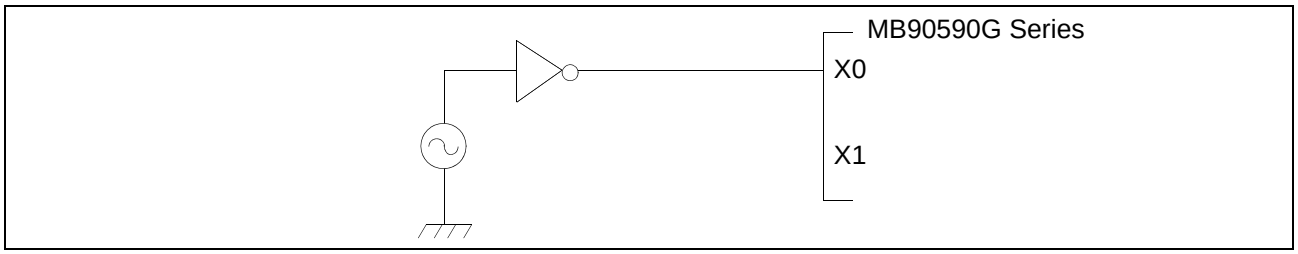
- A voltage higher than Vcc or lower than Vss is applied to an input or output pin.
- A voltage higher than the rated voltage is applied between Vcc and Vss.
- The AVcc power supply is applied before the Vcc voltage.

Latch-up may increase the power supply current drastically, causing thermal damage to the device.
For the same reason, also be careful not to let the analog power-supply voltage (AV_{CC}, AVRH) exceed the digital power-supply voltage.

(2) Treatment of unused pins
Leaving unused input pins open may result in misbehavior or latch up and possible permanent damage of the device. Therefor they must be pulled up or pulled down through resistors. In this case those resistors should be more than 2 kΩ.
Unused bidirectional pins should be set to the output state and can be left open, or the input state with the above described connection.

(3) Using external clock
To use external clock, drive X0 pin only and leave X1 pin unconnected.
Below is a diagram of how to use external clock.

Using external clock



(12) Initialization

The device contains internal registers which are initialized only by a power-on reset. To initialize these registers, please turn on the power again.

(13) Directions of “DIV A, Ri” and “DIVW A, RWi” instructions

In the Signed multiplication and division instructions (“DIV A, Ri” and “DIVW A, RWi”), the value of the corresponding bank register (DTB, ADB, USB, SSB) is set in “00 $_H$”.

If the values of the corresponding bank registers (DTB,ADB,USB,SSB) are set to other than “00 $_H$”, the remainder by the execution result of the instruction is not stored in the register of the instruction operand.

(14) Using REALOS

The use of EI^{2}OS is not possible with the REALOS real time operating system.

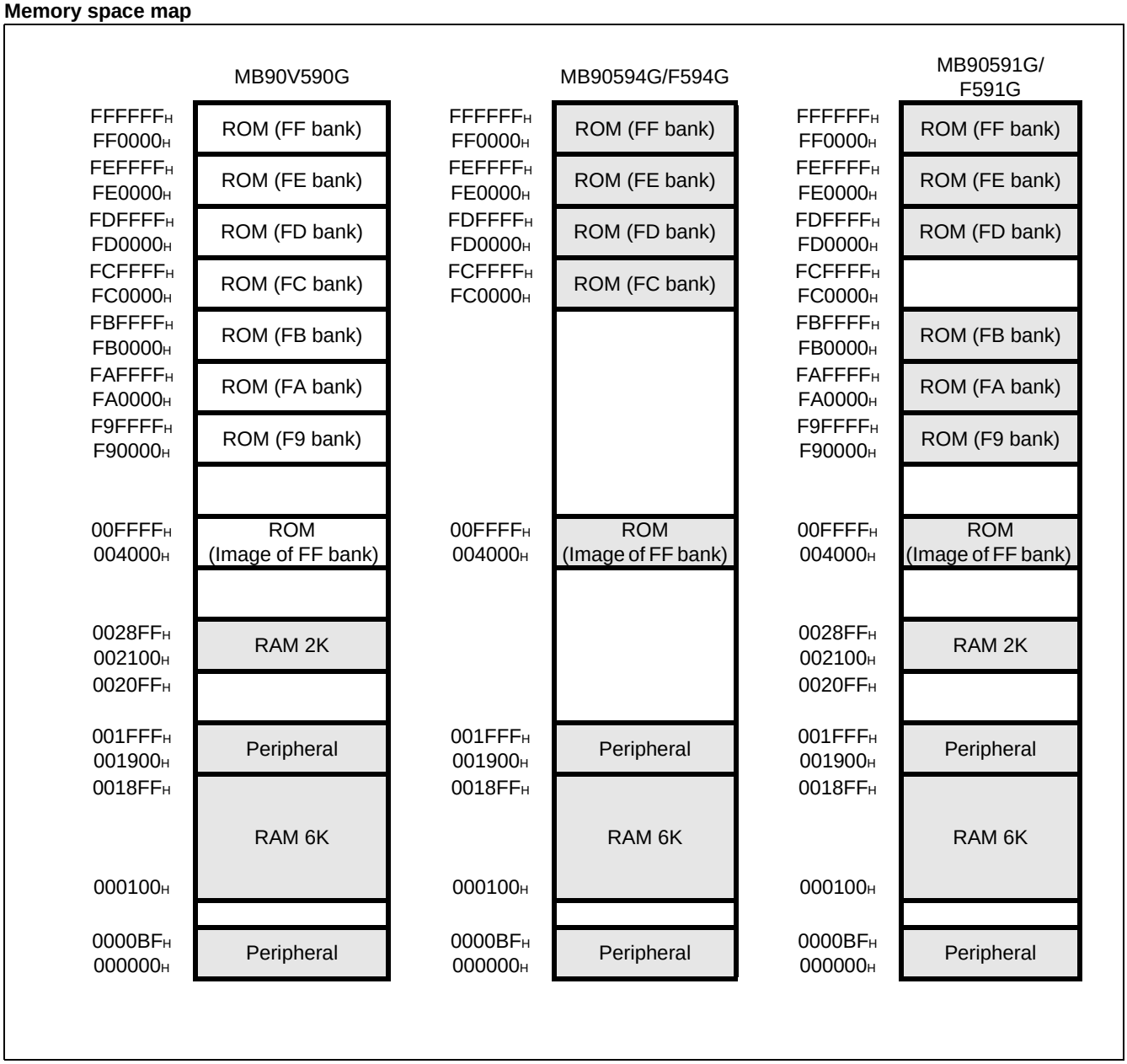
(15) Caution on Operations during PLL Clock Mode

If the PLL clock mode is selected in the microcontroller, it may attempt to continue the operation using the free-running frequency of the automatic oscillating circuit in the PLL circuitry even if the oscillator is out of place or the clock input is stopped. Performance of this operation, however, cannot be guaranteed.

7. Memory Space

The memory space of the MB90590/590G Series is shown below

Memory space map



Note: : The ROM data of bank FF is reflected in the upper address of bank 00, realizing effective use of the C compiler small model. The lower 16-bit of bank FF and the lower 16-bit of bank 00 are assigned to the same address, enabling reference of the table on the ROM without stating “far”.
For example, if an attempt has been made to access $00C000_H$, the contents of the ROM at $FFC000_H$ are accessed. Since the ROM area of the FF bank exceeds 48 Kbytes, the whole area cannot be reflected in the image for the 00 bank. The ROM data at $FF4000_H$ to $FFFFFF_H$ looks, therefore, as if it were the image for 004000_H to $00FFFF_H$. Thus, it is recommended that the ROM data table be stored in the area of $FF4000_H$ to $FFFFFF_H$.

Address	Register	Abbreviation	Access	Peripheral	Initial value
48H	PPG8 Operation Mode Control Register	PPGC8	R/W	16-bit Programmable Pulse Generator 8/9	0 _ 0 0 0 _ _ 1B
49H	PPG9 Operation Mode Control Register	PPGC9	R/W		0 _ 0 0 0 0 0 1B
4AH	PPG8,9 Output Pin Control Register	PPG89	R/W		0 0 0 0 0 0 0 0B
4BH	Reserved				
4CH	PPGA Operation Mode Control Register	PPGCA	R/W	16-bit Programmable Pulse Generator A/B	0 _ 0 0 0 _ _ 1B
4DH	PPGB Operation Mode Control Register	PPGCB	R/W		0 _ 0 0 0 0 0 1B
4EH	PPGA,B Output Pin Control Register	PPGAB	R/W		0 0 0 0 0 0 0 0B
4FH	Reserved				
50H	Timer Control Status Register 0 (low-order)	TMCSR0	R/W	16-bit Reload Timer 0	0 0 0 0 0 0 0 0B
51H	Timer Control Status Register 0 (high-order)	TMCSR0	R/W		_ _ _ _ 0 0 0 0B
52H	Timer Control Status Register 1 (low-order)	TMCSR1	R/W	16-bit Reload Timer 1	0 0 0 0 0 0 0 0B
53H	Timer Control Status Register 1 (high-order)	TMCSR1	R/W		_ _ _ _ 0 0 0 0B
54H	Input Capture Control Status Register 0/1	ICS01	R/W	Input Capture 0/1	0 0 0 0 0 0 0 0B
55H	Input Capture Control Status Register 2/3	ICS23	R/W	Input Capture 2/3	0 0 0 0 0 0 0 0B
56H	Input Capture Control Status Register 4/5	ICS45	R/W	Input Capture 4/5	0 0 0 0 0 0 0 0B
57H	Reserved				
58H	Output Compare Control Status Register 0	OCS0	R/W	Output Compare 0/1	0 0 0 0 _ _ 0 0B
59H	Output Compare Control Status Register 1	OCS1	R/W		_ _ _ 0 0 0 0 0B
5AH	Output Compare Control Status Register 2	OCS2	R/W	Output Compare 2/3	0 0 0 0 _ _ 0 0B
5BH	Output Compare Control Status Register 3	OCS3	R/W		_ _ _ 0 0 0 0 0B
5CH	Output Compare Control Status Register 4	OCS4	R/W	Output Compare 4/5	0 0 0 0 _ _ 0 0B
5DH	Output Compare Control Status Register 5	OCS5	R/W		_ _ _ 0 0 0 0 0B
5EH	Sound Control Register (low-order)	SGCR	R/W	Sound Generator	0 0 0 0 0 0 0 0B
5FH	Sound Control Register (high-order)	SGCR	R/W		0 _ _ _ _ _ _ 0B

(Continued)

Address	Register	Abbreviation	Access	Peripheral	Initial value
60H	Watch Timer Control Register (low-order)	WTCR	R/W	Watch Timer	0 0 0 _ _ 0 0 0B
61H	Watch Timer Control Register (high-order)	WTCR	R/W		0 0 0 0 0 0 0 0B
62H	PWM Control Register 0	PWC0	R/W	Stepping Motor Controller 0	0 0 0 0 0 _ _ 0B
63H	Reserved				
64H	PWM Control Register 1	PWC1	R/W	Stepping Motor Controller 1	0 0 0 0 0 _ _ 0B
65H	Reserved				
66H	PWM Control Register 2	PWC2	R/W	Stepping Motor Controller 2	0 0 0 0 0 _ _ 0B
67H	Reserved				
68H	PWM Control Register 3	PWC3	R/W	Stepping Motor Controller 3	0 0 0 0 0 _ _ 0B
69H to 6CH	Reserved				
6DH	Serial I/O Prescaler Register	CDCR	R/W	Prescaler (Serial I/O)	0 XXX 1 1 1 1B
6EH	Timer Control Status Register	TCCS	R/W	16-bit Free-run Timer	0 0 0 0 0 0 0 0B
6FH	ROM Mirror Function Select Register	ROMM	W	ROM Mirror	XXXXXXX1B
70H to 8FH	Reserved for CAN Interface 0/1. Refer to section about CAN Controller				
90H to 9DH	Reserved				
9EH	Program Address Detection Control Status Register	PACSR	R/W	Address Match Detection Function	0 0 0 0 0 0 0 0B
9FH	Delayed Interrupt/Release Register	DIRR	R/W	Delayed Interrupt	_ _ _ _ _ _ _ 0B
A0H	Low Power Mode Control Register	LPMCR	R/W	Low Power Controller	0 0 0 1 1 0 0 0B
A1H	Clock Selection Register	CKSCR	R/W	Low Power Controller	1 1 1 1 1 1 0 0B
A2H to A7H	Reserved				
A8H	Watchdog Timer Control Register	WDTC	R/W	Watchdog Timer	XXXXX 1 1 1B
A9H	Time Base Timer Control Register	TBTC	R/W	Time Base Timer	1 - - 0 0 1 0 0B
AAH to ADH	Reserved				
AEH	Flash Memory Control Status Register (Flash product only. Otherwise reserved)	FMCS	R/W	Flash Memory	0 0 0 X 0 0 0 0B
AFH	Reserved				

(Continued)

Address	Register	Abbreviation	Access	Peripheral	Initial value
1910H	Reload L Register	PRLL8	R/W	16-bit Programmable Pulse Generator 8/9	XXXXXXXXB
1911H	Reload H Register	PRLH8	R/W		XXXXXXXXB
1912H	Reload L Register	PRLL9	R/W		XXXXXXXXB
1913H	Reload H Register	PRLH9	R/W		XXXXXXXXB
1914H	Reload L Register	PRLLA	R/W	16-bit Programmable Pulse Generator A/B	XXXXXXXXB
1915H	Reload H Register	PRLHA	R/W		XXXXXXXXB
1916H	Reload L Register	PRLLB	R/W		XXXXXXXXB
1917H	Reload H Register	PRLHB	R/W		XXXXXXXXB
1918H to 191FH	Reserved				
1920H	Input Capture Register 0 (low-order)	IPCP0	R	Input Capture 0/1	XXXXXXXXB
1921H	Input Capture Register 0 (high-order)	IPCP0	R		XXXXXXXXB
1922H	Input Capture Register 1 (low-order)	IPCP1	R		XXXXXXXXB
1923H	Input Capture Register 1 (high-order)	IPCP1	R		XXXXXXXXB
1924H	Input Capture Register 2 (low-order)	IPCP2	R	Input Capture 2/3	XXXXXXXXB
1925H	Input Capture Register 2 (high-order)	IPCP2	R		XXXXXXXXB
1926H	Input Capture Register 3 (low-order)	IPCP3	R		XXXXXXXXB
1927H	Input Capture Register 3 (high-order)	IPCP3	R		XXXXXXXXB
1928H	Input Capture Register 4 (low-order)	IPCP4	R	Input Capture 4/5	XXXXXXXXB
1929H	Input Capture Register 4 (high-order)	IPCP4	R		XXXXXXXXB
192AH	Input Capture Register 5 (low-order)	IPCP5	R		XXXXXXXXB
192BH	Input Capture Register 5 (high-order)	IPCP5	R		XXXXXXXXB
192CH to 192FH	Reserved				

(Continued)

Address	Register	Abbreviation	Access	Peripheral	Initial value
1930H	Output Compare Register 0 (low-order)	OCCP0	R/W	Output Compare 0/1	XXXXXXXXB
1931H	Output Compare Register 0 (high-order)	OCCP0	R/W		XXXXXXXXB
1932H	Output Compare Register 1 (low-order)	OCCP1	R/W		XXXXXXXXB
1933H	Output Compare Register 1 (high-order)	OCCP1	R/W		XXXXXXXXB
1934H	Output Compare Register 2 (low-order)	OCCP2	R/W	Output Compare 2/3	XXXXXXXXB
1935H	Output Compare Register 2 (high-order)	OCCP2	R/W		XXXXXXXXB
1936H	Output Compare Register 3 (low-order)	OCCP3	R/W		XXXXXXXXB
1937H	Output Compare Register 3 (high-order)	OCCP3	R/W		XXXXXXXXB
1938H	Output Compare Register 4 (low-order)	OCCP4	R/W	Output Compare 4/5	XXXXXXXXB
1939H	Output Compare Register 4 (high-order)	OCCP4	R/W		XXXXXXXXB
193AH	Output Compare Register 5 (low-order)	OCCP5	R/W		XXXXXXXXB
193BH	Output Compare Register 5 (high-order)	OCCP5	R/W		XXXXXXXXB
193CH to 193FH	Reserved				
1940H	Timer 0/Reload Register 0 (low-order)	TMR0/TMRLR0	R/W	16-bit Reload Timer 0	XXXXXXXXB
1941H	Timer 0/Reload Register 0 (high-order)	TMR0/TMRLR0	R/W		XXXXXXXXB
1942H	Timer 1/Reload Register 1 (low-order)	TMR1/TMRLR1	R/W	16-bit Reload Timer 1	XXXXXXXXB
1943H	Timer 1/Reload Register 1 (high-order)	TMR1/TMRLR1	R/W		XXXXXXXXB
1944H	Timer Data Register (low-order)	TCDT	R/W	16-bit Free-run Timer	00000000B
1945H	Timer Data Register (high-order)	TCDT	R/W		00000000B
1946H	Frequency Data Register	SGFR	R/W	Sound Generator	XXXXXXXXB
1947H	Amplitude Data Register	SGAR	R/W		XXXXXXXXB
1948H	Decrement Grade Register	SGDR	R/W		XXXXXXXXB
1949H	Tone Count Register	SGTR	R/W		XXXXXXXXB

(Continued)

Address	Register	Abbreviation	Access	Peripheral	Initial value
194A$_H$	Sub-second Data Register (low-order)	WTBR	R/W	Watch Timer	XXXXXXXX$_B$
194B$_H$	Sub-second Data Register (middle-order)	WTBR	R/W		XXXXXXXX$_B$
194C$_H$	Sub-second Data Register (high-order)	WTBR	R/W		_ _ _ XXXXX$_B$
194D$_H$	Second Data Register	WTSR	R/W		_ _ 0 0 0 0 0 0 $_B$
194E$_H$	Minute Data Register	WTMR	R/W	Watch Timer	_ _ 0 0 0 0 0 0 $_B$
194F$_H$	Hour Data Register	WTHR	R/W		_ _ _ 0 0 0 0 0 $_B$
1950$_H$	PWM1 Compare Register 0	PWC10	R/W	Stepping Motor Controller 0	XXXXXXXX$_B$
1951$_H$	PWM2 Compare Register 0	PWC20	R/W		XXXXXXXX$_B$
1952$_H$	PWM1 Select Register 0	PWS10	R/W		_ _ 0 0 0 0 0 0 $_B$
1953$_H$	PWM2 Select Register 0	PWS20	R/W		_ 0 0 0 0 0 0 0 $_B$
1954$_H$	PWM1 Compare Register 1	PWC11	R/W	Stepping Motor Controller 1	XXXXXXXX$_B$
1955$_H$	PWM2 Compare Register 1	PWC21	R/W		XXXXXXXX$_B$
1956$_H$	PWM1 Select Register 1	PWS11	R/W		_ _ 0 0 0 0 0 0 $_B$
1957$_H$	PWM2 Select Register 1	PWS21	R/W		_ 0 0 0 0 0 0 0 $_B$
1958$_H$	PWM1 Compare Register 2	PWC12	R/W	Stepping Motor Controller 2	XXXXXXXX$_B$
1959$_H$	PWM2 Compare Register 2	PWC22	R/W		XXXXXXXX$_B$
195A$_H$	PWM1 Select Register 2	PWS12	R/W		_ _ 0 0 0 0 0 0 $_B$
195B$_H$	PWM2 Select Register 2	PWS22	R/W		_ 0 0 0 0 0 0 0 $_B$
195C$_H$	PWM1 Compare Register 3	PWC13	R/W	Stepping Motor Controller 3	XXXXXXXX$_B$
195D$_H$	PWM2 Compare Register 3	PWC23	R/W		XXXXXXXX$_B$
195E$_H$	PWM1 Select Register 3	PWS13	R/W		_ _ 0 0 0 0 0 0 $_B$
195F$_H$	PWM2 Select Register 3	PWS23	R/W		_0 0 0 0 0 0 0 $_B$
1960$_H$ to 19FF$_H$	Reserved				
1A00$_H$ to 1AFF$_H$	CAN Interface 0. Refer to section about CAN Controller				
1B00$_H$ to 1BFF$_H$	CAN Interface 1. Refer to section about CAN Controller				
1C00$_H$ to 1CFF$_H$	CAN Interface 0. Refer to section about CAN Controller				
1D00$_H$ to 1DFF$_H$	CAN Interface 1. Refer to section about CAN Controller				
1E00$_H$ to 1EFF$_H$	Reserved				

(Continued)

9. CAN Controllers

The CAN controller has the following features : Conforms to CAN Specification Version 2.0 Part A and B

- Supports transmission/reception in standard frame and extended frame formats
- Supports transmission of data frames by receiving remote frames
- 16 transmitting/receiving message buffers
  - 29-bit ID and 8-byte data
  - Multi-level message buffer configuration
- Provides full-bit comparison, full-bit mask, acceptance register 0/acceptance register 1 for each message buffer as 1D acceptance mask
  - Two acceptance mask registers in either standard frame format or extended frame formats
- Bit rate programmable from 10 Kbit/s to 2 Mbit/s (when input clock is at 16 MHz)

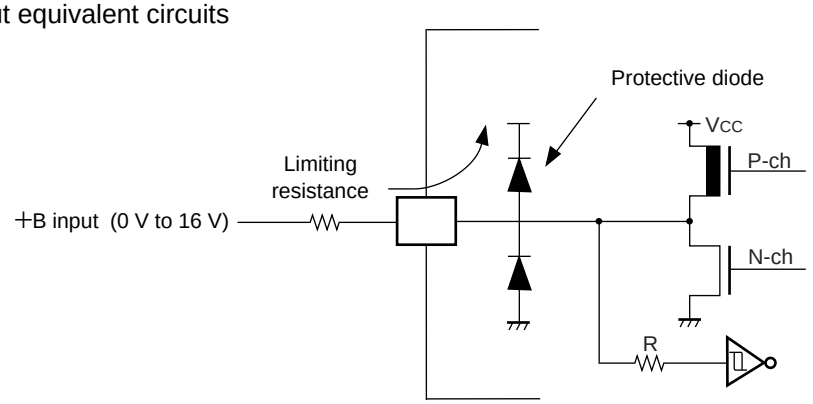
List of Control Registers

Address		Register	Abbreviation	Access	Initial Value
CAN0	CAN1				
000070H	000080H	Message buffer valid register	BVALR	R/W	00000000 00000000B
000071H	000081H				
000072H	000082H	Transmit request register	TREQR	R/W	00000000 00000000B
000073H	000083H				
000074H	000084H	Transmit cancel register	TCANR	W	00000000 00000000B
000075H	000085H				
000076H	000086H	Transmit complete register	TCR	R/W	00000000 00000000B
000077H	000087H				
000078H	000088H	Receive complete register	RCR	R/W	00000000 00000000B
000079H	000089H				
00007AH	00008AH	Remote request receiving register	RRTRR	R/W	00000000 00000000B
00007BH	00008BH				
00007CH	00008CH	Receive overrun register	ROVRR	R/W	00000000 00000000B
00007DH	00008DH				
00007EH	00008EH	Receive interrupt enable register	RIER	R/W	00000000 00000000B
00007FH	00008FH				

(Continued)

- Note that if a +B signal is input when the microcontroller power supply is off (not fixed at 0 V) , the power supply is provided from the pins, so that incomplete operation may result.
- Note that if the +B input is applied during power-on, the power supply is provided from the pins and the resulting supply voltage may not be sufficient to operate the power-on reset.
- Care must be taken not to leave the +B input pin open.
- Note that analog system input/output pins other than the A/D input pins (LCD drive pins, comparator input pins, etc.) cannot accept +B signal input.
- Sample recommended circuits

• Input/Output equivalent circuits



Note: : Average output current = operating current × operating efficiency

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

11.2 Recommended Conditions

(V_{SS} = AV_{SS} = 0.0 V)

Parameter	Symbol	Value			Unit	Remarks	
		Min	Typ	Max			
Power supply voltage	V_{CC} AV_{CC}	4.5	5.0	5.5	V	Under normal operation	MB90V590G MB90F594G MB90594G
		3.0	—	5.5	V	Maintains RAM data in stop mode	
		4.75	5.0	5.25	V	Under normal operation	MB90F591G MB90591G
		3.0	—	5.25	V	Maintains RAM data in stop mode	
Smooth capacitor	C_S	0.022	0.1	1.0	µF	*	
Operating temperature	T_A	–40	—	+85	°C		

* : Use a ceramic capacitor or a capacitor with equivalent frequency characteristics. The smoothing capacitor to be connected to the V_{CC} pin must have a capacitance value higher than C_S.

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their representatives beforehand.

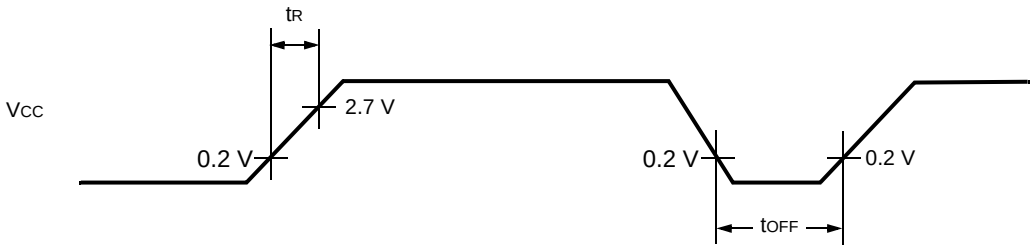
11.4.3 Power On Reset

(MB90V590G, MB90F594G, MB90594G : V_{CC} = 5.0 V±10 %, V_{SS} = AV_{SS} = 0.0 V, T_A = −40 °C to +85 °C)
(MB90F591G, MB90591G : V_{CC} = 5.0 V±5 %, V_{SS} = AV_{SS} = 0.0 V, T_A = −40 °C to +85 °C)

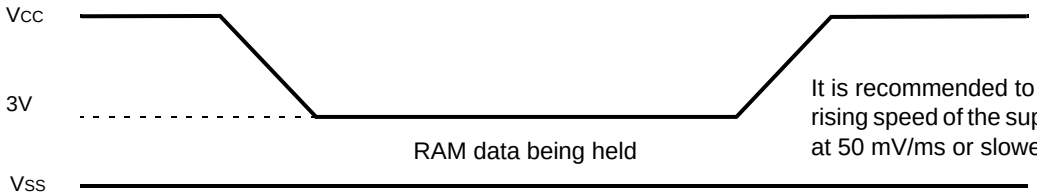
Parameter	Symbol	Pin name	Condition	Value		Unit	Remarks
				Min	Max		
Power on rise time	t_R	V_{CC}	—	0.05	30	ms	
Power off time	t_{OFF}	V_{CC}		50	—	ms	Due to repetitive operation

Notes:

- V_{CC} must be kept lower than 0.2 V before power-on.
- The above values are used for creating a power-on reset.
- Some registers in the device are initialized only upon a power-on reset. To initialize these register, turn on the power supply using the above values.

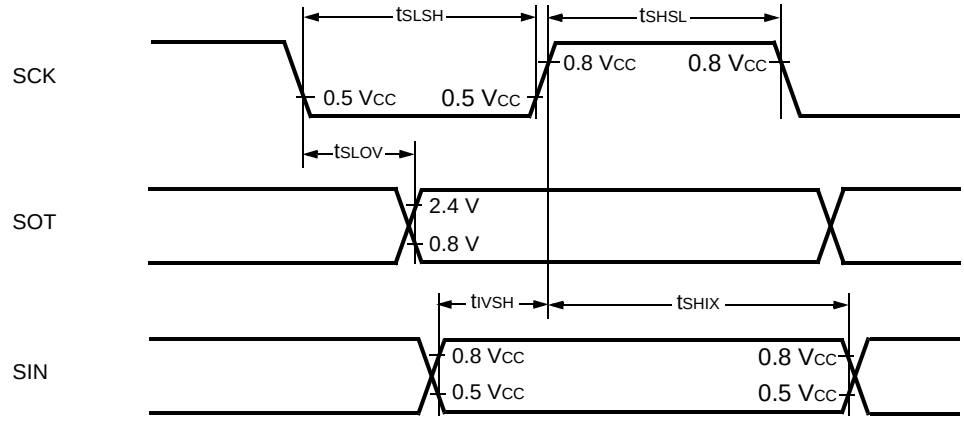


Sudden changes in the power supply voltage may cause a power-on reset.
To change the power supply voltage while the device is in operation, it is recommended to raise the voltage smoothly to suppress fluctuations as shown below.
In this case, change the supply voltage with the PLL clock not used. If the voltage drop is 1 V or fewer per second, however, you can use the PLL clock.



It is recommended to keep the rising speed of the supply voltage at 50 mV/ms or slower.

• **External Shift Clock Mode**

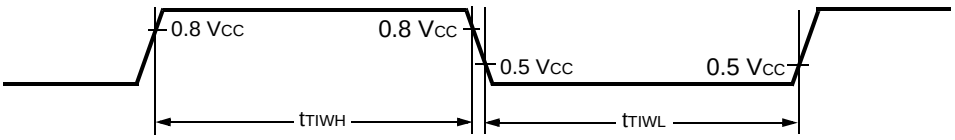


11.4.5 Timer Input Timing

(MB90V590G, MB90F594G, MB90594G : V_{CC} = 5.0 V±10 %, V_{SS} = AV_{SS} = 0.0 V, T_A = −40 °C to +85 °C)
(MB90F591G, MB90591G : V_{CC} = 5.0 V±5 %, V_{SS} = AV_{SS} = 0.0 V, T_A = −40 °C to +85 °C)

Parameter	Symbol	Pin name	Condition	Value		Unit	Remarks
				Min	Max		
Input pulse width	t_{TIWH}	TIN0	—	4 t_{CP}	—	ns	Under normal operation
	t_{TIWL}	IN0 to IN5		1	—	µs	In stop mode

• **Timer Input Timing**



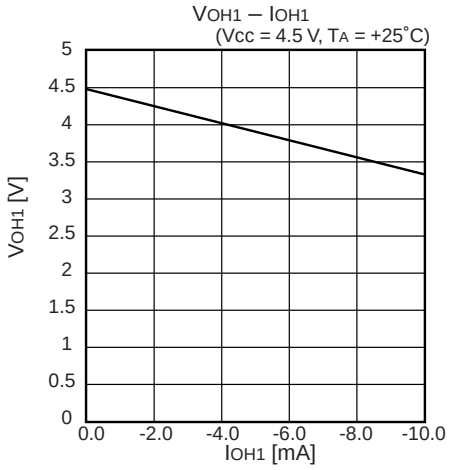
11.4.6 Trigger Input Timing

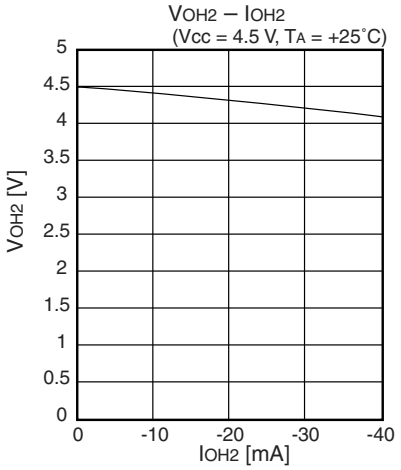
(MB90V590G, MB90F594G, MB90594G : V_{CC} = 5.0 V±10 %, V_{SS} = AV_{SS} = 0.0 V, T_A = −40 °C to +85 °C)
(MB90F591G, MB90591G : V_{CC} = 5.0 V±5 %, V_{SS} = AV_{SS} = 0.0 V, T_A = −40 °C to +85 °C)

Parameter	Symbol	Pin name	Condition	Value		Unit	Remarks
				Min	Max		
Input pulse width	t_{TRGH} t_{TRGL}	INT0 to INT7, ADTG	—	5 t_{CP}	—	ns	

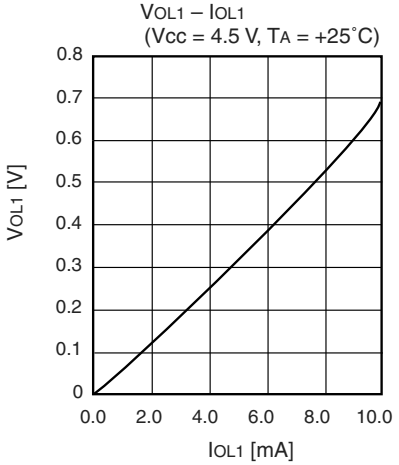
12. Example Characteristics

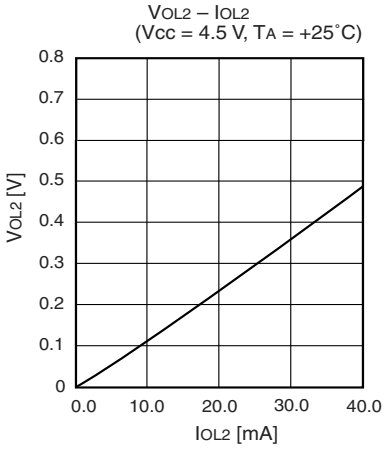
■ “H” Level Output Voltage



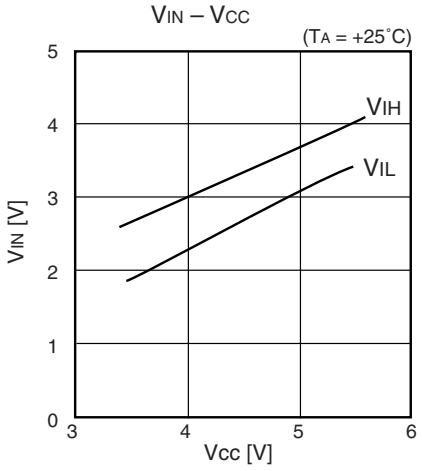


■ “L” Level Output





■ “H” Level Input Voltage/“L Level Input Voltage (Hysteresis Input)



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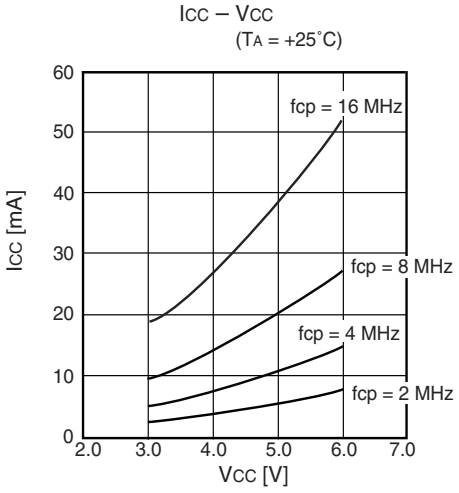
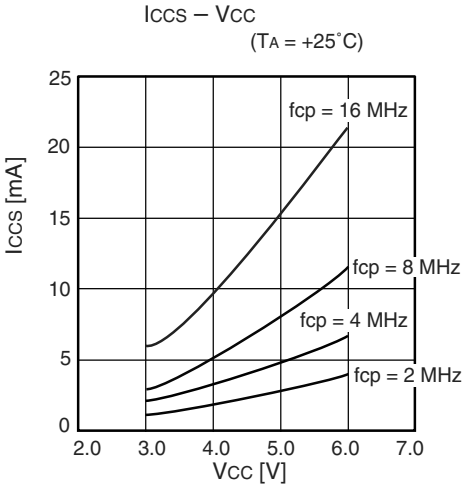
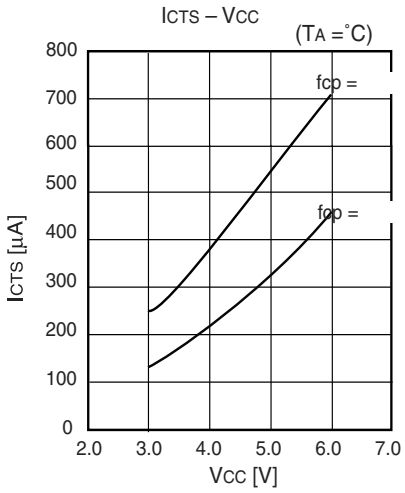
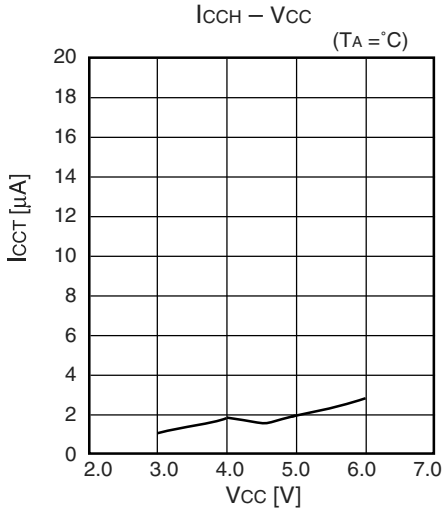
■ Power Supply Voltage









13. Ordering Information

Part number	Package	Remarks
MB90594GPF MB90F594GPF MB90F591GPF MB90591GPF	100-pin Plastic QFP (FPT-100P-M06)	
MB90V590GCR	256-pin Ceramic PGA (PGA-256C-A01)	For evaluation