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What is "Embedded - Microcontrollers"?

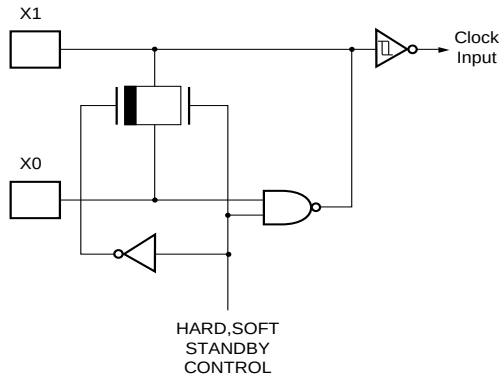
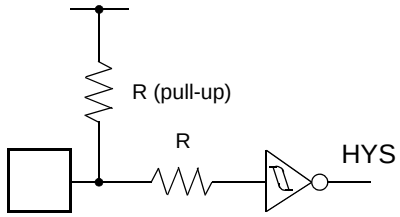
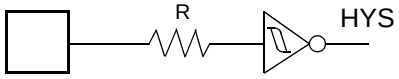
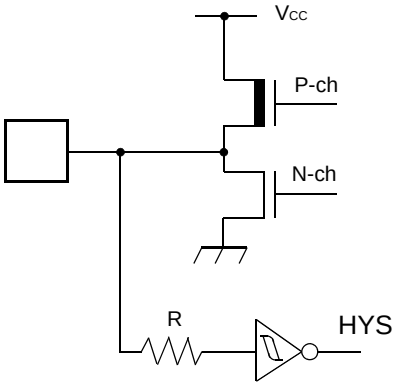
"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	F²MC-16LX
Core Size	16-Bit
Speed	16MHz
Connectivity	CANbus, EBI/EMI, SCI, Serial I/O, UART/USART
Peripherals	POR, PWM, WDT
Number of I/O	78
Program Memory Size	384KB (384K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.25V
Data Converters	A/D 8x8/10b
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-BQFP
Supplier Device Package	100-QFP (14x20)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/mb90f591gpf-ge1

Contents

4. I/O Circuit Type

Circuit Type	Circuit	Remarks
A		■ Oscillation feedback resistor : 1 MΩ approx.
B		■ Hysteresis input with pull-up resistor : 50 kΩ approx.
C		■ Hysteresis input
D		■ CMOS output ■ Hysteresis input

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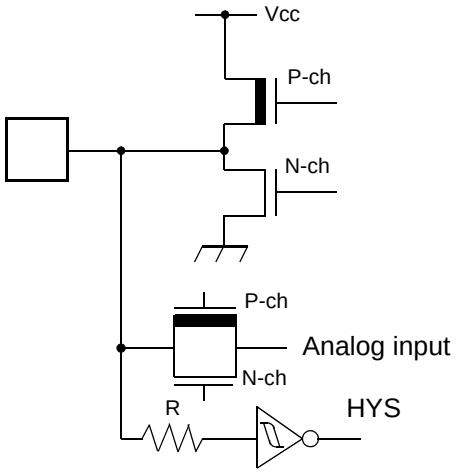
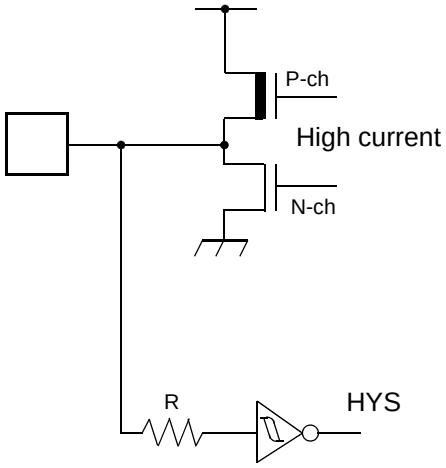
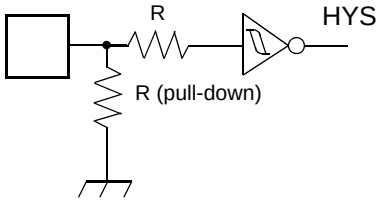
Circuit Type	Circuit	Remarks
E		■ CMOS output ■ Hysteresis input ■ Analog input
F		■ CMOS high current output ■ Hysteresis input
G		■ Hysteresis input with pull-down resistor : 50 kΩ approx. ■ Flash version does not have pull-down resistor.

(9) N.C. Pin
The N.C. (internally connected) pin must be opened for use.

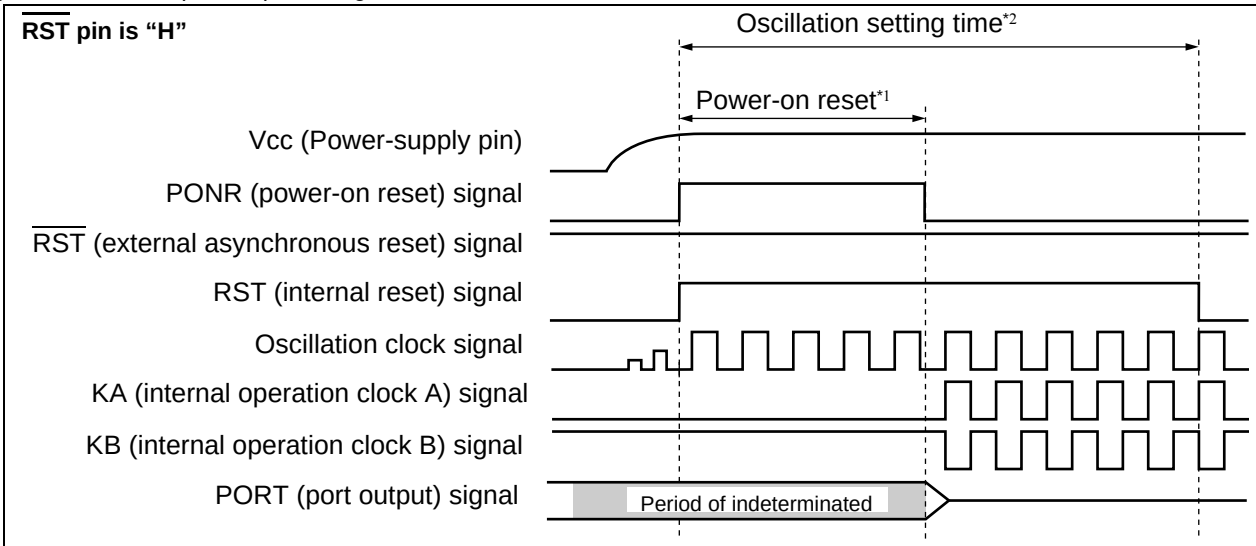
(10) Notes on Energization
To prevent the internal regulator circuit from malfunctioning, set the voltage rise time during energization at 50 µs or more (0.2 V to 2.7 V).

(11) Indeterminate outputs from ports 0 and 1 (without MB90F591G/591G, MB90F594G)
During oscillation setting time of step-down circuit (during a power-on reset) after the power is turned on, the outputs from ports 0 and 1 become following state.

■ If $\overline{RST}$ pin is “H”, the outputs become indeterminate.

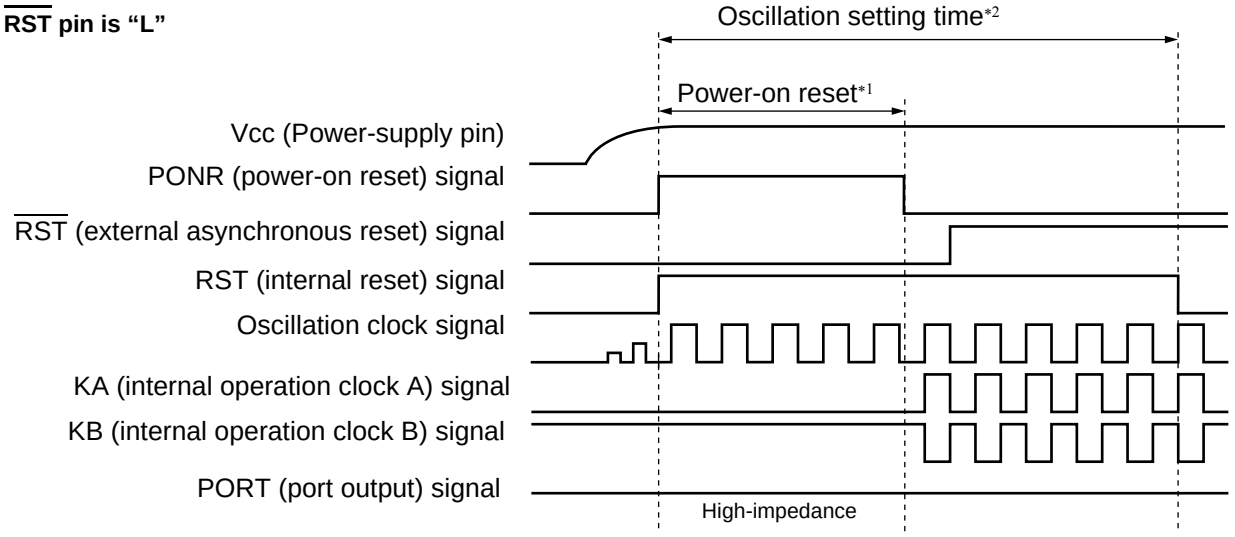
■ If $\overline{RST}$ pin is “L”, the outputs become high-impedance.
Pay attention to the port output timing shown as follow.

$\overline{RST}$ pin is “H”



*1 : Power-on reset time : "Period of clock frequency" × 2^{17} (Clock frequency of 16 MHz : 8.19 ms)
*2 : Oscillation setting time : "Period of clock frequency" × 2^{18} (Clock frequency of 16 MHz : 16.38ms)

$\overline{RST}$ pin is “L”



*1 : Power-on reset time : "Period of clock frequency" × 2^{17} (Clock frequency of 16 MHz : 8.19 ms)
*2 : Oscillation setting time : "Period of clock frequency" × 2^{18} (Clock frequency of 16 MHz : 16.38ms)

(12) Initialization

The device contains internal registers which are initialized only by a power-on reset. To initialize these registers, please turn on the power again.

(13) Directions of “DIV A, Ri” and “DIVW A, RWi” instructions

In the Signed multiplication and division instructions (“DIV A, Ri” and “DIVW A, RWi”), the value of the corresponding bank register (DTB, ADB, USB, SSB) is set in “00 $_H$”.

If the values of the corresponding bank registers (DTB,ADB,USB,SSB) are set to other than “00 $_H$”, the remainder by the execution result of the instruction is not stored in the register of the instruction operand.

(14) Using REALOS

The use of EI^{2}OS is not possible with the REALOS real time operating system.

(15) Caution on Operations during PLL Clock Mode

If the PLL clock mode is selected in the microcontroller, it may attempt to continue the operation using the free-running frequency of the automatic oscillating circuit in the PLL circuitry even if the oscillator is out of place or the clock input is stopped. Performance of this operation, however, cannot be guaranteed.

8. I/O Map

Address	Register	Abbreviation	Access	Peripheral	Initial value
00_H	Port 0 Data Register	PDR0	R/W	Port 0	XXXXXXXX$_B$
01_H	Port 1 Data Register	PDR1	R/W	Port 1	XXXXXXXX$_B$
02_H	Port 2 Data Register	PDR2	R/W	Port 2	XXXXXXXX$_B$
03_H	Port 3 Data Register	PDR3	R/W	Port 3	XXXXXXXX$_B$
04_H	Port 4 Data Register	PDR4	R/W	Port 4	XXXXXXXX$_B$
05_H	Port 5 Data Register	PDR5	R/W	Port 5	XXXXXXXX$_B$
06_H	Port 6 Data Register	PDR6	R/W	Port 6	XXXXXXXX$_B$
07_H	Port 7 Data Register	PDR7	R/W	Port 7	XXXXXXXX$_B$
08_H	Port 8 Data Register	PDR8	R/W	Port 8	XXXXXXXX$_B$
09_H	Port 9 Data Register	PDR9	R/W	Port 9	_ _ XXXXXX$_B$
$0A_H$ to $0F_H$	Reserved				
10_H	Port 0 Direction Register	DDR0	R/W	Port 0	0 0 0 0 0 0 0 0$_B$
11_H	Port 1 Direction Register	DDR1	R/W	Port 1	0 0 0 0 0 0 0 0$_B$
12_H	Port 2 Direction Register	DDR2	R/W	Port 2	0 0 0 0 0 0 0 0$_B$
13_H	Port 3 Direction Register	DDR3	R/W	Port 3	0 0 0 0 0 0 0 0$_B$
14_H	Port 4 Direction Register	DDR4	R/W	Port 4	0 0 0 0 0 0 0 0$_B$
15_H	Port 5 Direction Register	DDR5	R/W	Port 5	0 0 0 0 0 0 0 0$_B$
16_H	Port 6 Direction Register	DDR6	R/W	Port 6	0 0 0 0 0 0 0 0$_B$
17_H	Port 7 Direction Register	DDR7	R/W	Port 7	0 0 0 0 0 0 0 0$_B$
18_H	Port 8 Direction Register	DDR8	R/W	Port 8	0 0 0 0 0 0 0 0$_B$
19_H	Port 9 Direction Register	DDR9	R/W	Port 9	_ _ 0 0 0 0 0 0$_B$
$1A_H$	Reserved				
$1B_H$	Analog Input Enable Register	ADER	R/W	Port 6, A/D	1 1 1 1 1 1 1 1$_B$
$1C_H$ to $1F_H$	Reserved				
20_H	Serial Mode Control Register 0	UMC0	R/W	UART0	0 0 0 0 0 1 0 0$_B$
21_H	Serial Status Register 0	USR0	R/W		0 0 0 1 0 0 0 0$_B$
22_H	Serial Input/Output Data Register 0	UIDR0/UODR0	R/W		XXXXXXXX$_B$
23_H	Rate and Data Register 0	URD0	R/W		0 0 0 0 0 0 0X$_B$
24_H	Serial Mode Control Register 1	UMC1	R/W	UART1	0 0 0 0 0 1 0 0$_B$
25_H	Serial Status Register 1	USR1	R/W		0 0 0 1 0 0 0 0$_B$
26_H	Serial Input/Output Data Register 1	UIDR1/UODR1	R/W		XXXXXXXX$_B$
27_H	Rate and Data Register 1	URD1	R/W		0 0 0 0 0 0 0X$_B$

(Continued)

Address	Register	Abbreviation	Access	Peripheral	Initial value
60H	Watch Timer Control Register (low-order)	WTCR	R/W	Watch Timer	0 0 0 _ _ 0 0 0B
61H	Watch Timer Control Register (high-order)	WTCR	R/W		0 0 0 0 0 0 0 0B
62H	PWM Control Register 0	PWC0	R/W	Stepping Motor Controller 0	0 0 0 0 0 _ _ 0B
63H	Reserved				
64H	PWM Control Register 1	PWC1	R/W	Stepping Motor Controller 1	0 0 0 0 0 _ _ 0B
65H	Reserved				
66H	PWM Control Register 2	PWC2	R/W	Stepping Motor Controller 2	0 0 0 0 0 _ _ 0B
67H	Reserved				
68H	PWM Control Register 3	PWC3	R/W	Stepping Motor Controller 3	0 0 0 0 0 _ _ 0B
69H to 6CH	Reserved				
6DH	Serial I/O Prescaler Register	CDCR	R/W	Prescaler (Serial I/O)	0 XXX 1 1 1 1B
6EH	Timer Control Status Register	TCCS	R/W	16-bit Free-run Timer	0 0 0 0 0 0 0 0B
6FH	ROM Mirror Function Select Register	ROMM	W	ROM Mirror	XXXXXXX1B
70H to 8FH	Reserved for CAN Interface 0/1. Refer to section about CAN Controller				
90H to 9DH	Reserved				
9EH	Program Address Detection Control Status Register	PACSR	R/W	Address Match Detection Function	0 0 0 0 0 0 0 0B
9FH	Delayed Interrupt/Release Register	DIRR	R/W	Delayed Interrupt	_ _ _ _ _ _ _ 0B
A0H	Low Power Mode Control Register	LPMCR	R/W	Low Power Controller	0 0 0 1 1 0 0 0B
A1H	Clock Selection Register	CKSCR	R/W	Low Power Controller	1 1 1 1 1 1 0 0B
A2H to A7H	Reserved				
A8H	Watchdog Timer Control Register	WDTC	R/W	Watchdog Timer	XXXXX 1 1 1B
A9H	Time Base Timer Control Register	TBTC	R/W	Time Base Timer	1 - - 0 0 1 0 0B
AAH to ADH	Reserved				
AEH	Flash Memory Control Status Register (Flash product only. Otherwise reserved)	FMCS	R/W	Flash Memory	0 0 0 X 0 0 0 0B
AFH	Reserved				

(Continued)

Address	Register	Abbreviation	Access	Peripheral	Initial value
1930H	Output Compare Register 0 (low-order)	OCCP0	R/W	Output Compare 0/1	XXXXXXXXB
1931H	Output Compare Register 0 (high-order)	OCCP0	R/W		XXXXXXXXB
1932H	Output Compare Register 1 (low-order)	OCCP1	R/W		XXXXXXXXB
1933H	Output Compare Register 1 (high-order)	OCCP1	R/W		XXXXXXXXB
1934H	Output Compare Register 2 (low-order)	OCCP2	R/W	Output Compare 2/3	XXXXXXXXB
1935H	Output Compare Register 2 (high-order)	OCCP2	R/W		XXXXXXXXB
1936H	Output Compare Register 3 (low-order)	OCCP3	R/W		XXXXXXXXB
1937H	Output Compare Register 3 (high-order)	OCCP3	R/W		XXXXXXXXB
1938H	Output Compare Register 4 (low-order)	OCCP4	R/W	Output Compare 4/5	XXXXXXXXB
1939H	Output Compare Register 4 (high-order)	OCCP4	R/W		XXXXXXXXB
193AH	Output Compare Register 5 (low-order)	OCCP5	R/W		XXXXXXXXB
193BH	Output Compare Register 5 (high-order)	OCCP5	R/W		XXXXXXXXB
193CH to 193FH	Reserved				
1940H	Timer 0/Reload Register 0 (low-order)	TMR0/TMRLR0	R/W	16-bit Reload Timer 0	XXXXXXXXB
1941H	Timer 0/Reload Register 0 (high-order)	TMR0/TMRLR0	R/W		XXXXXXXXB
1942H	Timer 1/Reload Register 1 (low-order)	TMR1/TMRLR1	R/W	16-bit Reload Timer 1	XXXXXXXXB
1943H	Timer 1/Reload Register 1 (high-order)	TMR1/TMRLR1	R/W		XXXXXXXXB
1944H	Timer Data Register (low-order)	TCDT	R/W	16-bit Free-run Timer	00000000B
1945H	Timer Data Register (high-order)	TCDT	R/W		00000000B
1946H	Frequency Data Register	SGFR	R/W	Sound Generator	XXXXXXXXB
1947H	Amplitude Data Register	SGAR	R/W		XXXXXXXXB
1948H	Decrement Grade Register	SGDR	R/W		XXXXXXXXB
1949H	Tone Count Register	SGTR	R/W		XXXXXXXXB

(Continued)

Address	Register	Abbreviation	Access	Peripheral	Initial value
194A$_H$	Sub-second Data Register (low-order)	WTBR	R/W	Watch Timer	XXXXXXXX$_B$
194B$_H$	Sub-second Data Register (middle-order)	WTBR	R/W		XXXXXXXX$_B$
194C$_H$	Sub-second Data Register (high-order)	WTBR	R/W		_ _ _ XXXXX$_B$
194D$_H$	Second Data Register	WTSR	R/W		_ _ 0 0 0 0 0 0 $_B$
194E$_H$	Minute Data Register	WTMR	R/W	Watch Timer	_ _ 0 0 0 0 0 0 $_B$
194F$_H$	Hour Data Register	WTHR	R/W		_ _ _ 0 0 0 0 0 $_B$
1950$_H$	PWM1 Compare Register 0	PWC10	R/W	Stepping Motor Controller 0	XXXXXXXX$_B$
1951$_H$	PWM2 Compare Register 0	PWC20	R/W		XXXXXXXX$_B$
1952$_H$	PWM1 Select Register 0	PWS10	R/W		_ _ 0 0 0 0 0 0 $_B$
1953$_H$	PWM2 Select Register 0	PWS20	R/W		_ 0 0 0 0 0 0 0 $_B$
1954$_H$	PWM1 Compare Register 1	PWC11	R/W	Stepping Motor Controller 1	XXXXXXXX$_B$
1955$_H$	PWM2 Compare Register 1	PWC21	R/W		XXXXXXXX$_B$
1956$_H$	PWM1 Select Register 1	PWS11	R/W		_ _ 0 0 0 0 0 0 $_B$
1957$_H$	PWM2 Select Register 1	PWS21	R/W		_ 0 0 0 0 0 0 0 $_B$
1958$_H$	PWM1 Compare Register 2	PWC12	R/W	Stepping Motor Controller 2	XXXXXXXX$_B$
1959$_H$	PWM2 Compare Register 2	PWC22	R/W		XXXXXXXX$_B$
195A$_H$	PWM1 Select Register 2	PWS12	R/W		_ _ 0 0 0 0 0 0 $_B$
195B$_H$	PWM2 Select Register 2	PWS22	R/W		_ 0 0 0 0 0 0 0 $_B$
195C$_H$	PWM1 Compare Register 3	PWC13	R/W	Stepping Motor Controller 3	XXXXXXXX$_B$
195D$_H$	PWM2 Compare Register 3	PWC23	R/W		XXXXXXXX$_B$
195E$_H$	PWM1 Select Register 3	PWS13	R/W		_ _ 0 0 0 0 0 0 $_B$
195F$_H$	PWM2 Select Register 3	PWS23	R/W		_0 0 0 0 0 0 0 $_B$
1960$_H$ to 19FF$_H$	Reserved				
1A00$_H$ to 1AFF$_H$	CAN Interface 0. Refer to section about CAN Controller				
1B00$_H$ to 1BFF$_H$	CAN Interface 1. Refer to section about CAN Controller				
1C00$_H$ to 1CFF$_H$	CAN Interface 0. Refer to section about CAN Controller				
1D00$_H$ to 1DFF$_H$	CAN Interface 1. Refer to section about CAN Controller				
1E00$_H$ to 1EFF$_H$	Reserved				

(Continued)

9. CAN Controllers

The CAN controller has the following features : Conforms to CAN Specification Version 2.0 Part A and B

- Supports transmission/reception in standard frame and extended frame formats
- Supports transmission of data frames by receiving remote frames
- 16 transmitting/receiving message buffers
  - 29-bit ID and 8-byte data
  - Multi-level message buffer configuration
- Provides full-bit comparison, full-bit mask, acceptance register 0/acceptance register 1 for each message buffer as 1D acceptance mask
  - Two acceptance mask registers in either standard frame format or extended frame formats
- Bit rate programmable from 10 Kbit/s to 2 Mbit/s (when input clock is at 16 MHz)

List of Control Registers

Address		Register	Abbreviation	Access	Initial Value
CAN0	CAN1				
000070H	000080H	Message buffer valid register	BVALR	R/W	00000000 00000000B
000071H	000081H				
000072H	000082H	Transmit request register	TREQR	R/W	00000000 00000000B
000073H	000083H				
000074H	000084H	Transmit cancel register	TCANR	W	00000000 00000000B
000075H	000085H				
000076H	000086H	Transmit complete register	TCR	R/W	00000000 00000000B
000077H	000087H				
000078H	000088H	Receive complete register	RCR	R/W	00000000 00000000B
000079H	000089H				
00007AH	00008AH	Remote request receiving register	RRTRR	R/W	00000000 00000000B
00007BH	00008BH				
00007CH	00008CH	Receive overrun register	ROVRR	R/W	00000000 00000000B
00007DH	00008DH				
00007EH	00008EH	Receive interrupt enable register	RIER	R/W	00000000 00000000B
00007FH	00008FH				

(Continued)

List of Message Buffers (DLC Registers and Data Registers)

Address		Register	Abbreviation	Access	Initial Value
CAN0	CAN1				
001A60H	001B60H	DLC register 0	DLCR0	R/W	----XXXXB
001A61H	001B61H				
001A62H	001B62H	DLC register 1	DLCR1	R/W	----XXXXB
001A63H	001B63H				
001A64H	001B64H	DLC register 2	DLCR2	R/W	----XXXXB
001A65H	001B65H				
001A66H	001B66H	DLC register 3	DLCR3	R/W	----XXXXB
001A67H	001B67H				
001A68H	001B68H	DLC register 4	DLCR4	R/W	----XXXXB
001A69H	001B69H				
001A6AH	001B6AH	DLC register 5	DLCR5	R/W	----XXXXB
001A6BH	001B6BH				
001A6CH	001B6CH	DLC register 6	DLCR6	R/W	----XXXXB
001A6DH	001B6DH				
001A6EH	001B6EH	DLC register 7	DLCR7	R/W	----XXXXB
001A6FH	001B6FH				
001A70H	001B70H	DLC register 8	DLCR8	R/W	----XXXX
001A71H	001B71H				
001A72H	001B72H	DLC register 9	DLCR9	R/W	----XXXXB
001A73H	001B73H				
001A74H	001B74H	DLC register 10	DLCR10	R/W	----XXXXB
001A75H	001B75H				
001A76H	001B76H	DLC register 11	DLCR11	R/W	----XXXXB
001A77H	001B77H				
001A78H	001B78H	DLC register 12	DLCR12	R/W	----XXXXB
001A79H	001B79H				
001A7AH	001B7AH	DLC register 13	DLCR13	R/W	----XXXXB
001A7BH	001B7BH				
001A7CH	001B7CH	DLC register 14	DLCR14	R/W	----XXXXB
001A7DH	001B7DH				
001A7EH	001B7EH	DLC register 15	DLCR15	R/W	----XXXXB
001A7FH	001B7FH				
001A80H to 001A87H	001B80H to 001B87H	Data register 0 (8 bytes)	DTR0	R/W	XXXXXXXXB to XXXXXXXXB

(Continued)

11. Electrical Characteristics

11.1 Absolute Maximum Ratings

(V_{SS} = AV_{SS} = 0.0 V)

Parameter	Symbol	Rating		Unit	Remarks
		Min	Max		
Power supply voltage	V_{CC}	V_{SS} − 0.3	V_{SS} + 6.0	V	
	AV_{CC}	V_{SS} − 0.3	V_{SS} + 6.0	V	V_{CC} = AV_{CC} *1
	AVRH, AVRL	V_{SS} − 0.3	V_{SS} + 6.0	V	AV_{CC} ≥ AVRH/L, AVRH ≥ AVRL *1
	DV_{CC}	V_{SS} − 0.3	V_{SS} + 6.0	V	V_{CC} ≥ DV_{CC}
Input voltage	V_I	V_{SS} − 0.3	V_{SS} + 6.0	V	*2
Output voltage	V_O	V_{SS} − 0.3	V_{SS} + 6.0	V	*2
Max clamp current	I_{CLAMP}	−2.0	+ 2.0	mA	*6
Total Max clamp current	$\sum \lvert I_{CLAMP} \rvert$	—	20	mA	*6
“L” level Max output current	I_{OL1}	—	15	mA	Normal output *3
“L” level avg. output current	I_{OLAV1}	—	4	mA	Normal output, average value *4
“L” level Max output current	I_{OL2}	—	40	mA	High current output *3
“L” level avg. output current	I_{OLAV2}	—	30	mA	High current output, average value *4
“L” level Max overall output current	$\sum I_{OL1}$	—	100	mA	Total normal output
“L” level Max overall output current	$\sum I_{OL2}$		330	mA	Total high current output
“L” level avg. overall output current	$\sum I_{OLAV1}$	—	50	mA	Total normal output, average value *5
“L” level avg. overall output current	$\sum I_{OLAV2}$		250	mA	Total high current output, average value *5
“H” level Max output current	I_{OH1}	—	–15	mA	Normal output *3
“H” level avg. output current	I_{OHAV1}	—	–4	mA	Normal output, average value *4
“H” level Max output current	I_{OH2}	—	–40	mA	High current output *3
“H” level avg. output current	I_{OHAV2}	—	–30	mA	High current output, average value *4
“H” level Max overall output current	$\sum I_{OH1}$	—	–100	mA	Total normal output
“H” level Max overall output current	$\sum I_{OH2}$	—	–330	mA	Total high current output
“H” level avg. overall output current	$\sum I_{OHAV1}$	—	–50	mA	Total normal output, average value *5
“H” level avg. overall output current	$\sum I_{OHAV2}$	—	–250	mA	Total high current output, average value *5
Power consumption	P_D	—	500	mW	MB90F594G, MB90F591G
		—	400	mW	MB90594G, MB90591G
Operating temperature	T_A	–40	+85	°C	
Storage temperature	T_{STG}	–55	+150	°C	

*1 : AV_{CC}, AVRH, AVRL and DV_{CC} shall not exceed V_{CC}. AVRH and AVRL shall not exceed AV_{CC}.
Also, AVRL shall not exceed AVRH.

*2 : V_I and V_O should not exceed V_{CC} + 0.3V. V_I should not exceed the specified ratings. However if the maximum current to/from an input is limited by some means with external components, the I_{CLAMP} rating supersedes the V_I rating.

*3 : The maximum output current is a peak value for a corresponding pin.

*4 : Average output current is an average current value observed for a 100 ms period for a corresponding pin.

*5 : Total average current is an average current value observed for a 100 ms period for all corresponding pins.

*6 :

- Applicable to pins : P00 to P07, P10 to P17, P20 to P27, P30 to P37, P40 to P47, P50 to P57, P60 to P67, P70 to P77, P80 to P87, P90 toP95
- Use within recommended operating conditions.
- Use at DC voltage (current)
- The +B signal should always be applied with a limiting resistance placed between the +B signal and the microcontroller.
- The value of the limiting resistance should be set so that when the +B signal is applied the input current to the microcontroller pins does not exceed rated values, either instantaneously or for prolonged periods.
- Note that when the microcontroller drive current is low, such as in the power saving modes, the +B input potential may pass through the protective diode and increase the potential at the V_{CC} pin, and this may affect other devices.

(MB90F591G, MB90591G : V_{CC} = 5.0 V±5 %, V_{SS} = AV_{SS} = 0.0 V, T_A = −40 °C to +85 °C)

Parameter	Symbol	Pin name	Condition	Value			Unit	Remarks
				Min	Typ	Max		
Input capacity	C_{IN}	Other than C, AV_{CC}, AV_{SS}, AVRH, AVRL, V_{CC}, V_{SS}, DV_{CC}, DV_{SS}, P70 to P87	—	—	5	15	pF	
		P70 to P87	—	—	15	30	pF	
Pull-up resistance	R_{UP}	$\overline{RST}$	—	25	50	100	kΩ	
Pull-down resistance	R_{DOWN}	MD2	—	25	50	100	kΩ	

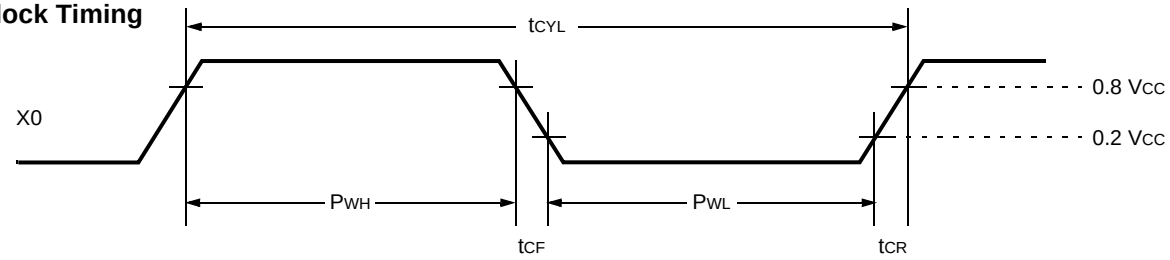
11.4 AC Characteristics

11.4.1 Clock Timing

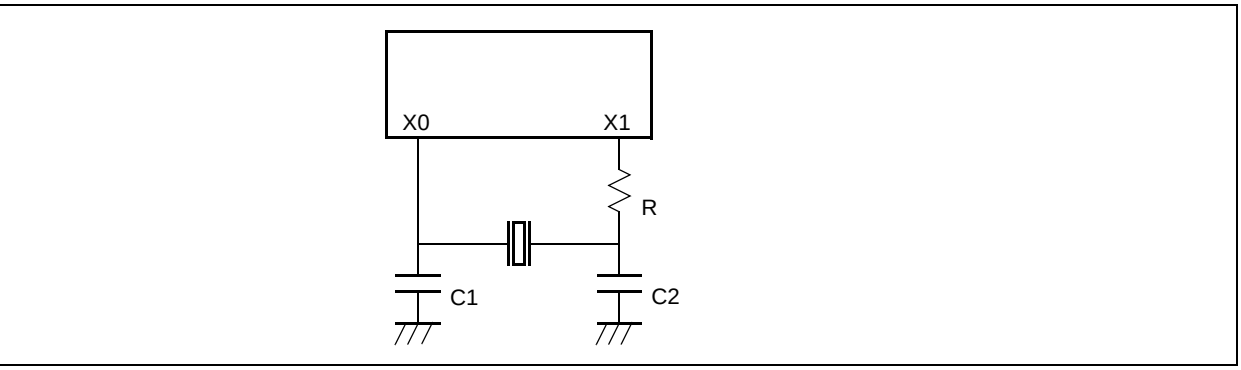
(MB90V590G, MB90F594G, MB90594G : V_{CC} = 5.0 V±10 %, V_{SS} = AV_{SS} = 0.0 V, T_A = −40 °C to +85 °C)
(MB90F591G, MB90591G : V_{CC} = 5.0 V±5 %, V_{SS} = AV_{SS} = 0.0 V, T_A = −40 °C to +85 °C)

Parameter	Symbol	Pin name	Value			Unit	Remarks
			Min	Typ	Max		
Oscillation frequency	f_C	X0, X1	3	—	16	MHz	
Oscillation cycle time	t_{CYL}	X0, X1	62.5	—	333	ns	
Input clock pulse width	P_{WH}, P_{WL}	X0	10	—	—	ns	Duty ratio is about 30 to 70%.
Input clock rise and fall time	t_{CR}, t_{CF}	X0	—	—	5	ns	When using external clock
Machine clock frequency	f_{CP}	—	1.5	—	16	MHz	
Machine clock cycle time	t_{CP}	—	62.5	—	666	ns	
Flash read cycle time	t_{CYCFL}	—	—	2 t_{CP}	—	ns	When Flash is accessed by CPU

• **Clock Timing**



Example of Oscillation circuit



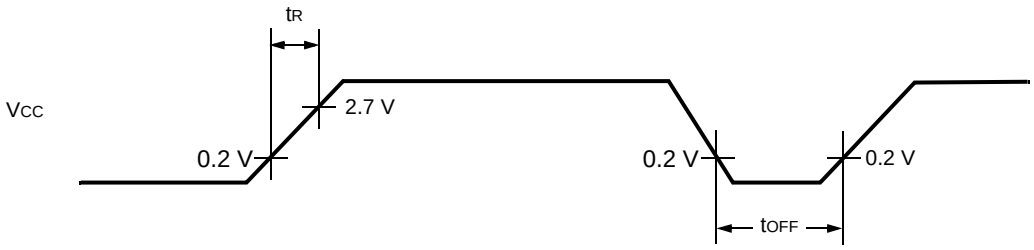
11.4.3 Power On Reset

(MB90V590G, MB90F594G, MB90594G : V_{CC} = 5.0 V±10 %, V_{SS} = AV_{SS} = 0.0 V, T_A = −40 °C to +85 °C)
(MB90F591G, MB90591G : V_{CC} = 5.0 V±5 %, V_{SS} = AV_{SS} = 0.0 V, T_A = −40 °C to +85 °C)

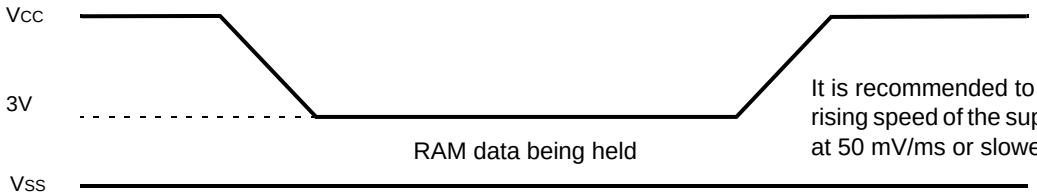
Parameter	Symbol	Pin name	Condition	Value		Unit	Remarks
				Min	Max		
Power on rise time	t_R	V_{CC}	—	0.05	30	ms	
Power off time	t_{OFF}	V_{CC}		50	—	ms	Due to repetitive operation

Notes:

- V_{CC} must be kept lower than 0.2 V before power-on.
- The above values are used for creating a power-on reset.
- Some registers in the device are initialized only upon a power-on reset. To initialize these register, turn on the power supply using the above values.

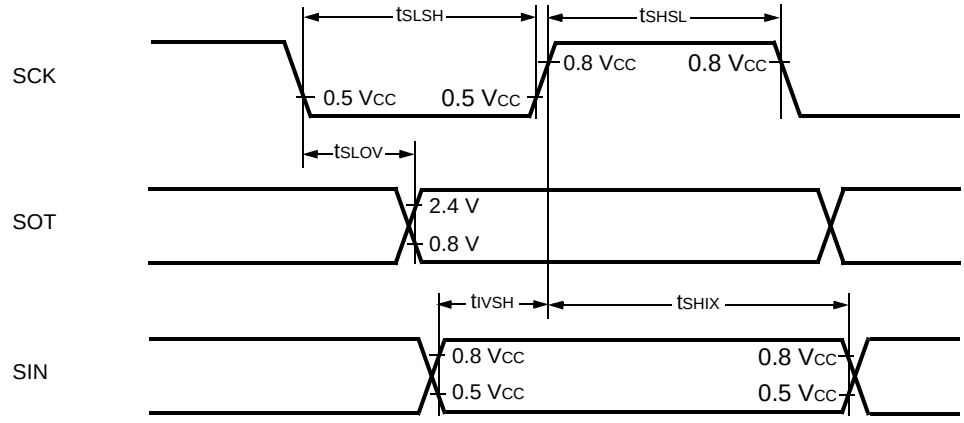


Sudden changes in the power supply voltage may cause a power-on reset.
To change the power supply voltage while the device is in operation, it is recommended to raise the voltage smoothly to suppress fluctuations as shown below.
In this case, change the supply voltage with the PLL clock not used. If the voltage drop is 1 V or fewer per second, however, you can use the PLL clock.



It is recommended to keep the rising speed of the supply voltage at 50 mV/ms or slower.

• **External Shift Clock Mode**

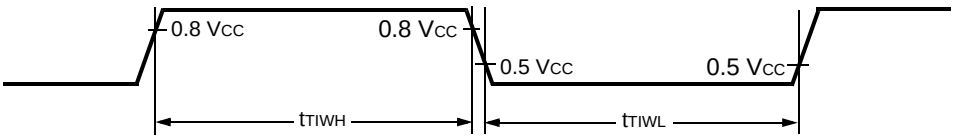


11.4.5 Timer Input Timing

(MB90V590G, MB90F594G, MB90594G : V_{CC} = 5.0 V±10 %, V_{SS} = AV_{SS} = 0.0 V, T_A = −40 °C to +85 °C)
(MB90F591G, MB90591G : V_{CC} = 5.0 V±5 %, V_{SS} = AV_{SS} = 0.0 V, T_A = −40 °C to +85 °C)

Parameter	Symbol	Pin name	Condition	Value		Unit	Remarks
				Min	Max		
Input pulse width	t_{TIWH}	TIN0	—	4 t_{CP}	—	ns	Under normal operation
	t_{TIWL}	IN0 to IN5		1	—	µs	In stop mode

• **Timer Input Timing**

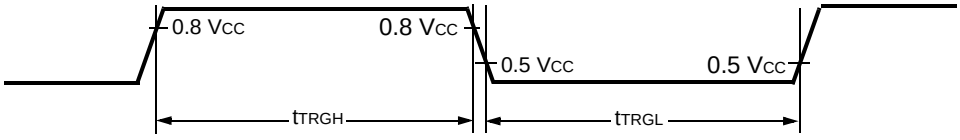


11.4.6 Trigger Input Timing

(MB90V590G, MB90F594G, MB90594G : V_{CC} = 5.0 V±10 %, V_{SS} = AV_{SS} = 0.0 V, T_A = −40 °C to +85 °C)
(MB90F591G, MB90591G : V_{CC} = 5.0 V±5 %, V_{SS} = AV_{SS} = 0.0 V, T_A = −40 °C to +85 °C)

Parameter	Symbol	Pin name	Condition	Value		Unit	Remarks
				Min	Max		
Input pulse width	t_{TRGH} t_{TRGL}	INT0 to INT7, ADTG	—	5 t_{CP}	—	ns	

- **Trigger Input Timing**



11.4.7 Slew Rate High Current Outputs (MB90F591G, MB90591G, MB90594G and MB90F594G only)

(MB90F594G, MB90594G : V_{CC} = 5.0 V±10 %, V_{SS} = AV_{SS} = 0.0 V, T_A = −40 °C to +85 °C)
(MB90F591G, MB90591G : V_{CC} = 5.0 V±5 %, V_{SS} = AV_{SS} = 0.0 V, T_A = −40 °C to +85 °C)

Parameter	Symbol	Pin name	Condition	Value		Unit	Remarks
				Min	Max		
Output Rise/Fall time	t_{R2} t_{F2}	Port P70 to P77, Port P80 to P87	—	15	40	ns	

- Slew Rate Output Timing

$V_H = V_{OL2} + 0.1 \times (V_{OH2} - V_{OL2})$
$V_L = V_{OL2} + 0.9 \times (V_{OH2} - V_{OL2})$

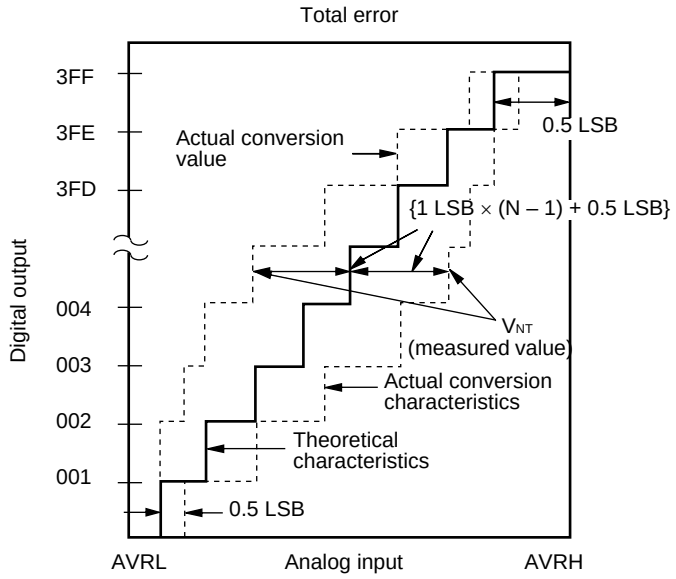
11.6 A/D Converter Glossary

Resolution : Analog changes that are identifiable with the A/D converter

Linearity error : The deviation of the straight line connecting the zero transition point (“00 0000 0000” ↔ “00 0000 0001”) with the full-scale transition point (“11 1111 1110” ↔ “11 1111 1111”) from actual conversion characteristics

Differential linearity error : The deviation of input voltage needed to change the output code by 1 LSB from the theoretical value

Total error : The total error is defined as a difference between the actual value and the theoretical value, which includes zero-transition error/full-scale transition error and linearity error.



1 LSB = (Theoretical value) $\frac{AVRH - AVRL}{1024}$ [V]

Total error for digital output N = $\frac{V_{NT} - \{1\ LSB \times (N - 1) + 0.5\ LSB\}}{1\ LSB}$ [LSB]

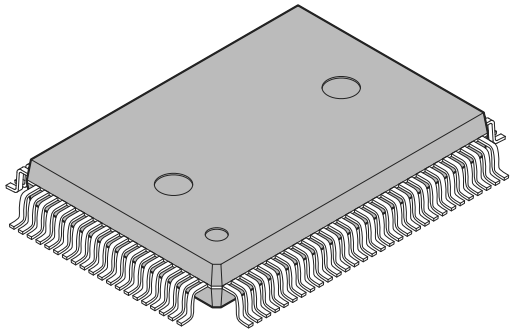
V_{OT} (Theoretical value) = AVRL + 0.5 LSB[V]

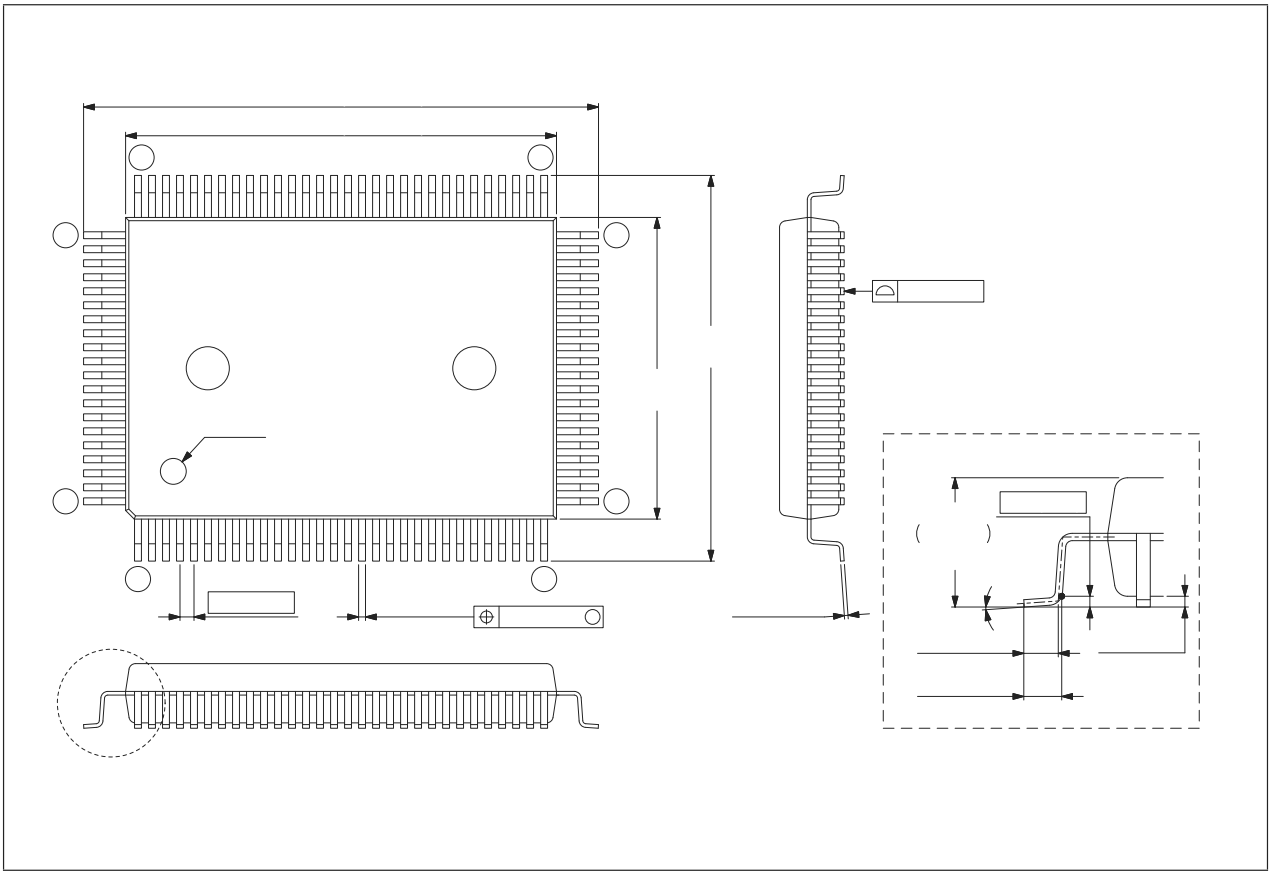
V_{NT} : Voltage at a transition of digital output from (N – 1) to N

V_{FST} (Theoretical value) = AVRH – 1.5 LSB[V]

(Continued)

14. Package Dimension





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