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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	F²MC-16LX
Core Size	16-Bit
Speed	16MHz
Connectivity	CANbus, EBI/EMI, SCI, Serial I/O, UART/USART
Peripherals	POR, PWM, WDT
Number of I/O	78
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	6K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 8x8/10b
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-BQFP
Supplier Device Package	100-QFP (14x20)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/mb90f594gpf-ge1

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Features	MB90591G/594G	MB90F591G/F594G	MB90V590G
CAN Interface	Number of channels : 2 Conforms to CAN Specification Version 2.0 Part A and B Automatic re-transmission in case of error Automatic transmission responding to Remote Frame Prioritized 16 message buffers for data and ID's Supports multiple messages Flexible configuration of acceptance filtering : Full bit compare / Full bit mask / Two partial bit masks Supports up to 1Mbps CAN bit timing setting : MB90(F)59xG : TSEG2 ≥ RSJW		
Stepping motor controller (4 channels)	Four high current outputs for each channel Synchronized two 8-bit PWM's for each channel		
External interrupt circuit	Number of inputs : 8 Started by a rising edge, a falling edge, an "H" level input, or an "L" level input.		
Sound generator	8-bit PWM signal is mixed with tone frequency from 8-bit reload counter PWM frequency : 62.5K, 31.2K, 15.6K, 7.8KHz (at System clock = 16MHz) Tone frequency : PWM frequency / 2 / (reload value + 1)		
Extended I/O serial interface	Clock synchronized transmission (31.25K/62.5K/125K/500K/1Mbps at machine clock frequency of 16 MHz) LSB first/MSB first		
Watch timer	Directly operates with the system clock Read/Write accessible Second/Minute/Hour registers		
Watchdog timer	Reset generation interval : 3.58 ms, 14.33 ms, 57.23 ms, 458.75 ms (at oscillation of 4 MHz, minimum value)		
Flash Memory	Supports automatic programming, Embedded Algorithm and Write/Erase/Erase-Suspend/Resume commands A flag indicating completion of the algorithm Hard-wired reset vector available in order to point to a fixed boot sector in Flash Memory Boot block configuration Erase can be performed on each block Block protection with external programming voltage Flash Writer from Minato Electronics Inc.		
Low-power consumption (stand-by) mode	Sleep/stop/CPU intermittent operation/watch timer/hardware stand-by		
Process	CMOS		
Power supply voltage for operation*2	5 V±10 % (MB90V590G, MB90F594G, MB90594G) 5 V±5 % (MB90F591G, MB90591G)		
Package	QFP-100		PGA-256

*1 : It is setting of DIP switch S2 when Emulation pod (MB2145-507) is used.
Please refer to the MB2145-507 hardware manual (2.7 Emulator-specific Power Pin) about details.

*2 : Varies with conditions such as the operating frequency. (See section "Electrical Characteristics.")

3. Pin Description

No.	Pin name	Circuit type	Function
82	X0	A	Oscillator pin
83	X1		
77	$\overline{RST}$	B	Reset input
52	$\overline{HST}$	C	Hardware standby input
85 to 90	P00 to P05	D	General purpose I/O
	IN0 to IN5		Inputs for the Input Captures
91 to 96	P06, P07, P10 to P13	D	General purpose I/O
	OUT0 to OUT5		Outputs for the Output Compares. To enable the signal outputs, the corresponding bits of the Port Direction registers should be set to “1”.
97	P14	D	General purpose I/O
	RX1		RX input for CAN Interface 1
98	P15	D	General purpose I/O
	TX1		TX output for CAN Interface 1. To enable the signal output, the corresponding bit of the Port Direction register should be set to “1”.
99	P16	D	General purpose I/O
	SGO		SGO output for the Sound Generator. To enable the signal output, the corresponding bit of the Port Direction register should be set to “1”.
100	P17	D	General purpose I/O
	SGA		SGA output for the Sound Generator. To enable the signal output, the corresponding bit of the Port Direction register should be set to “1”.
1 to 4	P20 to P23	D	General purpose I/O
5 to 8	P24 to P27	D	General purpose I/O
	INT4 to INT7		External interrupt input for INT4 to INT7
9, 10	P30, P31	D	General purpose I/O
12, 13	P32, P33	D	General purpose I/O
14	P34	D	General purpose I/O
	SOT0		SOT output for UART 0. To enable the signal output, the corresponding bit of the Port Direction register should be set to “1”.
15	P35	D	General purpose I/O
	SCK0		SCK input/output for UART 0. To enable the signal output, the corresponding bit of the Port Direction register should be set to “1”.

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No.	Pin name	Circuit type	Function
54 to 57	P70 to P73	F	General purpose I/O
	PWM1P0, PWM1M0, PWM2P0, PWM2M0		Output for Stepping Motor Controller channel 0.
59 to 62	P74 to P77	F	General purpose I/O
	PWM1P1, PWM1M1, PWM2P1, PWM2M1		Output for Stepping Motor Controller channel 1.
64 to 67	P80 to P83	F	General purpose I/O
	PWM1P2, PWM1M2, PWM2P2, PWM2M2		Output for Stepping Motor Controller channel 2.
69 to 72	P84 to P87	F	General purpose I/O
	PWM1P3, PWM1M3, PWM2P3, PWM2M3		Output for Stepping Motor Controller channel 3.
74	P90	D	General purpose I/O
	TX0		TX output for CAN Interface 0
75	P91	D	General purpose I/O
	RX0		RX input for CAN Interface 0
76	P92	D	General purpose I/O
	INT0		External interrupt input for INT0
78	P93	D	General purpose I/O
	INT1		External interrupt input for INT1
79	P94	D	General purpose I/O
	INT2		External interrupt input for INT2
80	P95	D	General purpose I/O
	INT3		External interrupt input for INT3
58, 68	DV_{CC}	—	Dedicated power supply pins for the high current output buffers (Pin No. 54 to 72)
53, 63, 73	DV_{SS}	—	Dedicated ground pins for the high current output buffers (Pin No. 54 to 72)
34	AV_{CC}	Power supply	Power supply for analog circuit pin When turning this power supply on or off, always be sure to first apply electric potential equal to or greater than AV_{CC} to V_{CC}.
37	AV_{SS}	Power supply	Ground level for analog circuit

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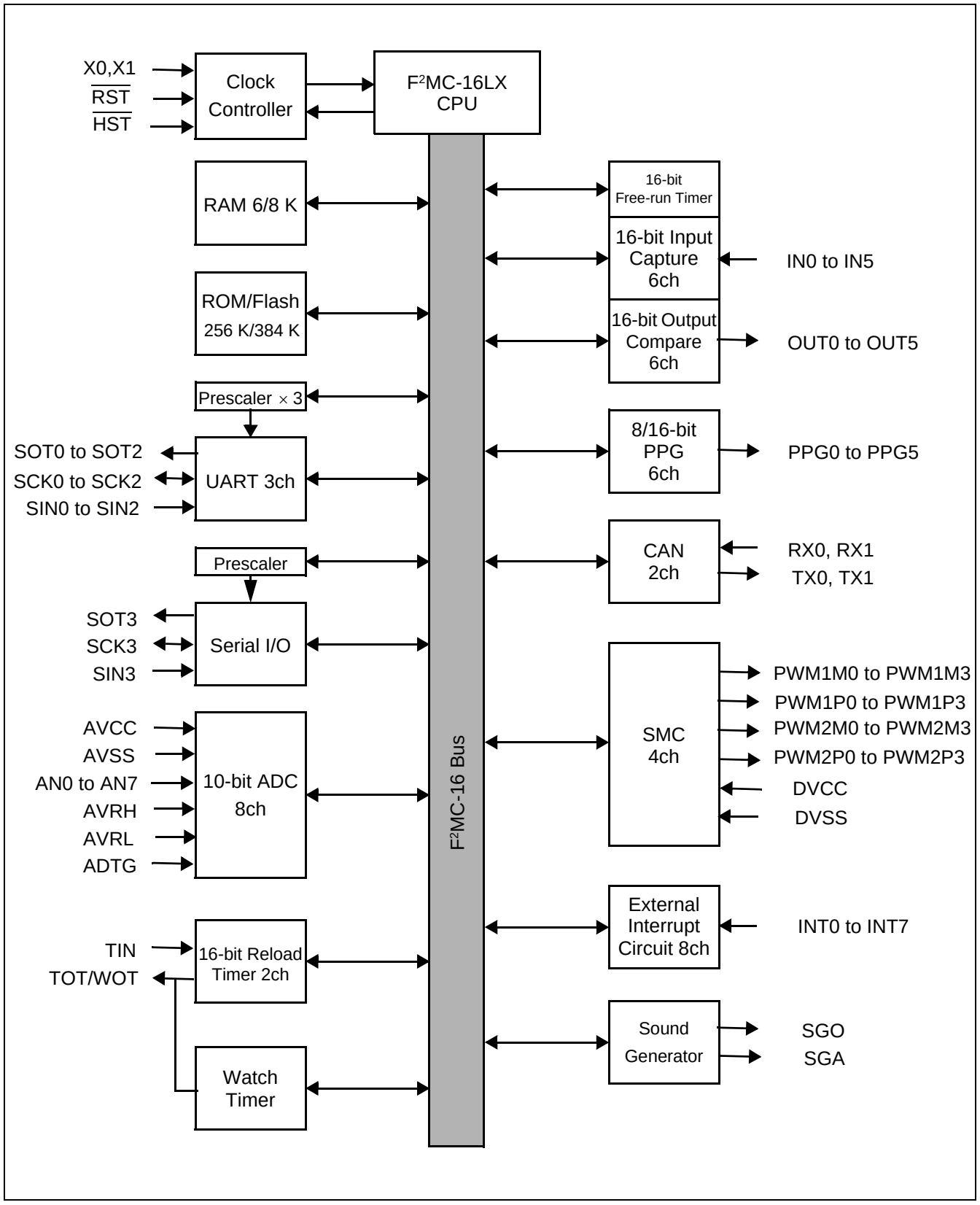
No.	Pin name	Circuit type	Function
35	AVRH	Power supply	Reference voltage input pin for analog circuit When turning this power supply on or off, always be sure to first apply electric potential equal to or greater than AVRH to AV_{CC}.
36	AVRL	Power supply	Reference voltage input pin for analog circuit
49, 50	MD0, MD1	C	Operating mode selection input pins Connect directly to V_{CC} or V_{SS}.
51	MD2	G	Operating mode selection input pin Connect directly to V_{CC} or V_{SS}.
27	C	—	This is the power supply stabilization capacitor pin. It should be connected externally to an 0.1 µF ceramic capacitor.
23, 84	V_{CC}	Power supply	Power supply (5.0 V) input pin for digital circuit
11,42,81	V_{SS}	Power supply	Power supply (GND) input pin for digital circuit

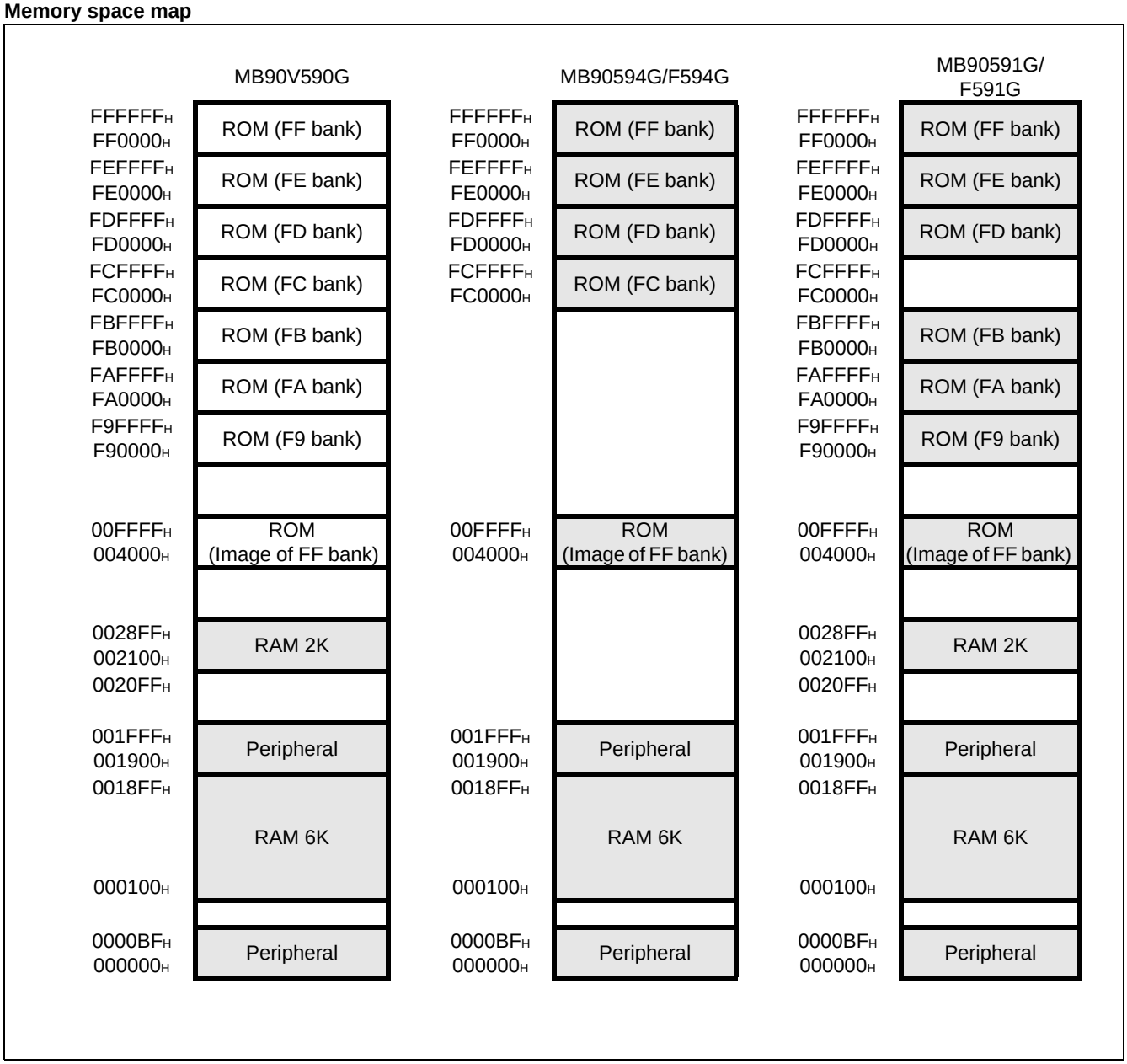
6. Block Diagram



7. Memory Space

The memory space of the MB90590/590G Series is shown below

Memory space map



Note: : The ROM data of bank FF is reflected in the upper address of bank 00, realizing effective use of the C compiler small model. The lower 16-bit of bank FF and the lower 16-bit of bank 00 are assigned to the same address, enabling reference of the table on the ROM without stating “far”.
For example, if an attempt has been made to access $00C000_H$, the contents of the ROM at $FFC000_H$ are accessed. Since the ROM area of the FF bank exceeds 48 Kbytes, the whole area cannot be reflected in the image for the 00 bank. The ROM data at $FF4000_H$ to $FFFFFF_H$ looks, therefore, as if it were the image for 004000_H to $00FFFF_H$. Thus, it is recommended that the ROM data table be stored in the area of $FF4000_H$ to $FFFFFF_H$.

Address	Register	Abbreviation	Access	Peripheral	Initial value
28H	Serial Mode Control Register 2	UMC2	R/W	UART2	0 0 0 0 0 1 0 0B
29H	Serial Status Register 2	USR2	R/W		0 0 0 1 0 0 0 0B
2AH	Serial Input/Output Data Register 2	UIDR2/UODR2	R/W		XXXXXXXXB
2BH	Rate and Data Register 2	URD2	R/W		0 0 0 0 0 0 0XB
2CH	Serial Mode Control Register (low-order)	SMCS	R/W	Serial I/O	_ _ _ _0 0 0 0B
2DH	Serial Mode Control Register (high-order)	SMCS	R/W		0 0 0 0 0 0 1 0B
2EH	Serial Data Register	SDR	R/W		XXXXXXXXB
2FH	Edge Selector Register	SES	R/W		_ _ _ _ _ _ _0B
30H	External Interrupt Enable Register	ENIR	R/W	External Interrupt	0 0 0 0 0 0 0 0B
31H	External Interrupt Request Register	EIRR	R/W		XXXXXXXXB
32H	External Interrupt Level Register	ELVR	R/W		0 0 0 0 0 0 0 0B
33H	External Interrupt Level Register	ELVR	R/W		0 0 0 0 0 0 0 0B
34H	A/D Control Status Register 0	ADCS0	R/W	A/D Converter	0 0 0 0 0 0 0 0B
35H	A/D Control Status Register 1	ADCS1	R/W		0 0 0 0 0 0 0 0B
36H	A/D Data Register 0	ADCR0	R		XXXXXXXXB
37H	A/D Data Register 1	ADCR1	R/W		0 0 0 0 1 0 XXB
38H	PPG0 Operation Mode Control Register	PPGC0	R/W	16-bit Programmable Pulse Generator 0/1	0 _ 0 0 0 _ _ 1B
39H	PPG1 Operation Mode Control Register	PPGC1	R/W		0 _ 0 0 0 0 0 1B
3AH	PPG0,1 Output Pin Control Register	PPG01	R/W		0 0 0 0 0 0 0 0B
3BH	Reserved				
3CH	PPG2 Operation Mode Control Register	PPGC2	R/W	16-bit Programmable Pulse Generator 2/3	0 _ 0 0 0 _ _1B
3DH	PPG3 Operation Mode Control Register	PPGC3	R/W		0 _ 0 0 0 0 0 1B
3EH	PPG2,3 Output Pin Control Register	PPG23	R/W		0 0 0 0 0 0 0 0B
3FH	Reserved				
40H	PPG4 Operation Mode Control Register	PPGC4	R/W	16-bit Programmable Pulse Generator 4/5	0 _ 0 0 0 _ _ 1B
41H	PPG5 Operation Mode Control Register	PPGC5	R/W		0 _ 0 0 0 0 0 1B
42H	PPG4,5 Output Pin Control Register	PPG45	R/W		0 0 0 0 0 0 0 0B
43H	Reserved				
44H	PPG6 Operation Mode Control Register	PPGC6	R/W	16-bit Programmable Pulse Generator 6/7	0 _ 0 0 0 _ _ 1B
45H	PPG7 Operation Mode Control Register	PPGC7	R/W		0 _ 0 0 0 0 0 1B
46H	PPG6,7 Output Pin Control Register	PPG67	R/W		0 0 0 0 0 0 0 0B
47H	Reserved				

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Address	Register	Abbreviation	Access	Peripheral	Initial value
48H	PPG8 Operation Mode Control Register	PPGC8	R/W	16-bit Programmable Pulse Generator 8/9	0 _ 0 0 0 _ _ 1B
49H	PPG9 Operation Mode Control Register	PPGC9	R/W		0 _ 0 0 0 0 0 1B
4AH	PPG8,9 Output Pin Control Register	PPG89	R/W		0 0 0 0 0 0 0 0B
4BH	Reserved				
4CH	PPGA Operation Mode Control Register	PPGCA	R/W	16-bit Programmable Pulse Generator A/B	0 _ 0 0 0 _ _ 1B
4DH	PPGB Operation Mode Control Register	PPGCB	R/W		0 _ 0 0 0 0 0 1B
4EH	PPGA,B Output Pin Control Register	PPGAB	R/W		0 0 0 0 0 0 0 0B
4FH	Reserved				
50H	Timer Control Status Register 0 (low-order)	TMCSR0	R/W	16-bit Reload Timer 0	0 0 0 0 0 0 0 0B
51H	Timer Control Status Register 0 (high-order)	TMCSR0	R/W		_ _ _ _ 0 0 0 0B
52H	Timer Control Status Register 1 (low-order)	TMCSR1	R/W	16-bit Reload Timer 1	0 0 0 0 0 0 0 0B
53H	Timer Control Status Register 1 (high-order)	TMCSR1	R/W		_ _ _ _ 0 0 0 0B
54H	Input Capture Control Status Register 0/1	ICS01	R/W	Input Capture 0/1	0 0 0 0 0 0 0 0B
55H	Input Capture Control Status Register 2/3	ICS23	R/W	Input Capture 2/3	0 0 0 0 0 0 0 0B
56H	Input Capture Control Status Register 4/5	ICS45	R/W	Input Capture 4/5	0 0 0 0 0 0 0 0B
57H	Reserved				
58H	Output Compare Control Status Register 0	OCS0	R/W	Output Compare 0/1	0 0 0 0 _ _ 0 0B
59H	Output Compare Control Status Register 1	OCS1	R/W		_ _ _ 0 0 0 0 0B
5AH	Output Compare Control Status Register 2	OCS2	R/W	Output Compare 2/3	0 0 0 0 _ _ 0 0B
5BH	Output Compare Control Status Register 3	OCS3	R/W		_ _ _ 0 0 0 0 0B
5CH	Output Compare Control Status Register 4	OCS4	R/W	Output Compare 4/5	0 0 0 0 _ _ 0 0B
5DH	Output Compare Control Status Register 5	OCS5	R/W		_ _ _ 0 0 0 0 0B
5EH	Sound Control Register (low-order)	SGCR	R/W	Sound Generator	0 0 0 0 0 0 0 0B
5FH	Sound Control Register (high-order)	SGCR	R/W		0 _ _ _ _ _ _ 0B

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Address	Register	Abbreviation	Access	Peripheral	Initial value
$B0_H$	Interrupt Control Register 00	ICR00	R/W	Interrupt controller	0 0 0 0 0 1 1 1$_B$
$B1_H$	Interrupt Control Register 01	ICR01	R/W		0 0 0 0 0 1 1 1$_B$
$B2_H$	Interrupt Control Register 02	ICR02	R/W		0 0 0 0 0 1 1 1$_B$
$B3_H$	Interrupt Control Register 03	ICR03	R/W		0 0 0 0 0 1 1 1$_B$
$B4_H$	Interrupt Control Register 04	ICR04	R/W		0 0 0 0 0 1 1 1$_B$
$B5_H$	Interrupt Control Register 05	ICR05	R/W		0 0 0 0 0 1 1 1$_B$
$B6_H$	Interrupt Control Register 06	ICR06	R/W		0 0 0 0 0 1 1 1$_B$
$B7_H$	Interrupt Control Register 07	ICR07	R/W		0 0 0 0 0 1 1 1$_B$
$B8_H$	Interrupt Control Register 08	ICR08	R/W		0 0 0 0 0 1 1 1$_B$
$B9_H$	Interrupt Control Register 09	ICR09	R/W		0 0 0 0 0 1 1 1$_B$
BA_H	Interrupt Control Register 10	ICR10	R/W		0 0 0 0 0 1 1 1$_B$
BB_H	Interrupt Control Register 11	ICR11	R/W		0 0 0 0 0 1 1 1$_B$
BC_H	Interrupt Control Register 12	ICR12	R/W		0 0 0 0 0 1 1 1$_B$
BD_H	Interrupt Control Register 13	ICR13	R/W		0 0 0 0 0 1 1 1$_B$
BE_H	Interrupt Control Register 14	ICR14	R/W		0 0 0 0 0 1 1 1$_B$
BF_H	Interrupt Control Register 15	ICR15	R/W		0 0 0 0 0 1 1 1$_B$
$C0_H$ to FF_H	Reserved				
1900_H	Reload L Register	PRLL0	R/W	16-bit Programmable Pulse Generator 0/1	XXXXXXXX$_B$
1901_H	Reload H Register	PRLH0	R/W		XXXXXXXX$_B$
1902_H	Reload L Register	PRLL1	R/W		XXXXXXXX$_B$
1903_H	Reload H Register	PRLH1	R/W		XXXXXXXX$_B$
1904_H	Reload L Register	PRLL2	R/W	16-bit Programmable Pulse Generator 2/3	XXXXXXXX$_B$
1905_H	Reload H Register	PRLH2	R/W		XXXXXXXX$_B$
1906_H	Reload L Register	PRLL3	R/W		XXXXXXXX$_B$
1907_H	Reload H Register	PRLH3	R/W		XXXXXXXX$_B$
1908_H	Reload L Register	PRLL4	R/W	16-bit Programmable Pulse Generator 4/5	XXXXXXXX$_B$
1909_H	Reload H Register	PRLH4	R/W		XXXXXXXX$_B$
$190A_H$	Reload L Register	PRLL5	R/W		XXXXXXXX$_B$
$190B_H$	Reload H Register	PRLH5	R/W		XXXXXXXX$_B$
$190C_H$	Reload L Register	PRLL6	R/W	16-bit Programmable Pulse Generator 6/7	XXXXXXXX$_B$
$190D_H$	Reload H Register	PRLH6	R/W		XXXXXXXX$_B$
$190E_H$	Reload L Register	PRLL7	R/W		XXXXXXXX$_B$
$190F_H$	Reload H Register	PRLH7	R/W		XXXXXXXX$_B$

(Continued)

Address	Register	Abbreviation	Access	Peripheral	Initial value
1930H	Output Compare Register 0 (low-order)	OCCP0	R/W	Output Compare 0/1	XXXXXXXXB
1931H	Output Compare Register 0 (high-order)	OCCP0	R/W		XXXXXXXXB
1932H	Output Compare Register 1 (low-order)	OCCP1	R/W		XXXXXXXXB
1933H	Output Compare Register 1 (high-order)	OCCP1	R/W		XXXXXXXXB
1934H	Output Compare Register 2 (low-order)	OCCP2	R/W	Output Compare 2/3	XXXXXXXXB
1935H	Output Compare Register 2 (high-order)	OCCP2	R/W		XXXXXXXXB
1936H	Output Compare Register 3 (low-order)	OCCP3	R/W		XXXXXXXXB
1937H	Output Compare Register 3 (high-order)	OCCP3	R/W		XXXXXXXXB
1938H	Output Compare Register 4 (low-order)	OCCP4	R/W	Output Compare 4/5	XXXXXXXXB
1939H	Output Compare Register 4 (high-order)	OCCP4	R/W		XXXXXXXXB
193AH	Output Compare Register 5 (low-order)	OCCP5	R/W		XXXXXXXXB
193BH	Output Compare Register 5 (high-order)	OCCP5	R/W		XXXXXXXXB
193CH to 193FH	Reserved				
1940H	Timer 0/Reload Register 0 (low-order)	TMR0/TMRLR0	R/W	16-bit Reload Timer 0	XXXXXXXXB
1941H	Timer 0/Reload Register 0 (high-order)	TMR0/TMRLR0	R/W		XXXXXXXXB
1942H	Timer 1/Reload Register 1 (low-order)	TMR1/TMRLR1	R/W	16-bit Reload Timer 1	XXXXXXXXB
1943H	Timer 1/Reload Register 1 (high-order)	TMR1/TMRLR1	R/W		XXXXXXXXB
1944H	Timer Data Register (low-order)	TCDT	R/W	16-bit Free-run Timer	00000000B
1945H	Timer Data Register (high-order)	TCDT	R/W		00000000B
1946H	Frequency Data Register	SGFR	R/W	Sound Generator	XXXXXXXXB
1947H	Amplitude Data Register	SGAR	R/W		XXXXXXXXB
1948H	Decrement Grade Register	SGDR	R/W		XXXXXXXXB
1949H	Tone Count Register	SGTR	R/W		XXXXXXXXB

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Address	Register	Abbreviation	Access	Peripheral	Initial value
1FF0H	Program Address Detection Register 0 (low-order)	PADR0	R/W	Address Match Detection Function	XXXXXXXX B
1FF1H	Program Address Detection Register 0 (middle-order)	PADR0	R/W		XXXXXXXX B
1FF2H	Program Address Detection Register 0 (high-order)	PADR0	R/W		XXXXXXXX B
1FF3H	Program Address Detection Register 1 (low-order)	PADR1	R/W		XXXXXXXX B
1FF4H	Program Address Detection Register 1 (middle-order)	PADR1	R/W		XXXXXXXX B
1FF5H	Program Address Detection Register 1 (high-order)	PADR1	R/W		XXXXXXXX B
1FF6H to 1FFFH	Reserved				

Note: : Initial value of "_" represents unused bit; "X" represents unknown value.
Addresses in the rage 0000H to 00FFH, which are not listed in the table, are reserved for the primary functions of the MCU. A read access to these reserved addresses results in reading "X", and any write access should not be performed.

(Continued)

List of Control Registers

Address		Register	Abbreviation	Access	Initial Value
CAN0	CAN1				
001C00H	001D00H	Control status register	CSR	R/W, R	00---000 0----0-1B
001C01H	001D01H				
001C02H	001D02H	Last event indicator register	LEIR	R/W	-------- 000-0000B
001C03H	001D03H				
001C04H	001D04H	Receive/transmit error counter	RTEC	R	00000000 00000000B
001C05H	001D05H				
001C06H	001D06H	Bit timing register	BTR	R/W	-1111111 11111111B
001C07H	001D07H				
001C08H	001D08H	IDE register	IDER	R/W	XXXXXXXX XXXXXXXXB
001C09H	001D09H				
001C0AH	001D0AH	Transmit RTR register	TRTRR	R/W	00000000 00000000B
001C0BH	001D0BH				
001C0CH	001D0CH	Remote frame receive waiting register	RFWTR	R/W	XXXXXXXX XXXXXXXXB
001C0DH	001D0DH				
001C0EH	001D0EH	Transmit interrupt enable register	TIER	R/W	00000000 00000000B
001C0FH	001D0FH				
001C10H	001D10H	Acceptance mask select register	AMSR	R/W	XXXXXXXX XXXXXXXXB
001C11H	001D11H				
001C12H	001D12H				XXXXXXXX XXXXXXXXB
001C13H	001D13H				
001C14H	001D14H	Acceptance mask register 0	AMR0	R/W	XXXXXXXX XXXXXXXXB
001C15H	001D15H				
001C16H	001D16H				XXXXX--- XXXXXXXXB
001C17H	001D17H				
001C18H	001D18H	Acceptance mask register 1	AMR1	R/W	XXXXXXXX XXXXXXXXB
001C19H	001D19H				
001C1AH	001D1AH				XXXXX--- XXXXXXXXB
001C1BH	001D1BH				

(Continued)

Address		Register	Abbreviation	Access	Initial Value
CAN0	CAN1				
001A88H to 001A8FH	001B88H to 001B8FH	Data register 1 (8 bytes)	DTR1	R/W	XXXXXXXXB to XXXXXXXXB
001A90H to 001A97H	001B90H to 001B97H	Data register 2 (8 bytes)	DTR2	R/W	XXXXXXXXB to XXXXXXXXB
001A98H to 001A9FH	001B98H to 001B9FH	Data register 3 (8 bytes)	DTR3	R/W	XXXXXXXXB to XXXXXXXXB
001AA0H to 001AA7H	001BA0H to 001BA7H	Data register 4 (8 bytes)	DTR4	R/W	XXXXXXXXB to XXXXXXXXB
001AA8H to 001AAFH	001BA8H to 001BAFH	Data register 5 (8 bytes)	DTR5	R/W	XXXXXXXXB to XXXXXXXXB
001AB0H to 001AB7H	001BB0H to 001BB7H	Data register 6 (8 bytes)	DTR6	R/W	XXXXXXXXB to XXXXXXXXB
001AB8H to 001ABFH	001BB8H to 001BBFH	Data register 7 (8 bytes)	DTR7	R/W	XXXXXXXXB to XXXXXXXXB
001AC0H to 001AC7H	001BC0H to 001BC7H	Data register 8 (8 bytes)	DTR8	R/W	XXXXXXXXB to XXXXXXXXB
001AC8H to 001ACFH	001BC8H to 001BCFH	Data register 9 (8 bytes)	DTR9	R/W	XXXXXXXXB to XXXXXXXXB
001AD0H to 001AD7H	001BD0H to 001BD7H	Data register 10 (8 bytes)	DTR10	R/W	XXXXXXXXB to XXXXXXXXB
001AD8H to 001ADFH	001BD8H to 001BDFH	Data register 11 (8 bytes)	DTR11	R/W	XXXXXXXXB to XXXXXXXXB
001AE0H to 001AE7H	001BE0H to 001BE7H	Data register 12 (8 bytes)	DTR12	R/W	XXXXXXXXB to XXXXXXXXB
001AE8H to 001AEFH	001BE8H to 001BEFH	Data register 13 (8 bytes)	DTR13	R/W	XXXXXXXXB to XXXXXXXXB
001AF0H to 001AF7H	001BF0H to 001BF7H	Data register 14 (8 bytes)	DTR14	R/W	XXXXXXXXB to XXXXXXXXB
001AF8H to 001AFFH	001BF8H to 001BFFH	Data register 15 (8 bytes)	DTR15	R/W	XXXXXXXXB to XXXXXXXXB

Notes:

- For a peripheral module with two interrupt for a single interrupt number, both interrupt request flags are cleared by the EI²OS interrupt clear signal.
- At the end of EI²OS, the EI²OS clear signal will be asserted for all the interrupt flags assigned to the same interrupt number. If one interrupt flag starts the EI²OS and in the meantime another interrupt flag is set by a hardware event, the later event is lost because the flag is cleared by the EI²OS clear signal caused by the first event. So it is recommended not to use the EI²OS for this interrupt number.
- If EI²OS is enabled, EI²OS is initiated when one of the two interrupt signals in the same interrupt control register (ICR) is asserted. This means that different interrupt sources share the same EI²OS Descriptor which should be unique for each interrupt source. For this reason, when one interrupt source uses the EI²OS, the other interrupt should be disabled.

11. Electrical Characteristics

11.1 Absolute Maximum Ratings

(V_{SS} = AV_{SS} = 0.0 V)

Parameter	Symbol	Rating		Unit	Remarks
		Min	Max		
Power supply voltage	V_{CC}	V_{SS} − 0.3	V_{SS} + 6.0	V	
	AV_{CC}	V_{SS} − 0.3	V_{SS} + 6.0	V	V_{CC} = AV_{CC} *1
	AVRH, AVRL	V_{SS} − 0.3	V_{SS} + 6.0	V	AV_{CC} ≥ AVRH/L, AVRH ≥ AVRL *1
	DV_{CC}	V_{SS} − 0.3	V_{SS} + 6.0	V	V_{CC} ≥ DV_{CC}
Input voltage	V_I	V_{SS} − 0.3	V_{SS} + 6.0	V	*2
Output voltage	V_O	V_{SS} − 0.3	V_{SS} + 6.0	V	*2
Max clamp current	I_{CLAMP}	−2.0	+ 2.0	mA	*6
Total Max clamp current	$\sum \lvert I_{CLAMP} \rvert$	—	20	mA	*6
“L” level Max output current	I_{OL1}	—	15	mA	Normal output *3
“L” level avg. output current	I_{OLAV1}	—	4	mA	Normal output, average value *4
“L” level Max output current	I_{OL2}	—	40	mA	High current output *3
“L” level avg. output current	I_{OLAV2}	—	30	mA	High current output, average value *4
“L” level Max overall output current	$\sum I_{OL1}$	—	100	mA	Total normal output
“L” level Max overall output current	$\sum I_{OL2}$		330	mA	Total high current output
“L” level avg. overall output current	$\sum I_{OLAV1}$	—	50	mA	Total normal output, average value *5
“L” level avg. overall output current	$\sum I_{OLAV2}$		250	mA	Total high current output, average value *5
“H” level Max output current	I_{OH1}	—	–15	mA	Normal output *3
“H” level avg. output current	I_{OHAV1}	—	–4	mA	Normal output, average value *4
“H” level Max output current	I_{OH2}	—	–40	mA	High current output *3
“H” level avg. output current	I_{OHAV2}	—	–30	mA	High current output, average value *4
“H” level Max overall output current	$\sum I_{OH1}$	—	–100	mA	Total normal output
“H” level Max overall output current	$\sum I_{OH2}$	—	–330	mA	Total high current output
“H” level avg. overall output current	$\sum I_{OHAV1}$	—	–50	mA	Total normal output, average value *5
“H” level avg. overall output current	$\sum I_{OHAV2}$	—	–250	mA	Total high current output, average value *5
Power consumption	P_D	—	500	mW	MB90F594G, MB90F591G
		—	400	mW	MB90594G, MB90591G
Operating temperature	T_A	–40	+85	°C	
Storage temperature	T_{STG}	–55	+150	°C	

*1 : AV_{CC}, AVRH, AVRL and DV_{CC} shall not exceed V_{CC}. AVRH and AVRL shall not exceed AV_{CC}.
Also, AVRL shall not exceed AVRH.

*2 : V_I and V_O should not exceed V_{CC} + 0.3V. V_I should not exceed the specified ratings. However if the maximum current to/from an input is limited by some means with external components, the I_{CLAMP} rating supersedes the V_I rating.

*3 : The maximum output current is a peak value for a corresponding pin.

*4 : Average output current is an average current value observed for a 100 ms period for a corresponding pin.

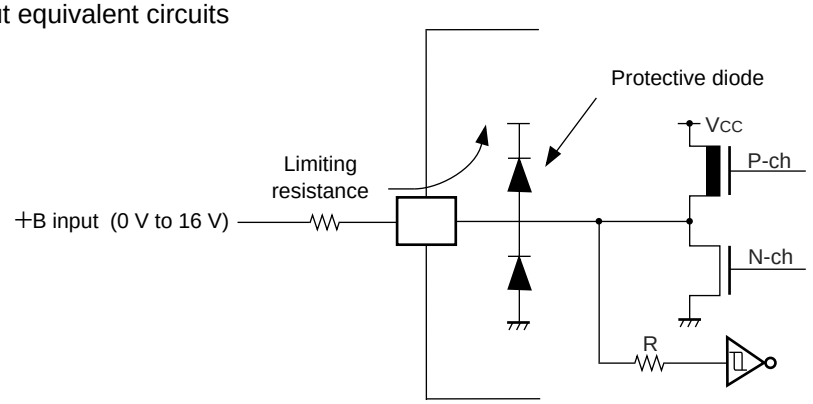
*5 : Total average current is an average current value observed for a 100 ms period for all corresponding pins.

*6 :

- Applicable to pins : P00 to P07, P10 to P17, P20 to P27, P30 to P37, P40 to P47, P50 to P57, P60 to P67, P70 to P77, P80 to P87, P90 toP95
- Use within recommended operating conditions.
- Use at DC voltage (current)
- The +B signal should always be applied with a limiting resistance placed between the +B signal and the microcontroller.
- The value of the limiting resistance should be set so that when the +B signal is applied the input current to the microcontroller pins does not exceed rated values, either instantaneously or for prolonged periods.
- Note that when the microcontroller drive current is low, such as in the power saving modes, the +B input potential may pass through the protective diode and increase the potential at the V_{CC} pin, and this may affect other devices.

- Note that if a +B signal is input when the microcontroller power supply is off (not fixed at 0 V) , the power supply is provided from the pins, so that incomplete operation may result.
- Note that if the +B input is applied during power-on, the power supply is provided from the pins and the resulting supply voltage may not be sufficient to operate the power-on reset.
- Care must be taken not to leave the +B input pin open.
- Note that analog system input/output pins other than the A/D input pins (LCD drive pins, comparator input pins, etc.) cannot accept +B signal input.
- Sample recommended circuits

• Input/Output equivalent circuits



Note: : Average output current = operating current × operating efficiency

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

11.2 Recommended Conditions

(V_{SS} = AV_{SS} = 0.0 V)

Parameter	Symbol	Value			Unit	Remarks	
		Min	Typ	Max			
Power supply voltage	V_{CC} AV_{CC}	4.5	5.0	5.5	V	Under normal operation	MB90V590G MB90F594G MB90594G
		3.0	—	5.5	V	Maintains RAM data in stop mode	
		4.75	5.0	5.25	V	Under normal operation	MB90F591G MB90591G
		3.0	—	5.25	V	Maintains RAM data in stop mode	
Smooth capacitor	C_S	0.022	0.1	1.0	µF	*	
Operating temperature	T_A	–40	—	+85	°C		

* : Use a ceramic capacitor or a capacitor with equivalent frequency characteristics. The smoothing capacitor to be connected to the V_{CC} pin must have a capacitance value higher than C_S.

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their representatives beforehand.

11.3 DC Characteristics

(MB90V590G, MB90F594G, MB90594G : V_{CC} = 5.0 V±10 %, V_{SS} = AV_{SS} = 0.0 V, T_A = −40 °C to +85 °C)
(MB90F591G, MB90591G : V_{CC} = 5.0 V±5 %, V_{SS} = AV_{SS} = 0.0 V, T_A = −40 °C to +85 °C)

Parameter	Symbol	Pin name	Condition	Value			Unit	Remarks
				Min	Typ	Max		
Input H voltage	V_{IHS}	CMOS hysteresis input	—	0.8 V_{CC}	—	V_{CC} +0.3	V	
	V_{IHM}	MD input	—	V_{CC} – 0.3	—	V_{CC} +0.3	V	
Input L voltage	V_{ILS}	CMOS hysteresis input	—	V_{SS} – 0.3	—	0.5V_{CC}	V	
	V_{ILM}	MD input	—	V_{SS} – 0.3	—	V_{SS} + 0.3	V	
	V_{ILR}	$\overline{RST}$, $\overline{HST}$	—	V_{SS} – 0.3	—	0.2V_{CC}	V	
Output H voltage	V_{OH1}	Normal output	V_{CC} = 4.5 V, I_{OH1} = –4.0 mA	V_{CC} – 0.5	—	—	V	
	V_{OH2}	High current output	V_{CC} = 4.5 V, I_{OH2} = –30.0 mA	V_{CC} – 0.5	—	—	V	
Output L voltage	V_{OL1}	Normal output	V_{CC} = 4.5 V, I_{OL1} = 4.0 mA	—	—	0.4	V	
	V_{OL2}	High current output	V_{CC} = 4.5 V, I_{OL2} = 30.0 mA	—	—	0.5	V	
Input leak current	I_{IL}	—	V_{CC} = 5.5 V, V_{SS} < V_I < V_{CC}	–5	—	5	µA	
Analog input leak current	I_{IAL}	AN0 to AN7	V_{CC} = 5.5 V, AV_{SS} < V_I < AV_{CC}	–1	—	1	µA	
Power supply current *	I_{CC}	V_{CC}	V_{CC} = 5.0 V±10%, Internal frequency : 16 MHz, At normal operation.	—	37	60	mA	MB90594G
				—	50	80	mA	MB90F594G
				—	50	80	mA	MB90F591G
				—	45	60	mA	MB90591G
	I_{CCS}		V_{CC} = 5.0 V±10%, Internal frequency : 16 MHz, At Sleep mode.	—	13	20	mA	MB90594G
				—	15	23	mA	MB90F594G
				—	15	23	mA	MB90F591G
				—	15	23	mA	MB90591G
	I_{CTS}		V_{CC} = 5.0 V±10%, Internal frequency : 2 MHz, At Timer mode	—	0.3	0.6	mA	MB90594G
				—	0.35	0.6	mA	MB90F594G
				—	0.35	0.6	mA	MB90F591G
				—	0.35	0.6	mA	MB90591G
	I_{CCH}		V_{CC} = 5.0 V±10%, At Stop mode, T_A = 25°C	—	5	20	µA	MB90594G
				—	5	20	µA	MB90F594G
				—	5	20	µA	MB90F591G
				—	5	20	µA	MB90591G

* : The power supply current testing conditions are when using the external clock.

(Continued)

11.4.4 UART0/1/2, Serial I/O Timing

(MB90V590G, MB90F594G, MB90594G : V_{CC} = 5.0 V±10 %, V_{SS} = AV_{SS} = 0.0 V, T_A = −40 °C to +85 °C)
(MB90F591G, MB90591G : V_{CC} = 5.0 V±5 %, V_{SS} = AV_{SS} = 0.0 V, T_A = −40 °C to +85 °C)

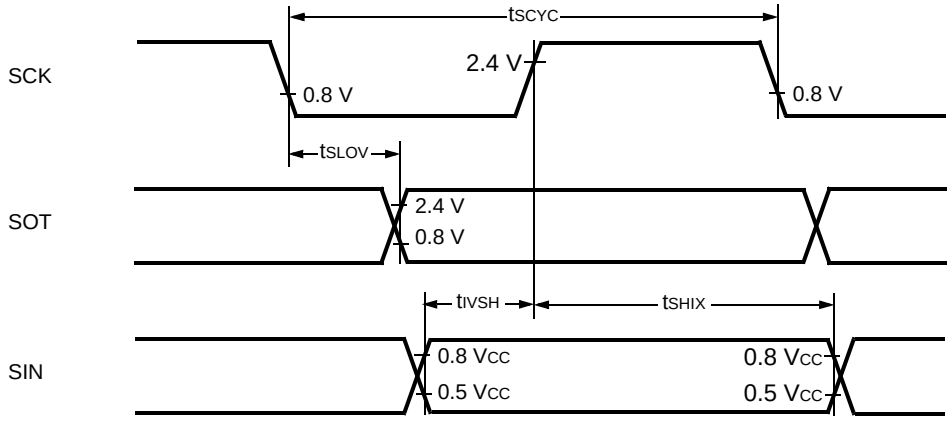
Parameter	Symbol	Pin name	Condition	Value		Unit	Remarks
				Min	Max		
Serial clock cycle time	t_{SCYC}	SCK0 to SCK3	Internal clock operation output pins are C_L = 80 pF + 1 TTL.	8 t_{CP}*	—	ns	
SCK ↓ ⇒ SOT delay time	t_{SLOV}	SCK0 to SCK3, SOT0 to SOT3		–80	80	ns	
Valid SIN ⇒ SCK ↑	t_{IVSH}	SCK0 to SCK3, SIN0 to SIN3		100	—	ns	
SCK ↑ ⇒ Valid SIN hold time	t_{SHIX}	SCK0 to SCK3, SIN0 to SIN3		60	—	ns	
Serial clock "H" pulse width	t_{SHSL}	SCK0 to SCK3	External clock operation output pins are C_L = 80 pF + 1 TTL.	4 t_{CP}	—	ns	
Serial clock "L" pulse width	t_{SLSH}	SCK0 to SCK3		4 t_{CP}	—	ns	
SCK ↓ ⇒ SOT delay time	t_{SLOV}	SCK0 to SCK3, SOT0 to SOT3		—	150	ns	
Valid SIN ⇒ SCK ↑	t_{IVSH}	SCK0 to SCK3, SIN0 to SIN3		60	—	ns	
SCK ↑ ⇒ Valid SIN hold time	t_{SHIX}	SCK0 to SCK3, SIN0 to SIN3		60	—	ns	

* : t_{CP} is the machine cycle (Unit : ns)

Notes:

- AC characteristic in CLK synchronized mode.
- C_L is load capacity value of pins when testing.

- **Internal Shift Clock Mode**



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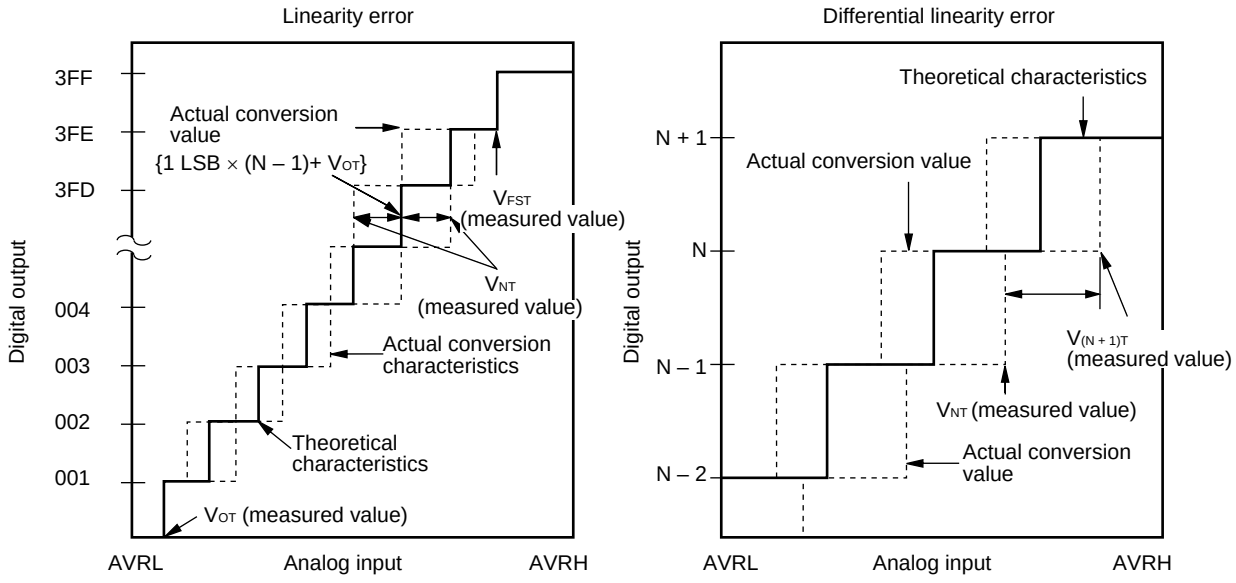


$$\text{Linearity error of digital output N} = \frac{V_{NT} - \{1\ \text{LSB} \times (N - 1) + V_{OT}\}}{1\ \text{LSB}}\ [\text{LSB}]$$

$$\text{Differential linearity error of digital N} = \frac{V_{(N+1)T} - V_{NT}}{1\ \text{LSB}} - 1\ \text{LSB}\ [\text{LSB}]$$

$$1\ \text{LSB} = \frac{V_{FST} - V_{OT}}{1022}\ [\text{V}]$$

V_{OT} : Voltage at transition of digital output from "000_H" to "001_H"

V_{FST} : Voltage at transition of digital output from "$3FE_H$" to "$3FF_H$"

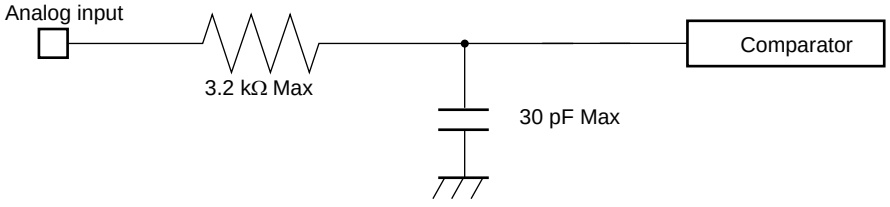
11.7 Notes on Using A/D Converter

Select the output impedance value for the external circuit of analog input according to the following conditions, :

- Output impedance values of the external circuit of 15 kΩ or lower are recommended.
- When capacitors are connected to external pins, the capacitance of several thousand times the internal capacitor value is recommended to minimized the effect of voltage distribution between the external capacitor and internal capacitor.

When the output impedance of the external circuit is too high, the sampling period for analog voltages may not be sufficient (sampling period = 4.00 μs @machine clock of 16 MHz).

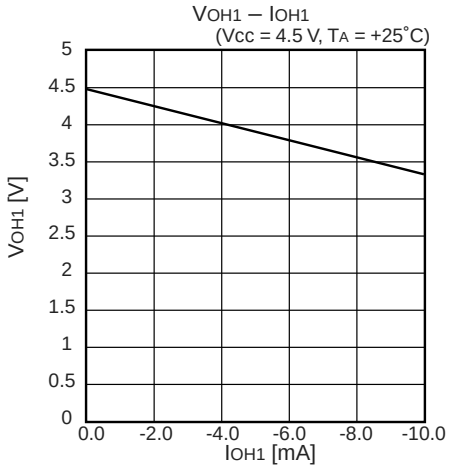
- **Equipment of analog input circuit model**

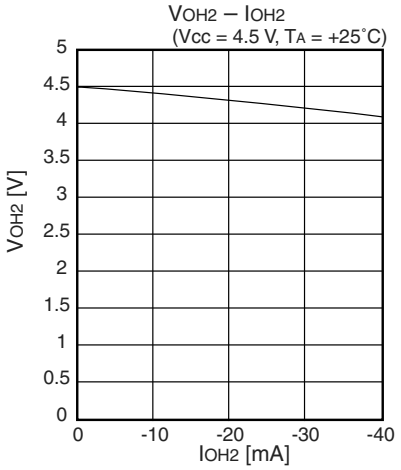


Note : Listed values must be considered as standards.

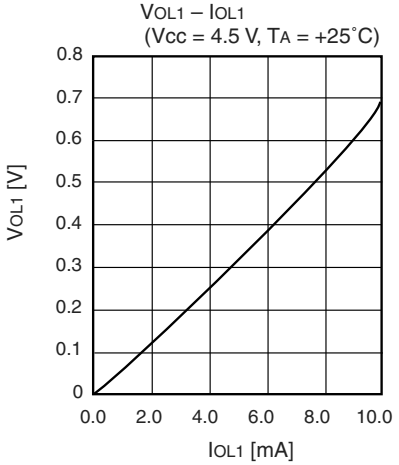
12. Example Characteristics

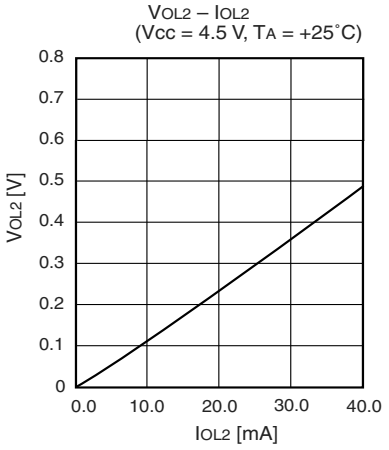
■ “H” Level Output Voltage





■ “L” Level Output





■ “H” Level Input Voltage/“L Level Input Voltage (Hysteresis Input)