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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	8051/52
Core Size	8-Bit
Speed	16MHz
Connectivity	EBI/EMI, Serial Port
Peripherals	POR, PWM, WDT
Number of I/O	24
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	256 x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	44-BQFP
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/nuvoton-technology-corporation-america/w79e201a16fl

5.5 Power Management

Like the standard 8051/52, the W79E201 has IDLE and POWER DOWN modes of operation. In POWER DOWN mode, all of the peripheral clocks are stopped, and chip operation stops completely. This mode consumes the least amount of power.

5.6 Memory Organization

The W79E201 separates memory into two sections, Program Memory and Data Memory. Program Memory stores instruction op-codes, while Data Memory stores data or memory-mapped devices.

Program Memory

On the standard 8051/52, only 64 KB of Program Memory can be addressed, and, in the W79E201, this area is the 16-KB Flash EPROM (AP Flash EPROM). All instructions are fetched from this area, and the MOVC instruction can also access this region. There is an auxiliary 4-KB Flash EPROM (LD Flash EPROM), where the loader program for In-System Programming (ISP) resides. The AP Flash EPROM is re-programmed by serial or parallel download according to this loader program.

Data Memory

The W79E201 can access up to 64 KB of external Data Memory. This memory is accessed by MOVX instructions, and any MOVX instructions to 0000H through FFFFH go to the expanded bus on Ports 0 and 2. This is the default condition.

The W79E201 also has the standard 256 bytes of on-chip Scratchpad RAM. This can be accessed either by direct addressing or by indirect addressing. There are also some Special Function Registers (SFRs), which can only be accessed by direct addressing. Since the Scratchpad RAM is only 256 bytes, it can be used only when data contents are small.

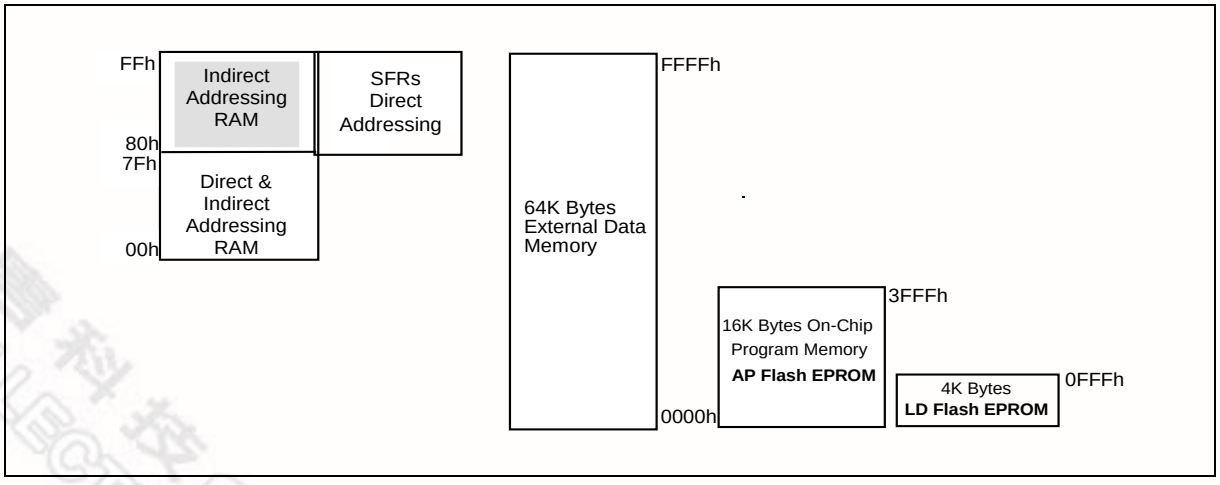


Figure 5-1 Memory Map

6. SPECIAL FUNCTION REGISTERS

The W79E201 uses Special Function Registers (SFR) to control and monitor peripherals. The SFR reside in register locations 80-FFh and are only accessed by direct addressing. The W79E201 contains all the SFR present in the standard 8051/52, as well as some additional SFR, and, in some cases, unused bits in the standard 8051/52 have new functions. SFR whose addresses end in 0 or 8 (hex) are bit-addressable. The following table of SFR is condensed, with eight locations per row. Empty locations indicate that there are no registers at these addresses. When a bit or register is not implemented, it reads high.

Table 1 Special Function Register Location Table

F8	EIP							
F0	B							
E8	EIE							
E0	ACC	ADCCON	ADCH		ADCCEN			
D8	WDCON	PWMP	PWM0	PWM1	PWMCON1	PWM2	PWM3	
D0	PSW							
C8	T2CON	T2MOD	RCAP2L	RCAP2H	TL2	TH2	PWMCON2	PWM4
C0				PWM5	PMR	Status		TA
B8	IP	SADEN						
B0	P3							
A8	IE	SADDR			SFRAL	SFRAH	SFRFD	SFRCN
A0	P2					P4		
98	SCON	SBUF						CHPCON
90	P1							
88	TCON	TMOD	TL0	TL1	TH0	TH1	CKCON	P0R
80	P0	SP	DPL	DPH				PCON

Note: The SFRs in the column with dark borders are bit-addressable.

Port 0

Bit:	7	6	5	4	3	2	1	0
	P0.7	P0.6	P0.5	P0.4	P0.3	P0.2	P0.1	P0.0

Mnemonic: P0 Address: 80h

Port 0 is an open-drain, bi-directional I/O port after chip is reset. Besides, it has internal pull-up resisters enabled by setting P0UP of P0R (8FH) to high. This port also provides a multiplexed, low-order address/data bus when the W79E201 accesses external memory.

Bit:	7	6	5	4	3	2	1	0
	TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0

Mnemonic: TCON Address: 88h

BIT	NAME	FUNCTION
7	TF1	Timer 1 overflow flag: This bit is set when Timer 1 overflows. It is cleared automatically when the program executes the Timer-1 interrupt service routine. Software can also set or clear this bit.
6	TR1	Timer 1 run control: This bit turns the Timer 1 on or off.
5	TF0	Timer 0 overflow flag: This bit is set when Timer 0 overflows. It is cleared automatically when the program executes the Timer-0 interrupt service routine. Software can also set or clear this bit.
4	TR0	Timer 0 run control: This bit turns Timer 0 on or off.
3	IE1	Interrupt 1 Edge Detect: Set by hardware when an edge / level is detected on $\overline{INT1}$. This bit is cleared by the hardware when the ISR is executed only if the interrupt is edge-triggered. Otherwise, it follows the pin.
2	IT1	Interrupt 1 type control: Specify falling-edge or low-level trigger for $\overline{INT1}$.
1	IE0	Interrupt 0 Edge Detect: Set by hardware when an edge / level is detected on $\overline{INT0}$. This bit is cleared by the hardware when the ISR is executed only if the interrupt is edge-triggered. Otherwise, it follows the pin.
0	IT0	Interrupt 0 type control: Specify falling-edge or low-level trigger for $\overline{INT0}$.

Timer Mode Control

Bit:	7	6	5	4	3	2	1	0
	GATE	$C/\overline{T}$	M1	M0	GATE	$C/\overline{T}$	M1	M0

Mnemonic: TMOD Address: 89h

BIT	NAME	FUNCTION
7	GATE	Gating control: When this bit is set, Timer 1 is enabled only while the $\overline{INT1}$ pin is high and the TR1 control bit is set. When clear, the $\overline{INT1}$ pin has no effect, and Timer 1 is enabled whenever TR1 is set.
6	$C/\overline{T}$	Timer or Counter Select: When clear, Timer 1 is incremented by the internal clock. When set, the timer counts falling edges on the Tx pin.
5	M1	Timer 1 mode select bit 1. See table below.
4	M0	Timer 1 mode select bit 0. See table below.

SM0, SM1: Mode Select bits:

SM0	SM1	MODE	DESCRIPTION	LENGTH	BAUD RATE
0	0	0	Synchronous	8	Tclk divided by 4 or 12
0	1	1	Asynchronous	10	Variable
1	0	2	Asynchronous	11	Tclk divided by 32 or 64
1	1	3	Asynchronous	11	Variable

Serial Data Buffer

Bit:	7	6	5	4	3	2	1	0
	SBUF.7	SBUF.6	SBUF.5	SBUF.4	SBUF.3	SBUF.2	SBUF.1	SBUF.0

Mnemonic: SBUF Address: 99h

SBUF.7–0: Serial data in the serial port is read from or written to this location. It actually consists of two separate 8-bit registers, the receive register and the transmit buffer. Read accesses get data from the receive register, and write accesses write to the transmit buffer.

ISP Control Register

Bit:	7	6	5	4	3	2	1	0
	SWRST/ REBOOT	-	LDAP	-	-	-	FBOOTSL	FPROGEN

Mnemonic: CHPCON Address: 9Fh

BIT	NAME	FUNCTION
7	SWRST/ REBOOT	Set this bit to reset the device. This has the same effect as asserting the RST pin. The microcontroller returns to its initial state, and this bit is cleared automatically. Reading this bit indicates whether or not the device is in ISP hardware reboot mode.
6	-	Reserved
5	LDAP	This bit is read-only. 1: Device is running the program in LD Flash EPROM 0: Device is running the program in AP Flash EPROM
4-2	-	Reserved
1	FBOOTSL	Program Location Selection. This bit should be set before entering ISP mode. 1: Run the program in LD Flash EPROM. 0: Run the program in AP Flash EPROM.
0	FPROGEN	FLASH EPROM Programming Enable. 1: Enable in-system programming mode. The erase, program and read operations are executed according to various SFR settings. In this mode, the device runs in IDLE state, so PCON.1 has no effect. 0: Disable in-system programming mode. The device returns to normal operations, and PCON.1 is functional again.

ISP Address Low Byte

Bit:	7	6	5	4	3	2	1	0
	SFRAL.7	SFRAL.6	SFRAL.5	SFRAL.4	SFRAL.3	SFRAL.2	SFRAL.1	SFRAL.0

Mnemonic: SFRAL Address: ACh

Low-byte destination address for In-System Programming operations. SFRAH and SFRAL are specific ROM locations for erase, program or read operations.

ISP Address High Byte

Bit:	7	6	5	4	3	2	1	0
	SFRAH.7	SFRAH.6	SFRAH.5	SFRAH.4	SFRAH.3	SFRAH.2	SFRAH.1	SFRAH.0

Mnemonic: SFRAH Address: ADh

High-byte destination address for In-System Programming operations. SFRAH and SFRAL are specific ROM locations for erase, program or read operations.

ISP Data Buffer

Bit:	7	6	5	4	3	2	1	0
	SFRFD.7	SFRFD.6	SFRFD.5	SFRFD.4	SFRFD.3	SFRFD.2	SFRFD.1	SFRFD.0

Mnemonic: SFRFD Address: AEh

In ISP mode, bytes read from ROM and bytes written to ROM go through SFRFD

ISP Operation Modes

Bit:	7	6	5	4	3	2	1	0
	-	WFWIN	OEN	CEN	CTRL3	CTRL2	CTRL1	CTRL0

Mnemonic: SFRCN Address: AFh

BIT	NAME	FUNCTION
7	-	Reserved
6	WFWIN	On-chip Flash EPROM bank select for in-system programming. This bit should be set by the loader program in ISP mode. 0: 16-KB Flash EPROM is the destination for re-programming. 1: 4-KB Flash EPROM is the destination for re-programming.
5	OEN	Flash EPROM output is enabled.
4	CEN	Flash EPROM chip is enabled.
3~0	CTRL[3:0]	The flash control signals. See table below.

BIT	NAME	FUNCTION
7	CY	Carry flag: Set when an arithmetic operation results in a carry being generated from the ALU. It is also used as the accumulator for bit operations.
6	AC	Auxiliary carry: Set when the previous operation resulted in a carry from the high-order nibble.
5	F0	User flag 0: A general-purpose flag that can be set or cleared by the user.
4	RS1	Register Bank select bits. See table below.
3	RS0	Register Bank select bits. See table below.
2	OV	Overflow flag: Set when a carry was generated from the seventh bit but not from the eighth bit, or vice versa, as a result of the previous operation.
1	F1	User flag 1: A general-purpose flag that can be set or cleared by the user.
0	P	Parity flag: Set and cleared by the hardware to indicate an odd or even number of 1's in the accumulator.

RS1, RS0: Register Bank select bits:

RS1	RS0	REGISTER BANK	ADDRESS
0	0	0	00-07h
0	1	1	08-0Fh
1	0	2	10-17h
1	1	3	18-1Fh

Watchdog Control

Bit:	7	6	5	4	3	2	1	0
	-	POR	-	-	WDIF	WTRF	EWT	RWT

Mnemonic: WDCON Address: D8h

BIT	NAME	FUNCTION
7	-	Reserved.
6	POR	Power-on reset flag. The hardware sets this flag during power–up, and it can only be cleared by software. This flag can also be written by software.
5-4	-	Reserved.
3	WDIF	Watchdog Timer Interrupt Flag. If the watchdog interrupt is enabled, the hardware sets this bit to indicate that the watchdog interrupt has occurred. If the interrupt is not enabled, this bit indicates that the time-out period has elapsed. This bit must be cleared by software.
2	WTRF	Watchdog Timer Reset Flag. If EWT is 0, the Watchdog Timer has no affect on this bit. Otherwise, the hardware sets this bit when the Watchdog Timer causes a reset. It can be cleared by software or a power-fail reset. It can be also read by software, which helps determine the cause of a reset.
1	EWT	Enable Watchdog-Timer Reset. Set this bit to enable the Watchdog Timer Reset function.
0	RWT	Reset Watchdog Timer. Set this bit to reset the Watchdog Timer before a time-out occurs. This bit is automatically cleared by the hardware.

BIT	NAME	FUNCTION
7	PWM3OE	Output enable for PWM3 0: Disable PWM3 Output. 1: Enable PWM3 Output.
6	PWM2OE	Output enable for PWM2 0: Disable PWM2 Output. 1: Enable PWM2 Output.
5	ENPWM3	Enable PWM3 0: Disable PWM3. 1: Enable PWM3.
4	ENPWM2	Enable PWM2 0: Disable PWM2. 1: Enable PWM2.
3	PWM1OE	Output enable for PWM1 0: Disable PWM1 Output. 1: Enable PWM1 Output.
2	PWM0OE	Output enable for PWM0 0: Disable PWM0 Output. 1: Enable PWM0 Output.
1	ENPWM1	Enable PWM1 0: Disable PWM1. 1: Enable PWM1.
0	ENPWM0	Enable PWM0 0: Disable PWM0. 1: Enable PWM0.

PWM 2 Register

Bit:	7	6	5	4	3	2	1	0
	PWM2.7	PWM2.6	PWM2.5	PWM2.4	PWM2.3	PWM2.2	PWM2.1	PWM2.0

Mnemonic: PWM2 Address: DDh

PWM 3 Register

Bit:	7	6	5	4	3	2	1	0
	PWM3.7	PWM3.6	PWM3.5	PWM3.4	PWM3.3	PWM3.2	PWM3.1	PWM3.0

Mnemonic: PWM3 Address: DEh

Accumulator

Bit:	7	6	5	4	3	2	1	0
	ACC.7	ACC.6	ACC.5	ACC.4	ACC.3	ACC.2	ACC.1	ACC.0

Mnemonic: ACC Address: E0h

Stretching only affects the MOVX instruction. There is no effect on any other instruction or its timing, it is as if the state of the CPU is held for the desired period. The timing waveforms when the stretch value is zero, one, and two are shown below.

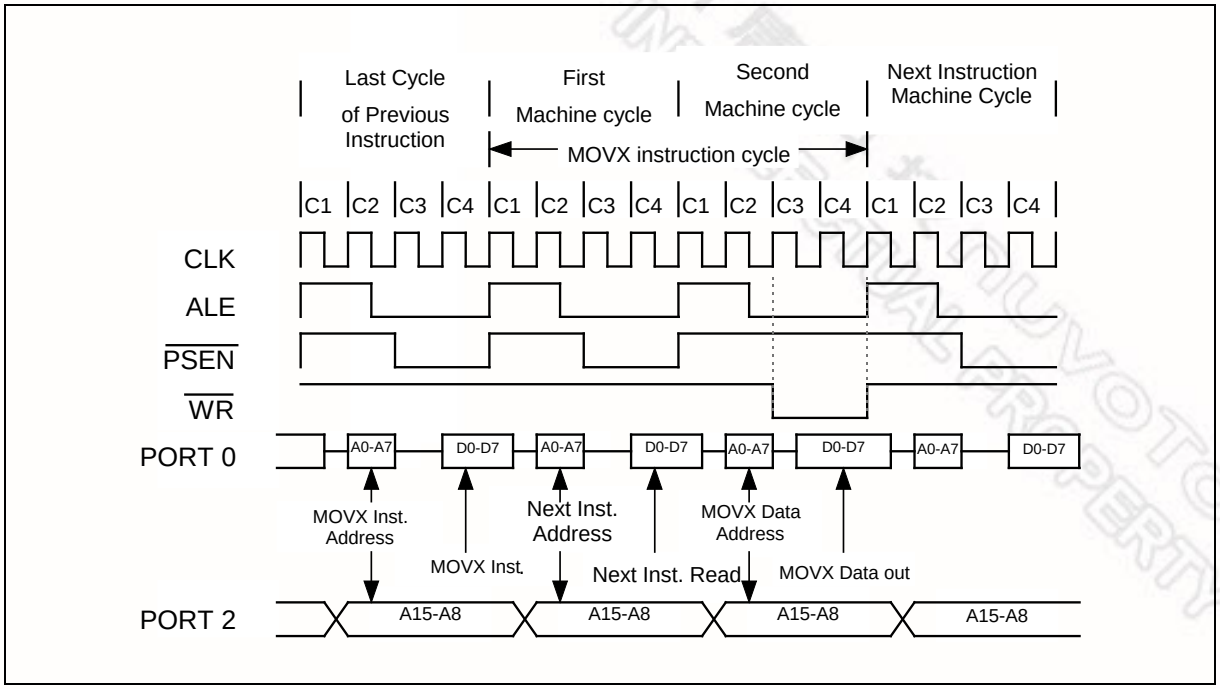


Figure 7-

10.2.3 Auto-Reload Mode, Counting Up/Down

This mode is enabled by clearing CP/$\overline{RL2}$ in T2CON and setting DCEN in T2MOD. In this mode, Timer/Counter 2 is a 16-bit up/down-counter, whose direction is controlled by the T2EX pin (1 = up, 0 = down). If Timer/Counter 2 is counting up, an overflow reloads TL2 and TH2 with the contents of the capture registers RCAP2L and RCAP2H. If Timer/Counter 2 is counting down, TL2 and TH2 are loaded with FFFFh when the contents of Timer/Counter 2 equal the capture registers RCAP2L and RCAP2H. Regardless of direction, reloading sets the TF2 bit. It also toggles the EXF2 bit, but the EXF2 bit can not generate an interrupt in this mode. This is illustrated below.

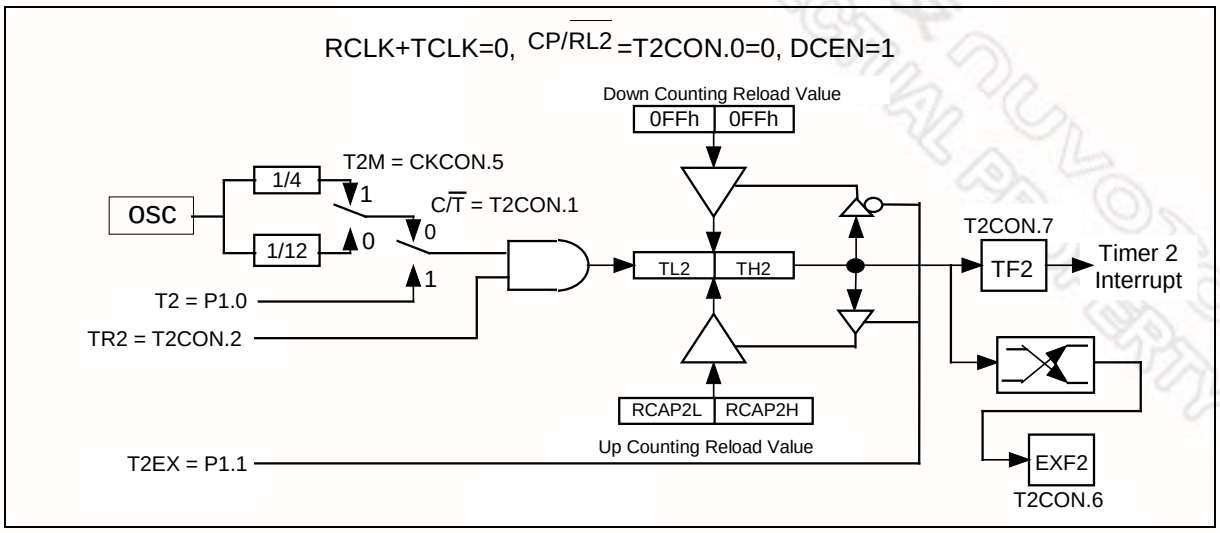


Figure 10-6 16-Bit Auto-reload Up/Down Counter

10.2.4 Baud Rate Generator Mode

Baud rate generator mode is enabled by setting either RCLK or TCLK in T2CON. In baud rate generator mode, Timer/Counter 2 is a 16-bit counter with auto-reload when the count rolls over from FFFFh. However, rolling-over does not set TF2. If EXEN2 is set, then a negative transition on the T2EX pin sets EXF2 bit in the T2CON register and causes an interrupt request.

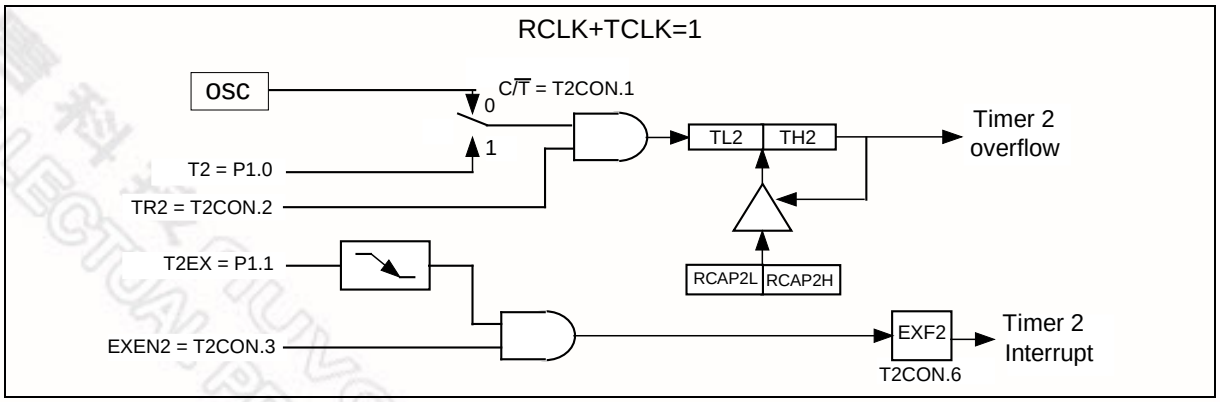


Figure 10-7 Baud Rate Generator Mode

If register PWM*n* is loaded with a new value, the associated output is updated immediately. By loading PWM*n* with 00H or FFH, the corresponding channel provides a constant high or low level output, respectively.[1]

Buffered PWM outputs may be used to drive DC motors. In this case, the rotation speed of the motor is proportional to the contents of PWM*n*. The repetition frequency Fpwm for channel *n* is given by:

$$Fpwm = \frac{Fosc}{2 \times (1 + PWMP) \times 255}$$

Prescale division factor = PWM + 1

$$\text{PWMn high/low ratio of } PWMn = \frac{(PWMn)}{255 - (PWMn)}$$

This gives a repetition frequency range of 123 Hz to 31.4 KHz (f_{osc} = 16 MHz).

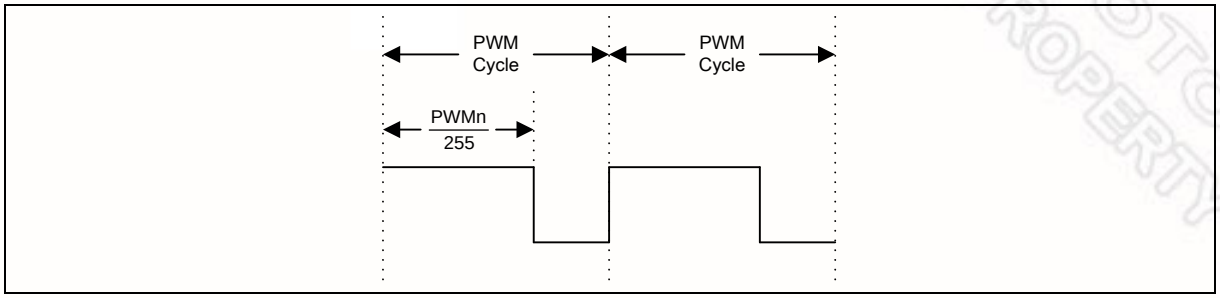


Figure 13-2 PWM Duty Cycle

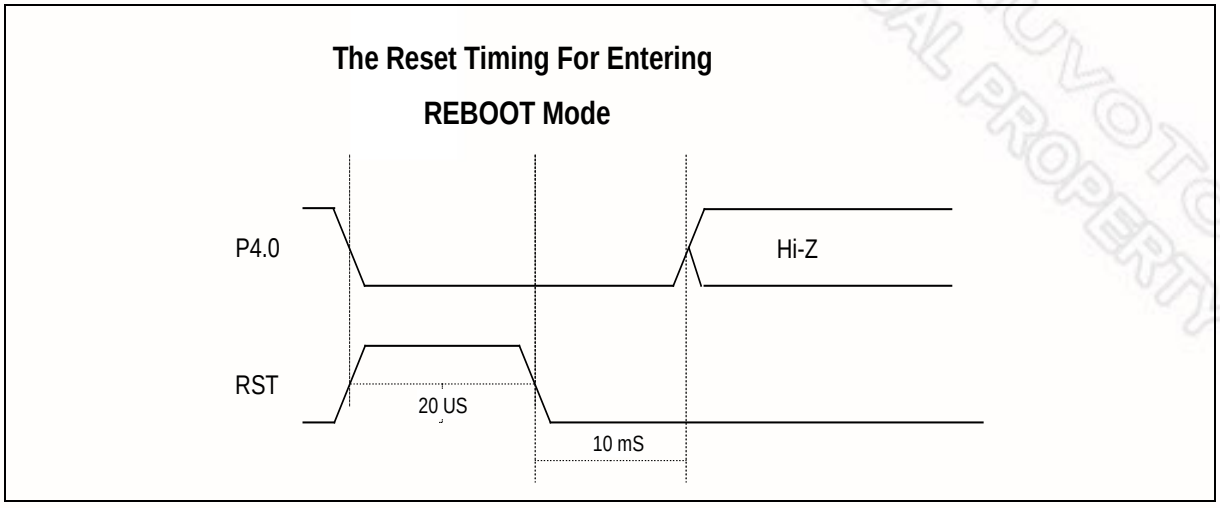
[1] Since the 8-bit counter counts modulo 255, it can never actually reach FFh, so the output remains low all the time.

16. H/W REBOOT MODE (BOOT FROM 4K BYTES OF LD FLASH EPROM)

The W79E201 boots from the AP Flash EPROM (16 KB) by default during an external reset. It is possible to boot from the LD Flash EPROM program (4 KB) instead. This is explained below. Note that it is necessary to add a 10-KΩ resistor on pin P4.0 to do this.

Reboot Mode

OPTION BITS	RST	P4.0	MODE
Bit3 L	H	L	REBOOT



Notes:

1: In application system design, user must take care the P4.0, ALE, /EA and /PSEN pin value at reset to avoid W79E201 entering the programming mode or REBOOT mode in normal operation.

17. IN-SYSTEM PROGRAMMING

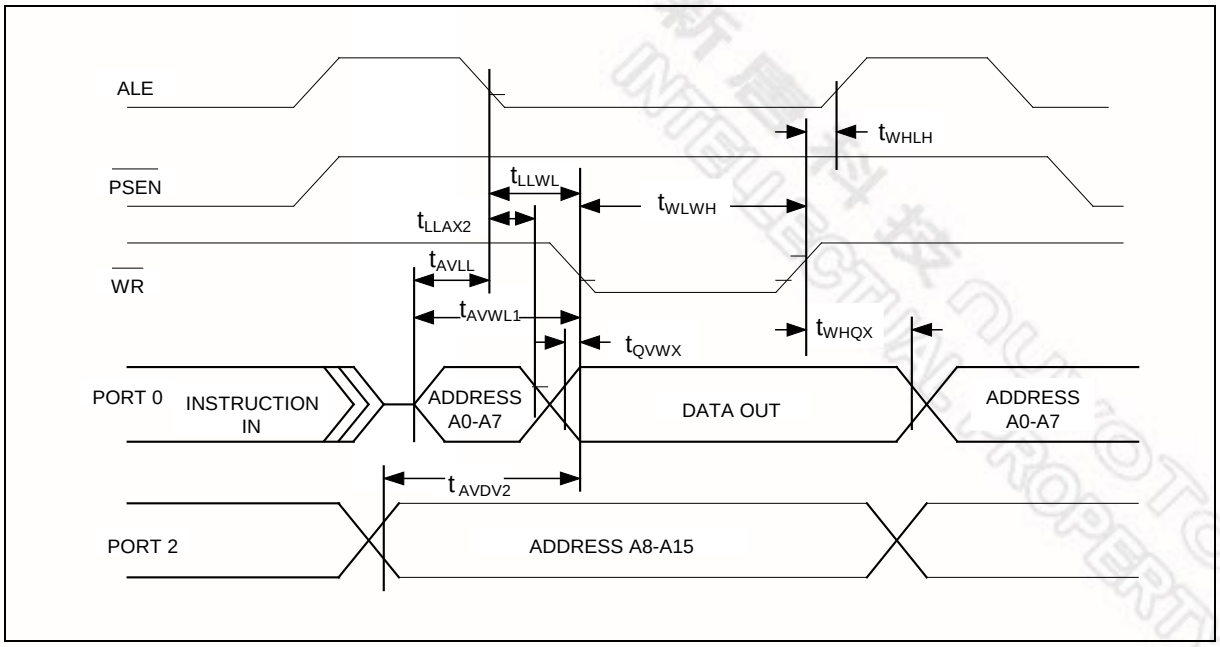
This section explains the key steps to use in-system programming. The steps depend on whether the loader program is located in the LD Flash EPROM or AP Flash EPROM, although both processes begin while the W79E201 is running with the AP Flash EPROM.

If the loader program is located in the LD Flash EPROM, the main program should set CHPCON to 03H, and then enter idle mode. When the W79E201 wakes up, the CPU switches to the LD Flash EPROM and executes a reset. (This reset switches to LD Flash EPROM memory too.) The loader program then sets the SFRCN register to update the AP Flash EPROM, and, afterwards, it requests a software reset (CHPCON = 83H) to switch back to the AP Flash EPROM. The CPU restarts using the updated program in the AP Flash EPROM.

If the loader program is located in the AP Flash EPROM, the main program should set CHPCON to 01H, and then enter idle mode. The loader program then sets the SFRCN register to update the LD Flash EPROM, and, afterwards, the CPU continues to run the program in the AP Flash EPROM.

Please see the In-system Programming Software Examples for additional details and code examples.

20.4.5 Data Memory Write Cycle



21. TYPICAL APPLICATION CIRCUITS

Expanded External Program Memory and Crystal

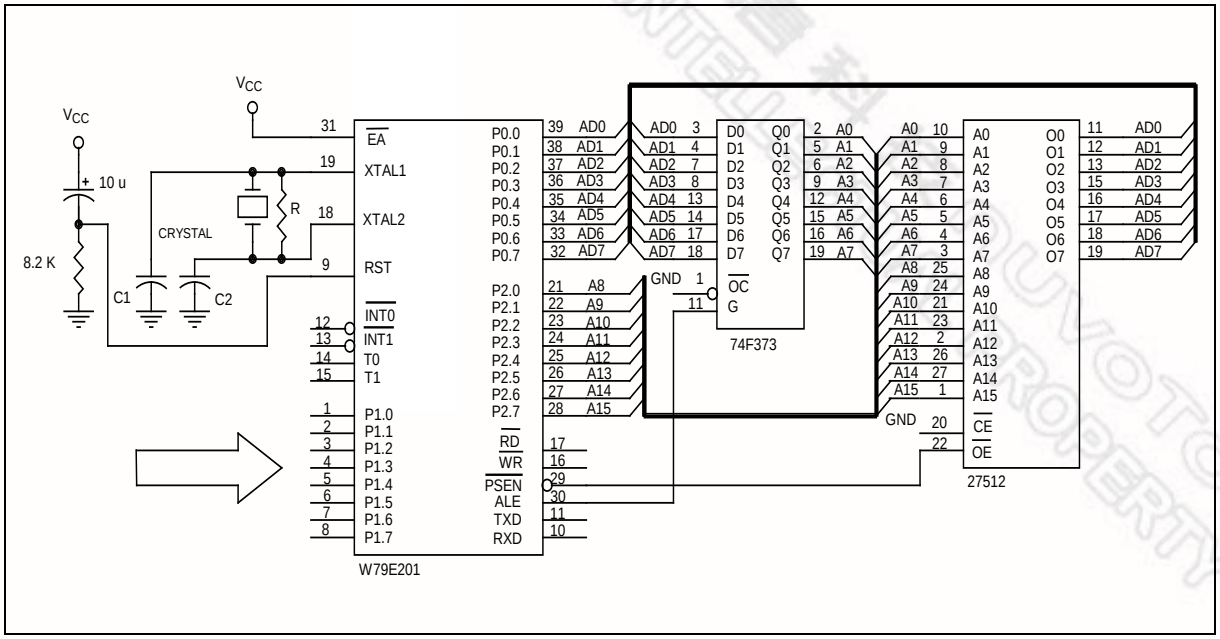


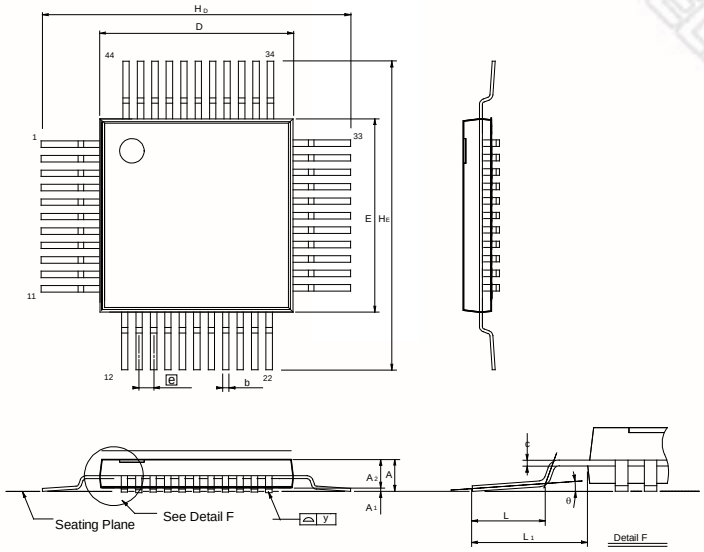
Figure A

CRYSTAL	C1	C2	R
12 MHz	Not necessary	Not necessary	Not necessary
16 MHz	Not necessary	Not necessary	Not necessary

Pull $\overline{EA}$ high to let the CPU fetch code in the embedded flash ROM, as long as the program counter is lower than 16K. When the program counter is higher than 16K, the CPU automatically fetches program code from extended external program memory.

22. PACKAGE DIMENSIONS

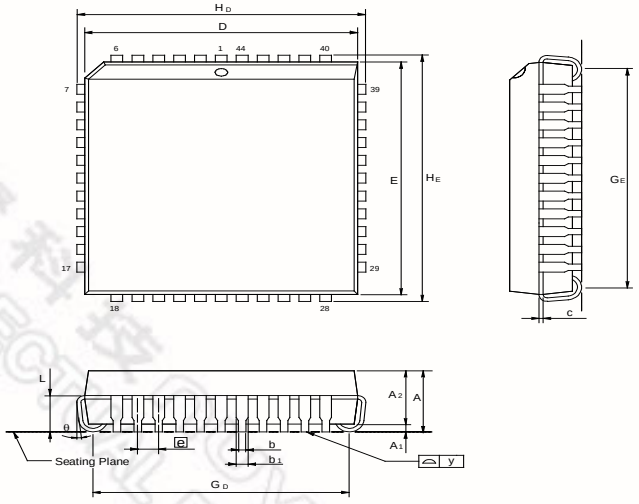
44-pin QFP



Symbol	Dimension in inch			Dimension in mm		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	---	---	---	---	---	---
A_1	0.002	0.01	0.02	0.05	0.25	0.5
A_2	0.075	0.081	0.087	1.90	2.05	2.20
b	0.01	0.014	0.018	0.25	0.35	0.45
c	0.004	0.006	0.010	0.101	0.152	0.254
D	0.390	0.394	0.398	9.9	10.00	10.1
E	0.390	0.394	0.398	9.9	10.00	10.1
e	0.025	0.031	0.036	0.635	0.80	0.952
H_D	0.510	0.520	0.530	12.95	13.2	13.45
H_E	0.510	0.520	0.530	12.95	13.2	13.45
L	0.025	0.031	0.037	0.65	0.8	0.95
L_1	0.051	0.063	0.075	1.295	1.6	1.905
y	—	—	0.003	—	—	0.08
θ	0°	—	7°	0°	—	7°

Notes:
1. Dimension D & E do not include interlead flash.
2. Dimension b does not include dambar protrusion/intrusion.
3. Controlling dimension: Millimeter
4. General appearance spec. should be based on final visual inspection spec.

44-pin PLCC



Symbol	Dimension in inches			Dimension in mm		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	—	—	0.185	—	—	4.699
A_1	0.020	—	—	0.508	—	—
A_2	0.145	0.150	0.155	3.683	3.81	3.937
b_1	0.026	0.028	0.032	0.66	0.711	0.813
b	0.016	0.018	0.022	0.406	0.457	0.559
c	0.008	0.010	0.014	0.203	0.254	0.356
D	0.648	0.653	0.658	16.46	16.59	16.71
E	0.648	0.653	0.658	16.46	16.59	16.71
e	0.050 BSC			1.27 BSC		
G_D	0.590	0.610	0.630	14.99	15.49	16.00
G_E	0.590	0.610	0.630	14.99	15.49	16.00
H_D	0.680	0.690	0.700	17.27	17.53	17.78
H_E	0.680	0.690	0.700	17.27	17.53	17.78
L	0.090	0.100	0.110	2.296	2.54	2.794
y	—	—	0.004	—	—	0.10

Notes:
1. Dimension D & E do not include interlead flash.
2. Dimension b1 does not include dambar protrusion/intrusion.
3. Controlling dimension: Inches
4. General appearance spec. should be based on final visual inspection spec.

```
        MOV     IE,#82H         ; IE = 82H, TIMER0 INTERRUPT ENABLED
        MOV     R6,#F0H
        MOV     R7,#FFH
        MOV     TL0,R6
        MOV     TH0,R7
        MOV     TCON,#10H       ; TCON = 10H, TR0 = 1, GO
        MOV     PCON,#01H       ; ENTER IDLE MODE
UPDATE_16K:
        MOV     TCON,#00H       ; TCON = 00H , TR = 0 TIM0 STOP
        MOV     IP,#00H         ; IP = 00H
        MOV     IE,#82H         ; IE = 82H, TIMER0 INTERRUPT ENABLED
        MOV     TMOD,#01H       ; TMOD = 01H, MODE1
        MOV     R6,#E0H          ; SET WAKE-UP TIME FOR ERASE OPERATION, ABOUT 15 ms
                                ;DEPENDING ON USER'S SYSTEM CLOCK RATE.
        MOV     R7,#B1H
        MOV     TL0,R6
        MOV     TH0,R7
ERASE_P_4K:
        MOV     SFRCN,#22H      ; SFRCN = 22H, ERASE 16K  AP Flash EPROM
        MOV     TCON,#10H       ; TCON = 10H, TR0 = 1,GO
        MOV     PCON,#01H       ; ENTER IDLE MODE (FOR ERASE OPERATION)
;*********************************************************************
;* BLANK CHECK
;*********************************************************************
        MOV     SFRCN,#0H       ; SFRCN = 00H, READ 16KB AP Flash EPROM
        MOV     SFRAH,#0H       ; START ADDRESS = 0H
        MOV     SFRAL,#0H
        MOV     R6,#FEH         ; SET TIMER FOR READ OPERATION, ABOUT 1.5 μS.
        MOV     R7,#FFH
        MOV     TL0,R6
        MOV     TH0,R7
blank_check_loop:
        SETB    TR0                     ; enable TIMER 0
        MOV     PCON,#01H               ; enter idle mode
        MOV     A,SFRFD                 ; read one byte
        CJNE    A,#FFH,blank_check_error
        INC     SFRAL                   ; next address
        MOV     A,SFRAL
        JNZ     blank_check_loop
        INC     SFRAH
```

```
        MOV     A,SFRAH
        CJNE    A,#40H,blank_check_loop         ; end address = FFFFH
        JMP     PROGRAM_16KROM
blank_check_error:
        JMP     $
;*****************************************************************************
;* RE-PROGRAMMING 16KB AP Flash EPROM BANK
;*****************************************************************************
PROGRAM_16KROM:
        MOV     R2,#00H         ; Target low byte address
        MOV     R1,#00H         ; TARGET HIGH BYTE ADDRESS
        MOV     DPTR,#0H
        MOV     SFRAH,R1        ; SFRAH, Target  high address
        MOV     SFRCN,#21H      ; SFRCN = 21H, PROGRAM 16K AP Flash EPROM
        MOV     R6,#BDH         ; SET TIMER FOR PROGRAMMING, ABOUT 50 μS.
        MOV     R7,#FFH
        MOV     TL0,R6
        MOV     TH0,R7
PROG_D_16K:
        MOV     SFRAL,R2        ; SFRAL = LOW BYTE ADDRESS
        CALL    GET_BYTE_FROM_PC_TO_ACC   ;THIS POOGRAM IS BASED ON USER'S CIRCUIT.
        MOV     @DPTR,A         ; SAVE DATA  INTO SRAM TO VERIFY CODE.
        MOV     SFRFD,A         ; SFRFD = data IN
        MOV     TCON,#10H       ; TCON = 10H, TR0 = 1,GO
        MOV     PCON,#01H       ; ENTER IDLE MODE (PRORGAMMING)
        INC     DPTR
        INC     R2
        CJNE    R2,#04H,PROG_D_16K
        INC     R1
        MOV     SFRAH,R1
        CJNE    R1,#40H,PROG_D_16K
;*****************************************************************************
; * VERIFY 16KB AP Flash EPROM BANK
;*****************************************************************************
        MOV     R4,#03H         ; ERROR COUNTER
        MOV     R6,#FEH         ; SET TIMER FOR READ VERIFY, ABOUT 1.5 μS.
        MOV     R7,#FFH
        MOV     TL0,R6
        MOV     TH0,R7
```

24. REVISION HISTORY

VERSION	DATE	PAGE	DESCRIPTION
A1	November 9, 2004	-	Initial Issued
A2	December 16, 2004	58 / 60	1.To add PWM Function Description 2.To add ADC Function Description
A3	April 19, 2005	87	1. Add Important Notice
A4	June 16, 2005	3 61	Add Lead free (RoHS) part numbers Modify PWM Function block diagram
A5	September 5, 2005	- 5 53	Re-organize document Modify pin description of port 0 Modify the diagram of serial port mode 2
A6	October 3, 2005	8 9	Correct AP Flash ROM size Correct the explanation of Port 0
A7	November 16, 2005	75	Revise "Pull $\overline{EA}$ low" to "Pull $\overline{EA}$ high"
A8	March 28, 2006	16	Revise SM0 and SM1
A9	November 6, 2006		Remove block diagram
		3	Remove all Leaded package parts
		65	Revise the input current P1,P2,P3 from -50uA(Min.) to 70uA(Min.)
		65	Revise the Logic 1 to 0 Transition Current P1, P2, P3 from -500uA(Min.) to -750uA(Mmin.)
		66	Revise the Sink current P1,P3 from 10mA(Max.) to 15mA(Max.)
		66	Revise the Sink current P0,P2,ALE, $\overline{PSEN}$ from 12mA(Max.) to 15mA(Max.)

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