Nuvoton Technology Corporation - W79E201A16PL Datasheet

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	8051/52
Core Size	8-Bit
Speed	16MHz
Connectivity	EBI/EMI, Serial Port
Peripherals	POR, PWM, WDT
Number of I/O	24
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	256 x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	44-LCC (J-Lead)
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/nuvoton-technology-corporation-america/w79e201a16pl

6. SPECIAL FUNCTION REGISTERS

The W79E201 uses Special Function Registers (SFR) to control and monitor peripherals. The SFR reside in register locations 80-FFh and are only accessed by direct addressing. The W79E201 contains all the SFR present in the standard 8051/52, as well as some additional SFR, and, in some cases, unused bits in the standard 8051/52 have new functions. SFR whose addresses end in 0 or 8 (hex) are bit-addressable. The following table of SFR is condensed, with eight locations per row. Empty locations indicate that there are no registers at these addresses. When a bit or register is not implemented, it reads high.

Table 1 Special Function Register Location Table

F8	EIP							
F0	B							
E8	EIE							
E0	ACC	ADCCON	ADCH		ADCCEN			
D8	WDCON	PWMP	PWM0	PWM1	PWMCON1	PWM2	PWM3	
D0	PSW							
C8	T2CON	T2MOD	RCAP2L	RCAP2H	TL2	TH2	PWMCON2	PWM4
C0				PWM5	PMR	Status		TA
B8	IP	SADEN						
B0	P3							
A8	IE	SADDR			SFRAL	SFRAH	SFRFD	SFRCN
A0	P2					P4		
98	SCON	SBUF						CHPCON
90	P1							
88	TCON	TMOD	TL0	TL1	TH0	TH1	CKCON	P0R
80	P0	SP	DPL	DPH				PCON

Note: The SFRs in the column with dark borders are bit-addressable.

Port 0

Bit:	7	6	5	4	3	2	1	0
	P0.7	P0.6	P0.5	P0.4	P0.3	P0.2	P0.1	P0.0

Mnemonic: P0 Address: 80h

Port 0 is an open-drain, bi-directional I/O port after chip is reset. Besides, it has internal pull-up resisters enabled by setting P0UP of P0R (8FH) to high. This port also provides a multiplexed, low-order address/data bus when the W79E201 accesses external memory.

Stack Pointer

Bit:	7	6	5	4	3	2	1	0
	SP.7	SP.6	SP.5	SP.4	SP.3	SP.2	SP.1	SP.0

Mnemonic: SP Address: 81h

The Stack Pointer stores the address in Scratchpad RAM where the stack begins. It always points to the top of the stack.

Data Pointer Low

Bit:	7	6	5	4	3	2	1	0
	DPL.7	DPL.6	DPL.5	DPL.4	DPL.3	DPL.2	DPL.1	DPL.0

Mnemonic: DPL Address: 82h

This is the low byte of the standard-8051/52, 16-bit data pointer.

Data Pointer High

Bit:	7	6	5	4	3	2	1	0
	DPH.7	DPH.6	DPH.5	DPH.4	DPH.3	DPH.2	DPH.1	DPH.0

Mnemonic: DPH Address: 83h

This is the high byte of the standard-8051/52, 16-bit data pointer.

Power Control

Bit:	7	6	5	4	3	2	1	0
	SM0D	SMOD0	-	-	GF1	GF0	PD	IDL

Mnemonic: PCON Address: 87h

BIT	NAME	FUNCTION
7	SMOD	1: This bit doubles the serial-port baud rate in modes 1, 2 and 3.
6	SMOD0	0: Disable Framing Error Detection. SCON.7 acts as per the standard 8051/52 function. 1: Enable Framing Error Detection. SCON.7 indicates a Frame Error and acts as the FE flag.
5-4	-	Reserved
3	GF1	General-purpose user flag.
2	GF0	General-purpose user flag.
1	PD	1: Go into POWER DOWN mode. In this mode, all clocks and program execution are stopped.
0	IDL	1: Go into IDLE mode. In this mode, the CPU clock stops, so program execution stops too. However, the clock to the serial port, ADC, timer and interrupt blocks does not stop, so these blocks continue operating.

Timer Control

Bit:	7	6	5	4	3	2	1	0
	TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0

Mnemonic: TCON Address: 88h

BIT	NAME	FUNCTION
7	TF1	Timer 1 overflow flag: This bit is set when Timer 1 overflows. It is cleared automatically when the program executes the Timer-1 interrupt service routine. Software can also set or clear this bit.
6	TR1	Timer 1 run control: This bit turns the Timer 1 on or off.
5	TF0	Timer 0 overflow flag: This bit is set when Timer 0 overflows. It is cleared automatically when the program executes the Timer-0 interrupt service routine. Software can also set or clear this bit.
4	TR0	Timer 0 run control: This bit turns Timer 0 on or off.
3	IE1	Interrupt 1 Edge Detect: Set by hardware when an edge / level is detected on $\overline{INT1}$. This bit is cleared by the hardware when the ISR is executed only if the interrupt is edge-triggered. Otherwise, it follows the pin.
2	IT1	Interrupt 1 type control: Specify falling-edge or low-level trigger for $\overline{INT1}$.
1	IE0	Interrupt 0 Edge Detect: Set by hardware when an edge / level is detected on $\overline{INT0}$. This bit is cleared by the hardware when the ISR is executed only if the interrupt is edge-triggered. Otherwise, it follows the pin.
0	IT0	Interrupt 0 type control: Specify falling-edge or low-level trigger for $\overline{INT0}$.

Timer Mode Control

Bit:	7	6	5	4	3	2	1	0
	GATE	$C/\overline{T}$	M1	M0	GATE	$C/\overline{T}$	M1	M0

Mnemonic: TMOD Address: 89h

BIT	NAME	FUNCTION
7	GATE	Gating control: When this bit is set, Timer 1 is enabled only while the $\overline{INT1}$ pin is high and the TR1 control bit is set. When clear, the $\overline{INT1}$ pin has no effect, and Timer 1 is enabled whenever TR1 is set.
6	$C/\overline{T}$	Timer or Counter Select: When clear, Timer 1 is incremented by the internal clock. When set, the timer counts falling edges on the Tx pin.
5	M1	Timer 1 mode select bit 1. See table below.
4	M0	Timer 1 mode select bit 0. See table below.

WD1	WD0	INTERRUPT TIME-OUT	RESET TIME-OUT
0	0	2^{17}	2^{17} + 512
0	1	2^{20}	2^{20} + 512
1	0	2^{23}	2^{23} + 512
1	1	2^{26}	2^{26} + 512

MD2, MD1, MD0: Stretch MOVX select bits:

MD2	MD1	MD0	STRETCH VALUE	MOVX DURATION
0	0	0	0	2 machine cycles
0	0	1	1	3 machine cycles *(Default)*
0	1	0	2	4 machine cycles
0	1	1	3	5 machine cycles
1	0	0	4	6 machine cycles
1	0	1	5	7 machine cycles
1	1	0	6	8 machine cycles
1	1	1	7	9 machine cycles

Port 0 pull-up resister

Bit:	7	6	5	4	3	2	1	0
	-	-	-	-	-	-	-	P0UP

Mnemonic: P0R Address: 8Fh

BIT	NAME	FUNCTION
7~1	-	Reserved
0	P0UP	Port 0 Pull-Up Resistor 0: No pull-up resistor 1: Pull-up resistor (~10 KΩ)

Port 1

Bit:	7	6	5	4	3	2	1	0
	P1.7	P1.6	P1.5	P1.4	P1.3	P1.2	P1.1	P1.0

Mnemonic: P1 Address: 90h

P1.7–0: General-purpose digital input port or analog input port AD0~AD7. For digital input, port-read instructions read the port pins, while read-modify-write instructions read the port latch. Additional functions are described below. This port is also used for 8 channels of analog inputs from ADC0 to ADC7.

SM0, SM1: Mode Select bits:

SM0	SM1	MODE	DESCRIPTION	LENGTH	BAUD RATE
0	0	0	Synchronous	8	Tclk divided by 4 or 12
0	1	1	Asynchronous	10	Variable
1	0	2	Asynchronous	11	Tclk divided by 32 or 64
1	1	3	Asynchronous	11	Variable

Serial Data Buffer

Bit:	7	6	5	4	3	2	1	0
	SBUF.7	SBUF.6	SBUF.5	SBUF.4	SBUF.3	SBUF.2	SBUF.1	SBUF.0

Mnemonic: SBUF Address: 99h

SBUF.7–0: Serial data in the serial port is read from or written to this location. It actually consists of two separate 8-bit registers, the receive register and the transmit buffer. Read accesses get data from the receive register, and write accesses write to the transmit buffer.

ISP Control Register

Bit:	7	6	5	4	3	2	1	0
	SWRST/ REBOOT	-	LDAP	-	-	-	FBOOTSL	FPROGEN

Mnemonic: CHPCON Address: 9Fh

BIT	NAME	FUNCTION
7	SWRST/ REBOOT	Set this bit to reset the device. This has the same effect as asserting the RST pin. The microcontroller returns to its initial state, and this bit is cleared automatically. Reading this bit indicates whether or not the device is in ISP hardware reboot mode.
6	-	Reserved
5	LDAP	This bit is read-only. 1: Device is running the program in LD Flash EPROM 0: Device is running the program in AP Flash EPROM
4-2	-	Reserved
1	FBOOTSL	Program Location Selection. This bit should be set before entering ISP mode. 1: Run the program in LD Flash EPROM. 0: Run the program in AP Flash EPROM.
0	FPROGEN	FLASH EPROM Programming Enable. 1: Enable in-system programming mode. The erase, program and read operations are executed according to various SFR settings. In this mode, the device runs in IDLE state, so PCON.1 has no effect. 0: Disable in-system programming mode. The device returns to normal operations, and PCON.1 is functional again.

ISP Address Low Byte

Bit:	7	6	5	4	3	2	1	0
	SFRAL.7	SFRAL.6	SFRAL.5	SFRAL.4	SFRAL.3	SFRAL.2	SFRAL.1	SFRAL.0

Mnemonic: SFRAL Address: ACh

Low-byte destination address for In-System Programming operations. SFRAH and SFRAL are specific ROM locations for erase, program or read operations.

ISP Address High Byte

Bit:	7	6	5	4	3	2	1	0
	SFRAH.7	SFRAH.6	SFRAH.5	SFRAH.4	SFRAH.3	SFRAH.2	SFRAH.1	SFRAH.0

Mnemonic: SFRAH Address: ADh

High-byte destination address for In-System Programming operations. SFRAH and SFRAL are specific ROM locations for erase, program or read operations.

ISP Data Buffer

Bit:	7	6	5	4	3	2	1	0
	SFRFD.7	SFRFD.6	SFRFD.5	SFRFD.4	SFRFD.3	SFRFD.2	SFRFD.1	SFRFD.0

Mnemonic: SFRFD Address: AEh

In ISP mode, bytes read from ROM and bytes written to ROM go through SFRFD

ISP Operation Modes

Bit:	7	6	5	4	3	2	1	0
	-	WFWIN	OEN	CEN	CTRL3	CTRL2	CTRL1	CTRL0

Mnemonic: SFRCN Address: AFh

BIT	NAME	FUNCTION
7	-	Reserved
6	WFWIN	On-chip Flash EPROM bank select for in-system programming. This bit should be set by the loader program in ISP mode. 0: 16-KB Flash EPROM is the destination for re-programming. 1: 4-KB Flash EPROM is the destination for re-programming.
5	OEN	Flash EPROM output is enabled.
4	CEN	Flash EPROM chip is enabled.
3~0	CTRL[3:0]	The flash control signals. See table below.

BIT	NAME	FUNCTION
7~3	-	Reserved.
2	ALE-OFF	0: ALE expression is enabled during on-board program and data accesses. 1: ALE expression is disabled. Keep the logic in the high state. External memory accesses automatically enable ALE, regardless of ALE-OFF.
1~0	-	Reserved.

Status Register

Bit:	7	6	5	4	3	2	1	0
	-	HIP	LIP	-	-	-	SPTA0	SPRA0

Mnemonic: STATUS Address: C5h

BIT	NAME	FUNCTION
7	-	Reserved.
6	HIP	High-Priority Interrupt Status. When set, it indicates that the software is servicing a high-priority interrupt. This bit is cleared when the program executes the corresponding RETI instruction.
5	LIP	Low-Priority Interrupt Status. When set, it indicates that the software is servicing a low-priority interrupt. This bit is cleared when the program executes the corresponding RETI instruction.
4-2	-	Reserved.
1	SPTA0	Serial-Port Transmit Activity. This bit is set when the serial port is transmitting data. It is cleared when the TI bit is set by the hardware.
0	SPRA0	Serial-Port Receive Activity. This bit is set when the serial port is receiving data. It is cleared when the RI bit is set by the hardware.

Timed Access

Bit:	7	6	5	4	3	2	1	0
	TA.7	TA.6	TA.5	TA.4	TA.3	TA.2	TA.1	TA.0

Mnemonic: TA Address: C7h

TA: This register controls the access to protected bits. To access protected bits, the program must write AAH, followed immediately by 55H, to TA. This opens a window for three machine cycles, during which the program can write to protected bits.

Timer 2 Control

Bit:	7	6	5	4	3	2	1	0
	TF2	EXF2	RCLK	TCLK	EXEN2	TR2	$C/\overline{T2}$	$CP/\overline{RL2}$

Mnemonic: T2CON Address: C8h

ACC.7-0: The A (or ACC) register is the standard 8051/52 accumulator.

ADC Control Register

Bit:	7	6	5	4	3	2	1	0
	ADC.1	ADC.0	ADCEX	ADCI	ADCS	AADR2	AADR1	AADR0

Mnemonic: ADCCON Address: E1h

<table>
<tr><th>BIT</th><th>NAME</th><th>FUNCTION</th></tr>
<tr><td>7</td><td>ADC.1</td><td>Bit 1 of ADC result.</td></tr>
<tr><td>6</td><td>ADC.0</td><td>Bit 0 of ADC result.</td></tr>
<tr><td>5</td><td>ADCEX</td><td>Enable STADC-triggered conversion
0: Conversion can only be started by software (i.e., by setting ADCS).
1: Conversion can be started by software or by a rising edge on STADC (pin P2.0).</td></tr>
<tr><td>4</td><td>ADCI</td><td>ADC Interrupt flag: This flag is set when the result of an A/D conversion is ready. This generates an ADC interrupt, if it is enabled. The flag may be cleared by the ISR. While this flag is 1, the ADC cannot start a new conversion. ADCI can not be set by software.</td></tr>
<tr><td>3</td><td>ADCS</td><td>ADC Start and Status: Set this bit to start an A/D conversion. It may also be set by STADC if ADCEX is 1. This signal remains high while the ADC is busy and is reset right after ADCI is set. ADCS can not be reset by software, and the ADC cannot start a new conversion while ADCS is high.
<table>
<tr><th>ADCI</th><th>ADCS</th><th>ADC Status</th></tr>
<tr><td>0</td><td>0</td><td>ADC not busy; a conversion can be started</td></tr>
<tr><td>0</td><td>1</td><td>ADC busy; start of a new conversion is blocked</td></tr>
<tr><td>1</td><td>0</td><td>Conversion completed; start of a new conversion requires ADCI=0</td></tr>
<tr><td>1</td><td>1</td><td>Conversion completed; start of a new conversion requires ADCI=0</td></tr>
</table>
It is recommended to clear ADCI before ADCS is set. However, if ADCI is cleared and ADCS is set at the same time, a new A/D conversion may start on the same channel.</td></tr>
<tr><td>2</td><td>AADR2</td><td>See table below.</td></tr>
<tr><td>1</td><td>AADR1</td><td>See table below.</td></tr>
<tr><td>0</td><td>AADR0</td><td>See table below.</td></tr>
</table>

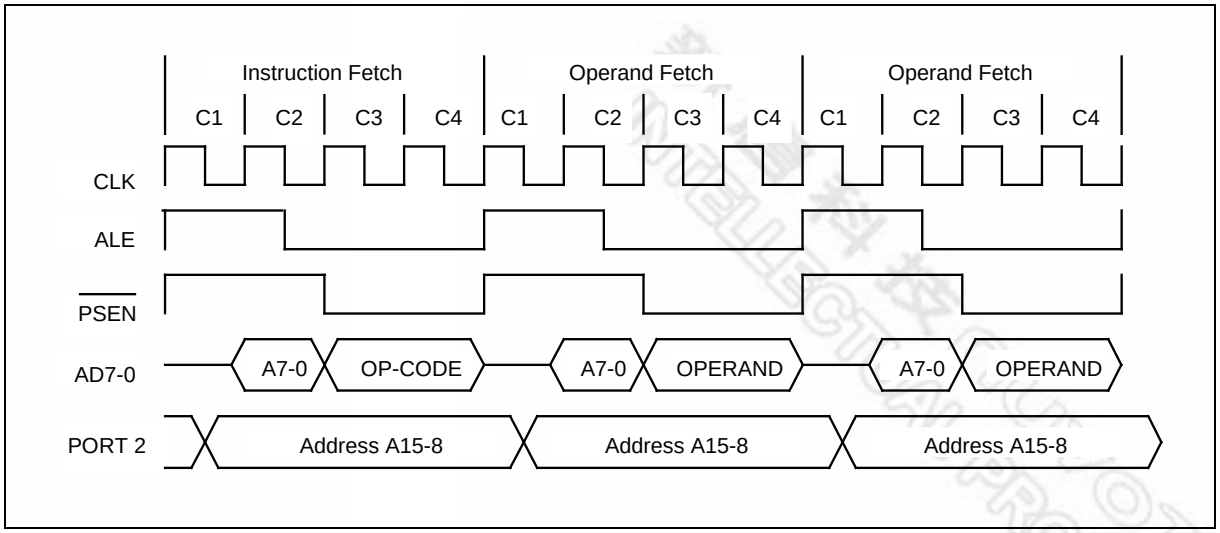

Figure 7-3 Three Cycle Instruction Timing

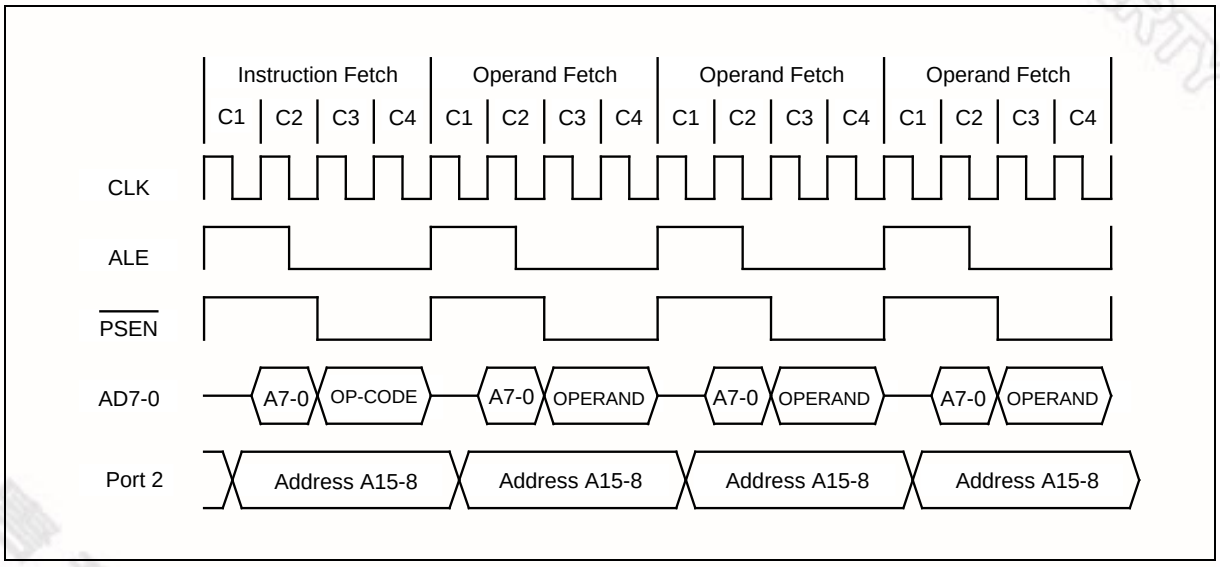

Figure 7-4 Four Cycle Instruction Timing

Stretching only affects the MOVX instruction. There is no effect on any other instruction or its timing, it is as if the state of the CPU is held for the desired period. The timing waveforms when the stretch value is zero, one, and two are shown below.

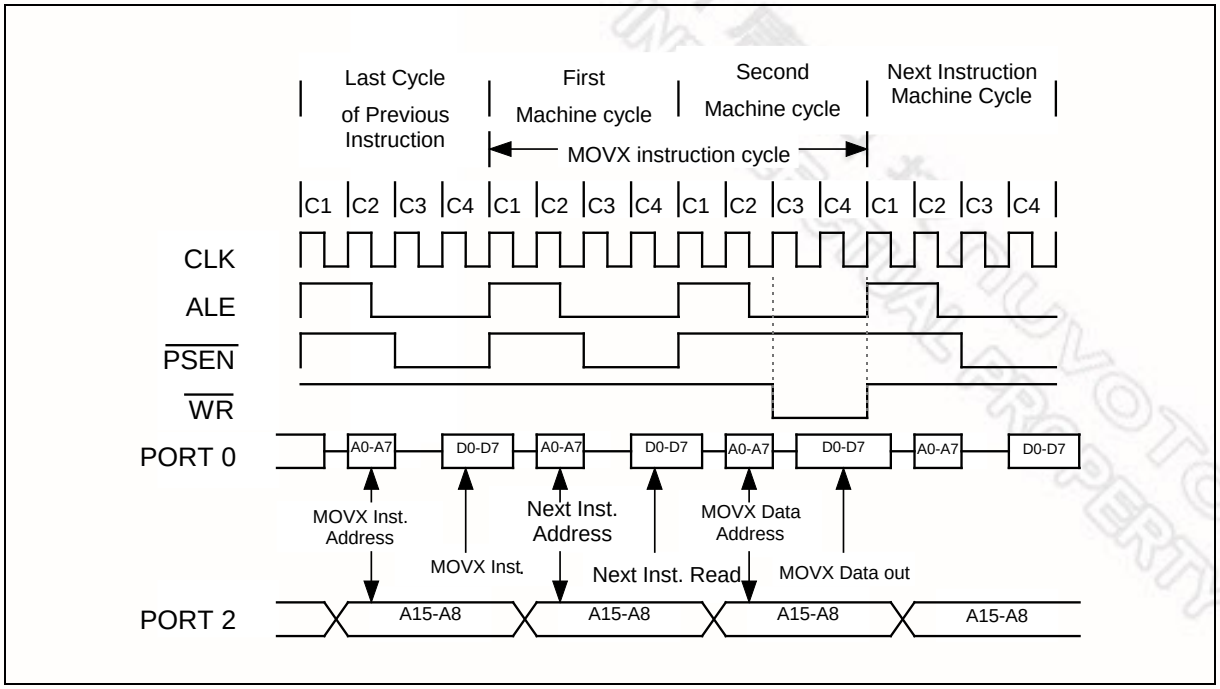

Figure 7-6 Data Memory Write with Stretch Value = 0

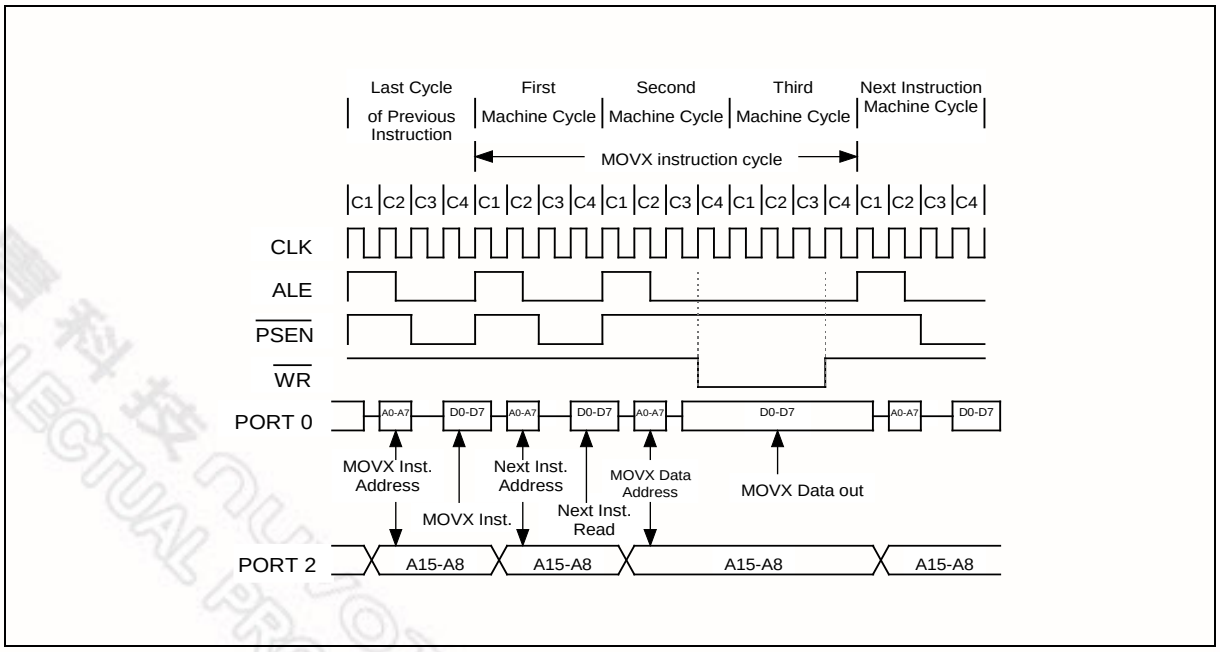

Figure 7-7 Data Memory Write with Stretch Value = 1

Table 4 SFR Reset Value, continued

SFR NAME	RESET VALUE	SFR NAME	RESET VALUE
TL0	00000000b	RCAP2L	00000000b
TL1	00000000b	RCAP2H	00000000b
TH0	00000000b	TL2	00000000b
TH1	00000000b	TH2	00000000b
CKCON	00000001b	PSW	00000000b
P1	11111111b	WDCON	see below
SCON	00000000b	PWMP	00000000b
SBUF	xxxxxxxxb	PWMCON1	00000000b
P2	11111111b	PWM0	00000000b
P0R	00000000b	PWM1	00000000b
P4	Xxxxxxx1b	PWM2	00000000b
IE	00000000b	PWM3	00000000b
SADDR	00000000b	ACC	00000000b
CHPCON	00000000b	ADCCON	xxxxx000b
SFRAL	00000000b	ADCH	xxxxxxxxb
SFRAH	00000000b	ADCCEN	xxxxxxx1b
SFRFD	11111111b	PWMCON2	00000000b
SFRCN	00111111b	PWM4	00000000b
P3	11111111b	EIE	xxx00000b
PWM5	00000000b	B	00000000b

The WDCON register reset value depends on the source of the reset.

	External reset	Watchdog reset	Power on reset
WDCON	0x0x0xx0b	0x0x01x0b	01000000b

The WTRF bit is set by a Watchdog Timer reset, and the POR bit is set by a power-on reset. A power-on reset also clears the WTRF and EWT bits, which clears the Watchdog Timer reset flag and disables the Watchdog Timer. In contrast, the Watchdog Timer reset and External reset have no effect on the EWT bit.

Reset does not affect the on-chip RAM, however, so RAM is preserved as long as V_{DD} remains above approximately 2 V, the minimum operating voltage for the RAM. If V_{DD} falls below 2 V, the RAM contents are also lost. In either case, the stack pointer is always reset, so the stack contents are lost.

10.2.3 Auto-Reload Mode, Counting Up/Down

This mode is enabled by clearing CP/$\overline{RL2}$ in T2CON and setting DCEN in T2MOD. In this mode, Timer/Counter 2 is a 16-bit up/down-counter, whose direction is controlled by the T2EX pin (1 = up, 0 = down). If Timer/Counter 2 is counting up, an overflow reloads TL2 and TH2 with the contents of the capture registers RCAP2L and RCAP2H. If Timer/Counter 2 is counting down, TL2 and TH2 are loaded with FFFFh when the contents of Timer/Counter 2 equal the capture registers RCAP2L and RCAP2H. Regardless of direction, reloading sets the TF2 bit. It also toggles the EXF2 bit, but the EXF2 bit can not generate an interrupt in this mode. This is illustrated below.

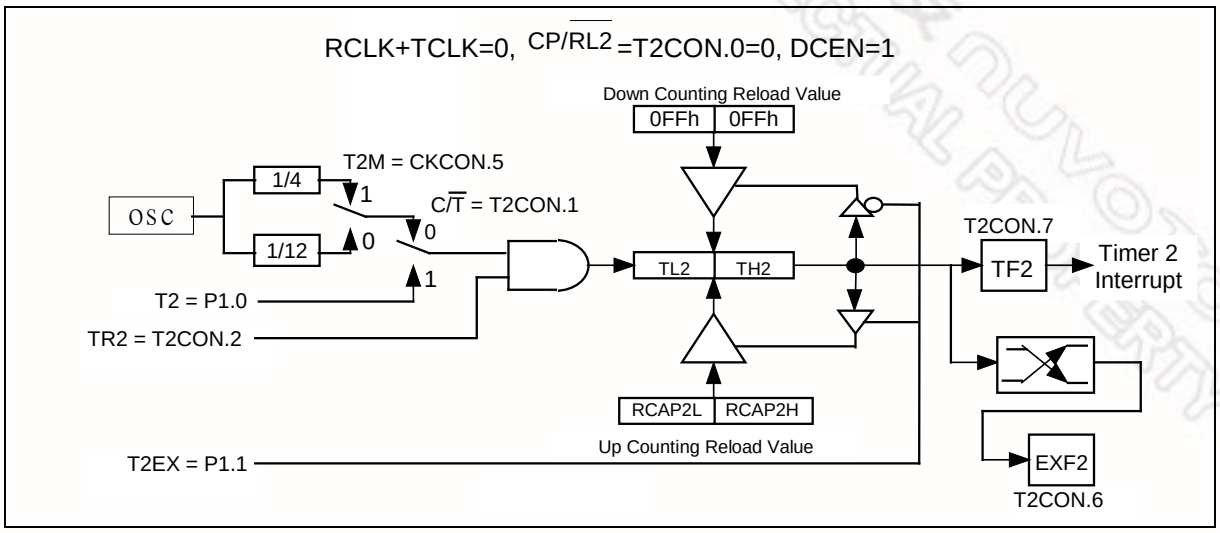

Figure 10-6 16-Bit Auto-reload Up/Down Counter

10.2.4 Baud Rate Generator Mode

Baud rate generator mode is enabled by setting either RCLK or TCLK in T2CON. In baud rate generator mode, Timer/Counter 2 is a 16-bit counter with auto-reload when the count rolls over from FFFFh. However, rolling-over does not set TF2. If EXEN2 is set, then a negative transition on the T2EX pin sets EXF2 bit in the T2CON register and causes an interrupt request.

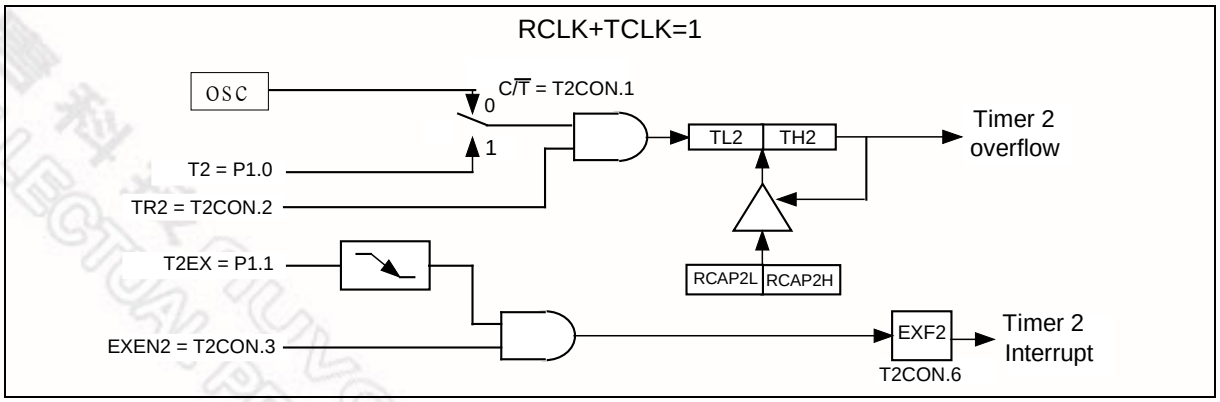

Figure 10-7 Baud Rate Generator Mode

14. ANALOG-TO-DIGITAL CONVERTER (ADC)

The ADC converts one of eight analog input channels into a 10-bit value using successive approximation control logic. The conversion process takes 50 machine cycles to complete. The functional diagram is illustrated below.

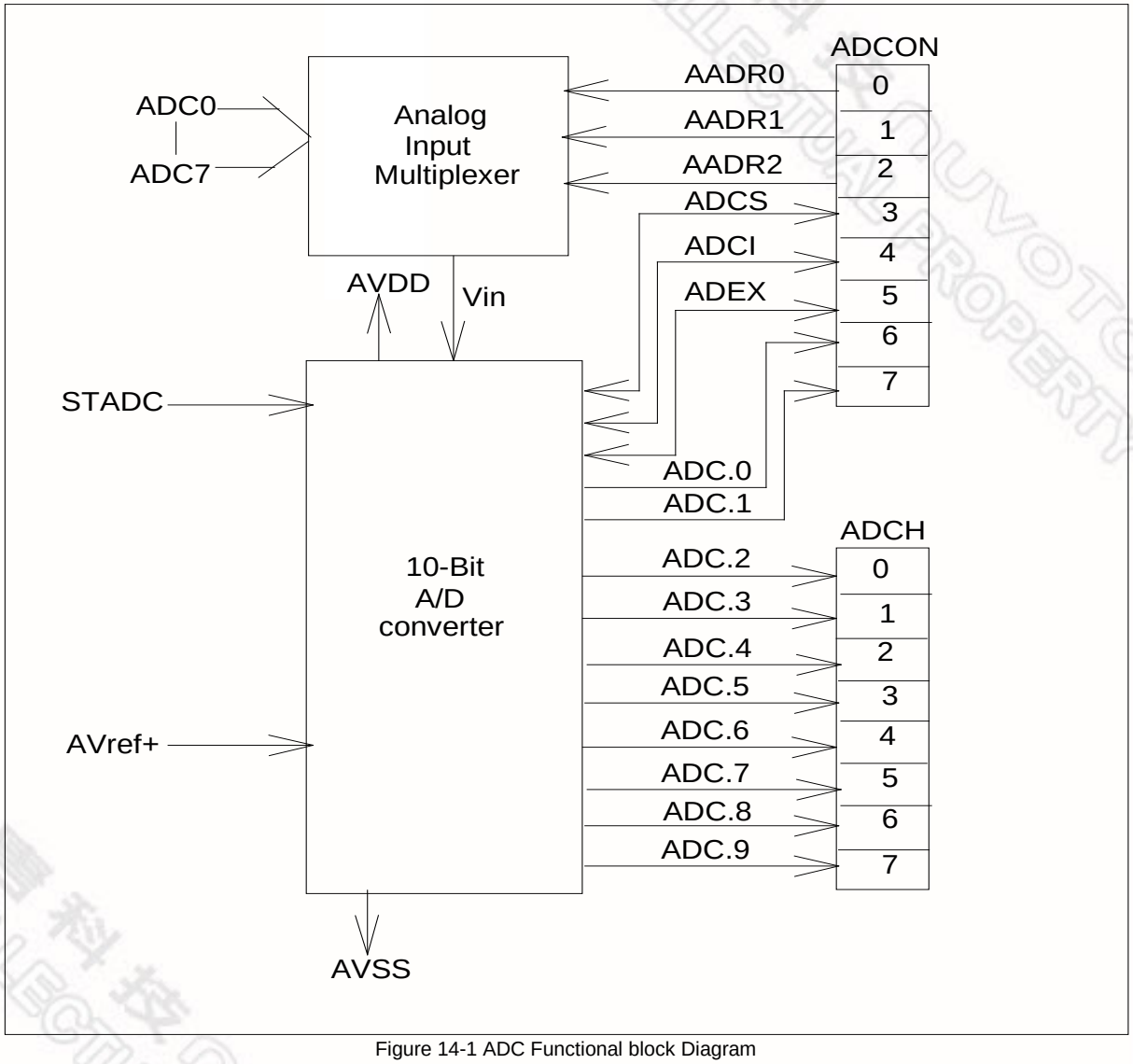

Figure 14-1 ADC Functional block Diagram

The ADC circuit is enabled by ADCCEN. Control bits ADCCON.0, ADCCON.1 and ADCCON.2 are connected to an analog multiplexer that selects one of eight analog channels to convert (Vin). A conversion is initiated by setting the ADCS bit (ADDCON.3). The ADCS bit can be set by either hardware (P2.0) or software, according to the ADEX bit (ADCCON.5). If ADEX is 0, only the software can set ADCS. If ADEX is 1, the software can set ADCS, or it can be set by applying a rising edge to external pin STADC. The rising edge must consist of a low level on STADC for at least one machine

17. IN-SYSTEM PROGRAMMING

This section explains the key steps to use in-system programming. The steps depend on whether the loader program is located in the LD Flash EPROM or AP Flash EPROM, although both processes begin while the W79E201 is running with the AP Flash EPROM.

If the loader program is located in the LD Flash EPROM, the main program should set CHPCON to 03H, and then enter idle mode. When the W79E201 wakes up, the CPU switches to the LD Flash EPROM and executes a reset. (This reset switches to LD Flash EPROM memory too.) The loader program then sets the SFRCN register to update the AP Flash EPROM, and, afterwards, it requests a software reset (CHPCON = 83H) to switch back to the AP Flash EPROM. The CPU restarts using the updated program in the AP Flash EPROM.

If the loader program is located in the AP Flash EPROM, the main program should set CHPCON to 01H, and then enter idle mode. The loader program then sets the SFRCN register to update the LD Flash EPROM, and, afterwards, the CPU continues to run the program in the AP Flash EPROM.

Please see the In-system Programming Software Examples for additional details and code examples.

19. THE PERFORMANCE CHARACTERISTIC OF ADC

The offset error is the deviation between the ideal transfer value and actual transfer value. The gain error is the difference between the slope of the ideal transfer curve and the slope of actual transfer curve. The differential non-linearity (DNL) is the difference between the actual step width and ideal step width. The ideal step width is 1 LSB. The characteristics of DNL are shown in Figure 19-1 below.

$V_{DD} - V_{SS}$ = 5V ±10%, $AV_{DD} - V_{SS}$ =5V, Vref=5V, T_A = 25°C, Fosc = 16 MHz

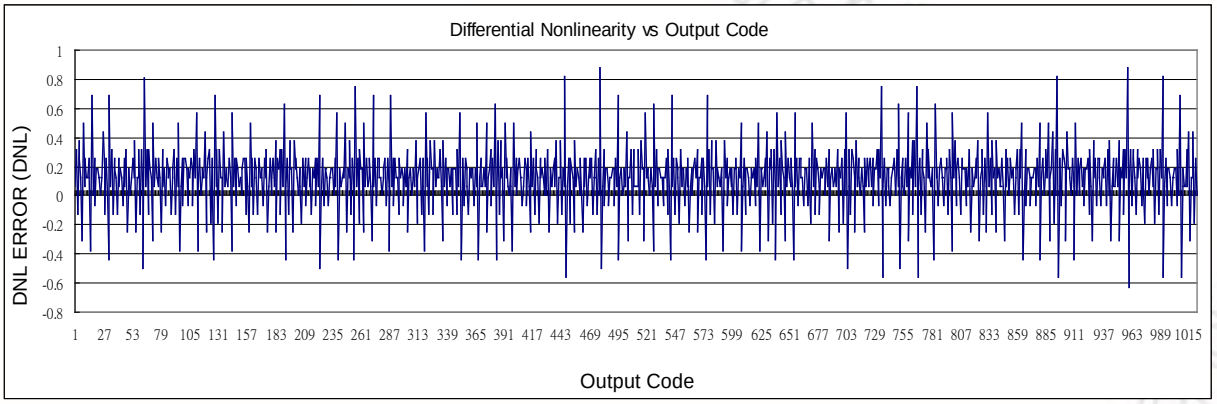

Figure 19-1 Differential Nonlinearity vs. Output Code

The integral non-linearity (INL) is the deviation of a code from the actual straight line. The deviation of each code is measured from the middle of the code. The characteristics of INL are shown in Figure 19-2 below.

$V_{DD} - V_{SS}$ = 5V ±10%, $AV_{DD} - V_{SS}$ = 5V, Vref = 5V, T_A = 25°C, Fosc = 16 MHz

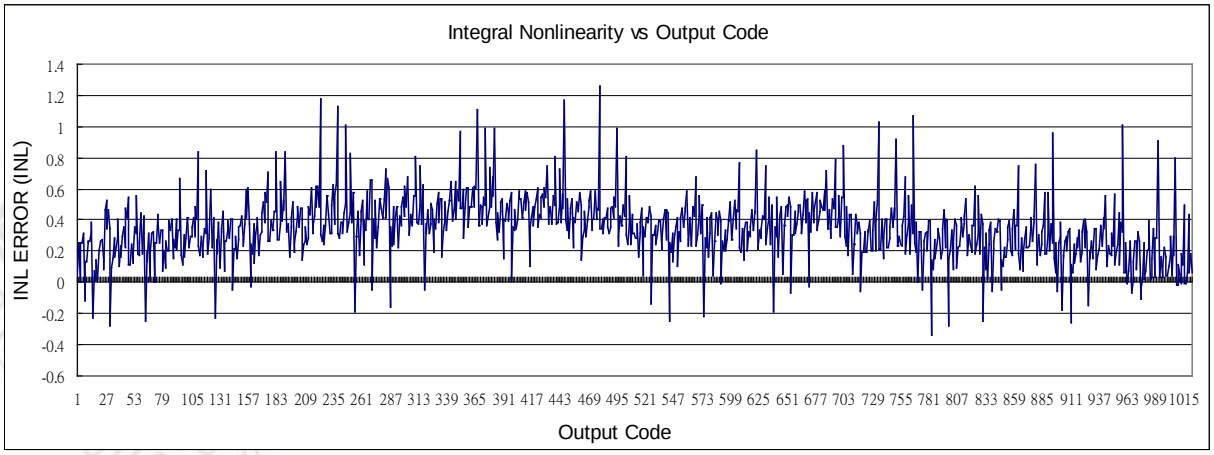

Figure 19-2 Integral Nonlinearity vs. Output Code

20. ELECTRICAL CHARACTERISTICS

20.1 Absolute Maximum Ratings

SYMBOL	PARAMETER	CONDITION	RATING	UNIT
DC Power Supply	$V_{DD} - V_{SS}$	-0.3	+7.0	V
Input Voltage	V_{IN}	V_{SS} -0.3	V_{DD} +0.3	V
Operating Temperature	T_A	0	+70	°C
Storage Temperature	Tst	-55	+150	°C

Note: Exposure to conditions beyond those listed under Absolute Maximum Ratings may adversely affect the life and reliability of the device.

20.2 DC Characteristics

($V_{DD} - V_{SS}$ = 5V ±10%, T_A = 25°C, Fosc = 16 MHz, unless otherwise specified.)

PARAMETER	SYMBOL	SPECIFICATION			TEST CONDITIONS
		MIN.	MAX.	UNIT	
Operating Voltage	V_{DD}	4.5	5.5	V	
Operating Current	I_{DD}	-	30	mA	No load V_{DD} = RST = 5.5V
Idle Current	I_{IDLE}	-	24	mA	Idle mode V_{DD} = 5.5V
Power Down Current	I_{PWDN}	-	10	µA	Power-down mode V_{DD} = 5.5V
Input Current P1, P2, P3	I_{IN1}	-70	+10	µA	V_{DD} = 5.5V V_{IN} = 0V or V_{DD}
Input Current RST[*1]	I_{IN2}	-10	+120	µA	V_{DD} = 5.5V 0<V_{IN}<V_{DD}
Input Leakage Current P0, $\overline{EA}$	I_{LK}	-10	+10	µA	V_{DD} = 5.5V 0V<V_{IN}<V_{DD}
Logic 1 to 0 Transition Current P1, P2, P3	I_{TL}[*4]	-750	-200	µA	V_{DD} = 5.5V V_{IN} = 2.0V
Input Low Voltage P0, P1, P2, P3, $\overline{EA}$	V_{IL1}	0	0.8	V	V_{DD} = 4.5V
Input Low Voltage RST[*1]	V_{IL2}	0	0.8	V	V_{DD} = 4.5V
Input Low Voltage XTAL1[*3]	VIL3	0	0.8	V	VDD = 4.5V

DC Characteristics, continued

PARAMETER	SYMBOL	SPECIFICATION			TEST CONDITIONS
		MIN.	MAX.	UNIT	
Input High Voltage P0, P1, P2, P3, $\overline{EA}$	V_{IH1}	2.4	VDD +0.2	V	VDD = 5.5V
Input High Voltage RST	V_{IH2}	3.5	VDD +0.2	V	VDD = 5.5V
Input High Voltage XTAL1[*3]	V_{IH3}	3.5	VDD +0.2	V	VDD = 5.5V
Sink current P1, P3	I_{SK1}	4	15	mA	VDD =4.5V Vs = 0.45V
Sink current P0,P2, ALE, $\overline{PSEN}$	I_{SK2}	8	15	mA	VDD =4.5V VOL = 0.45V
Source current P1, P3	I_{SR1}	-180	-360	uA	VDD =4.5V VOL = 2.4V
Source current P0, P2, ALE, $\overline{PSEN}$	I_{SR2}	-10	-14	mA	VDD =4.5V VOL = 2.4V
Output Low Voltage P1, P3	V_{OL1}	-	0.45	V	VDD = 4.5V IOL = +6 mA
Output Low Voltage P0, P2, ALE, $\overline{PSEN}$ [*2]	V_{OL2}	-	0.45	V	VDD = 4.5V IOL = +10 mA
Output High Voltage P1, P3	V_{OH1}	2.4	-	V	VDD = 4.5V IOH = -180 μA
Output High Voltage P0, P2, ALE, $\overline{PSEN}$ [*2]	V_{OH2}	2.4	-	V	VDD = 4.5V IOH = -10mA

Notes:

*1. RST pin is a Schmitt trigger input.

*2. P0, ALE and $\overline{PSEN}$ are tested in the external access mode.

*3. XTAL1 is a CMOS input.

*4. Pins of P1, P2 and P3 can source a transition current when they are being externally driven from 1 to 0. The transition current reaches its maximum value when VIN approximates to 2V.

M2	M1	M0	MOVX CYCLES	T_{MCS}
0	0	0	2 machine cycles	0
0	0	1	3 machine cycles	4 t_{CLCL}
0	1	0	4 machine cycles	8 t_{CLCL}
0	1	1	5 machine cycles	12 t_{CLCL}
1	0	0	6 machine cycles	16 t_{CLCL}
1	0	1	7 machine cycles	20 t_{CLCL}
1	1	0	8 machine cycles	24 t_{CLCL}
1	1	1	9 machine cycles	28 t_{CLCL}

Explanation of Logics Symbols

In order to maintain compatibility with the original 8051/52 family, this device specifies the same parameter for each device, using the same symbols. The explanation of the symbols is as follows.

t	Time	A	Address
C	Clock	D	Input Data
H	Logic level high	L	Logic level low
I	Instruction	P	$\overline{PSEN}$
Q	Output Data	R	$\overline{RD}$ signal
V	Valid	W	$\overline{WR}$ signal
X	No longer a valid state	Z	Tri-state

```
        MOV     DPTR,#0H        ; The start address of sample code
        MOV     R2,#00H         ; Target  low byte address
        MOV     R1,#00H         ; Target  high byte address
        MOV     SFRAH,R1        ; SFRAH, Target high address
        MOV     SFRCN,#00H      ; SFRCN = 00H, Read AP Flash EPROM
READ_VERIFY_16K:
        MOV      SFRAL,R2       ; SFRAL = LOW ADDRESS
        MOV     TCON,#10H       ; TCON = 10H, TR0 = 1,GO
        MOV     PCON,#01H
        INC     R2
        MOVX     A,@DPTR
        INC     DPTR
        CJNE    A,SFRFD,ERROR_16K
        CJNE    R2,#00H,READ_VERIFY_16K
        INC     R1
        MOV     SFRAH,R1
        CJNE    R1,#40H,READ_VERIFY_16K
;*****************************************************************************
;* PROGRAMMING COMPLETLY, SOFTWARE RESET CPU
;*****************************************************************************
        MOV     TA,#AAH
        MOV     TA,#55H
        MOV     CHPCON,#83H             ; SOFTWARE RESET. CPU will restart from AP Flash EPROM
ERROR_16K:
        DJNZ    R4,UPDATE_16K           ; IF ERROR OCCURS, REPEAT 3 TIMES.
                                        ; IN-SYST PROGRAMMING FAIL, USER'S PROCESS TO DEAL
                                          WITH IT.
                .
                .
                .
```