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Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Obsolete
Core Processor	ARM® Cortex®-M0
Core Size	32-Bit Single-Core
Speed	50MHz
Connectivity	EBI/EMI, I ² C, IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	40
Program Memory Size	8KB (8K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	2.5V ~ 5.5V
Data Converters	A/D 8x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/nuvoton-technology-corporation-america/m052lbn



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- Up to two sets of UART device
- Programmable baud-rate generator
- Buffered receiver and transmitter, each with 15 bytes FIFO
- Optional flow control function (CTS and RTS)
- Supports IrDA(SIR) function
- Supports RS485 function
- Supports LIN function
- SPI
 - Up to two sets of SPI device.
 - Supports master/slave mode
 - Full duplex synchronous serial data transfer
 - Provide 3 wire function
 - Variable length of transfer data from 1 to 32 bits
 - MSB or LSB first data transfer
 - Rx latching data can be either at rising edge or at falling edge of serial clock
 - Tx sending data can be either at rising edge or at falling edge of serial clock
 - Supports Byte suspend mode in 32-bit transmission
- I²C
 - Supports master/slave mode
 - Bidirectional data transfer between masters and slaves
 - Multi-master bus (no central master).
 - Arbitration between simultaneously transmitting masters without corruption of serial data on the bus
 - Serial clock synchronization allows devices with different bit rates to communicate via one serial bus.



Pin number		Symbol	Alternate Function			Type ^[1]	Description
QFN33	LQFP48		1	2	3		
NC	28	P4.4	$\overline{\text{CS}}$			I/O	The ICE_CLK/ICE_DAT pins are for JTAG-ICE function used.
NC	29	P4.5	ALE			I/O	PWM0-3 can be used from P4.0-P4.3 when EBI is active.
19	30	P4.6	ICE_CLK			I/O	The T2EX/T3EX pins are for external capture/reset trigger input of Timer2/3.
20	31	P4.7	ICE_DAT			I/O	

Table 5-1 NuMicro™ M051 Series Pin Description

[1] I/O type description. I: input, O: output, I/O: quasi bi-direction, D: open-drain, P: power pins, ST: Schmitt trigger.

[2] The pins features which are set by S/W. Only one-set pin can be used while S/W to set it.



- Load/store-multiples and multicycle-multiplies that can be abandoned and restarted to facilitate rapid interrupt handling.
- C Application Binary Interface compliant exception model.
This is the ARMv6-M, C Application Binary Interface(C-ABI) compliant exception model that enables the use of pure C functions as interrupt handlers.
- Low power sleep-mode entry using Wait For Interrupt (WFI), Wait For Event(WFE) instructions, or the return from interrupt sleep-on-exit feature.

NVIC features:

- 32 external interrupt inputs, each with four levels of priority.
- Dedicated non-Maskable Interrupt (NMI) input.
- Support for both level-sensitive and pulse-sensitive interrupt lines
- Wake-up Interrupt Controller (WIC), supports ultra-low power sleep mode.

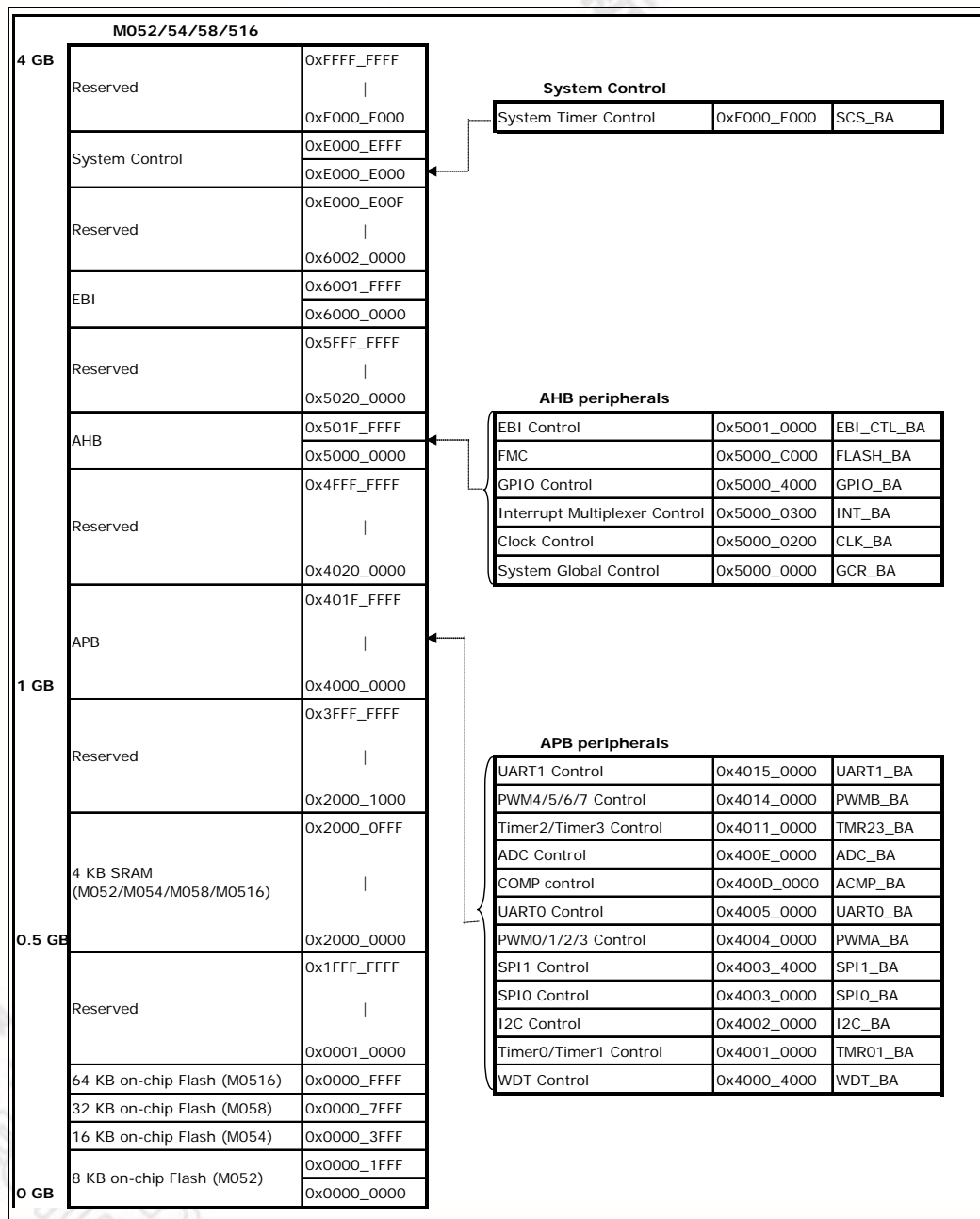
Debug support:

- Four hardware breakpoints.
- Two watchpoints.
- Program Counter Sampling Register (PCSR) for non-intrusive code profiling.
- Single step and vector catch capabilities.

Bus interfaces:

- Single 32-bit AMBA-3 AHB-Lite system interface that provides simple integration to all system peripherals and memory.
- Single 32-bit slave port that supports the DAP (Debug Access Port).

6.2.5 Whole System Memory Mapping Table



6.2.6 System Timer (SysTick)

The Cortex-M0 includes an integrated system timer, SysTick. SysTick provides a simple, 24-bit

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Revision V1.01

6.3.3 System Clock & SysTick Clock

The system clock has 4 clock sources which were generated from clock generator block. The clock source switch depends on the register HCLK_S(CLKSEL0[2:0]). The block diagram is shown in the Figure 6-4.

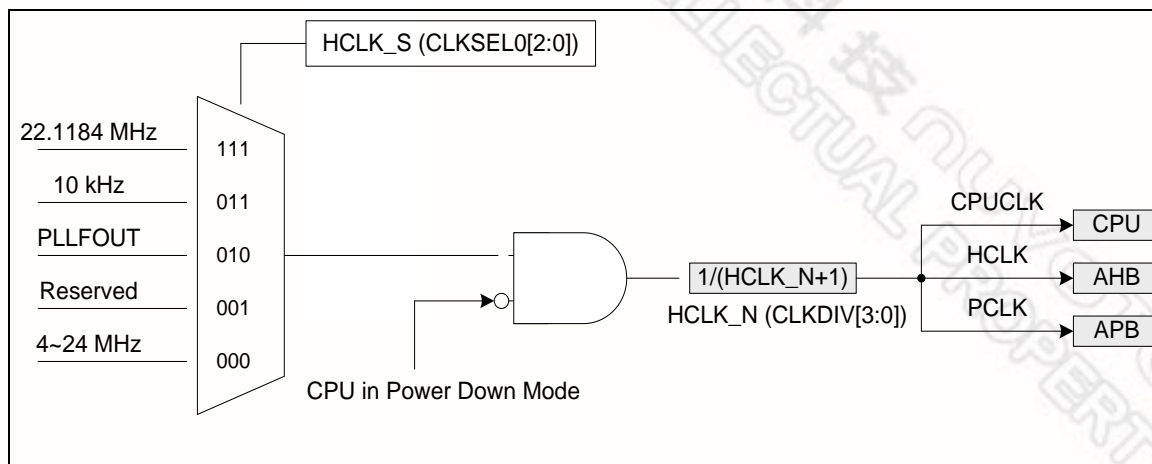


Figure 6-4 System Clock Block Diagram

The clock source of SysTick in Cortex-M0 core can use CPU clock or external clock (SYST_CSR[2]). If using external clock, the SysTick clock (STCLK) has 4 clock sources. The clock source switch depends on the setting of the register STCLK_S (CLKSEL0[5:3]). The block diagram is shown in the Figure 6-5.

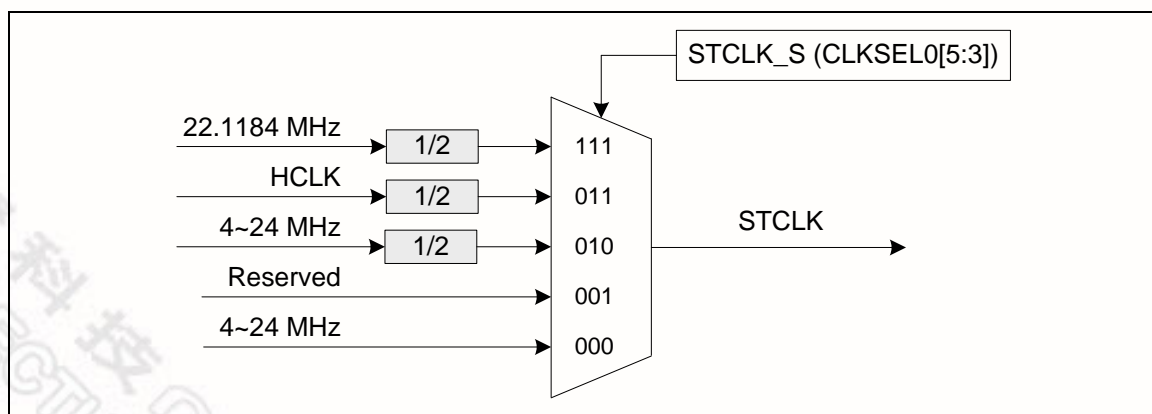


Figure 6-5 SysTick clock Control Block Diagram

6.3.4 AHB Clock Source Select

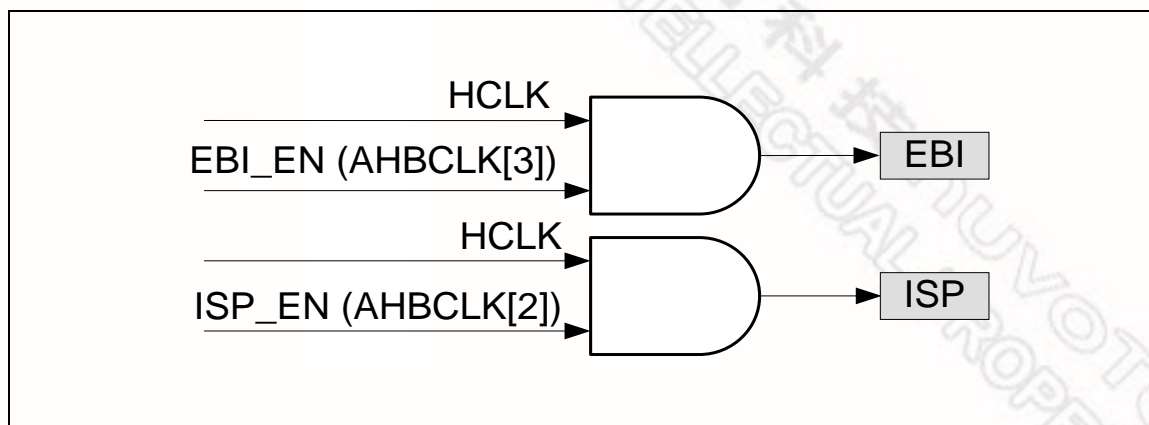


Figure 6-6 AHB Clock Source for HCLK

6.3.5 Peripherals Clock Source Select

The peripherals clock had different clock source switch setting which depends on the different peripheral.

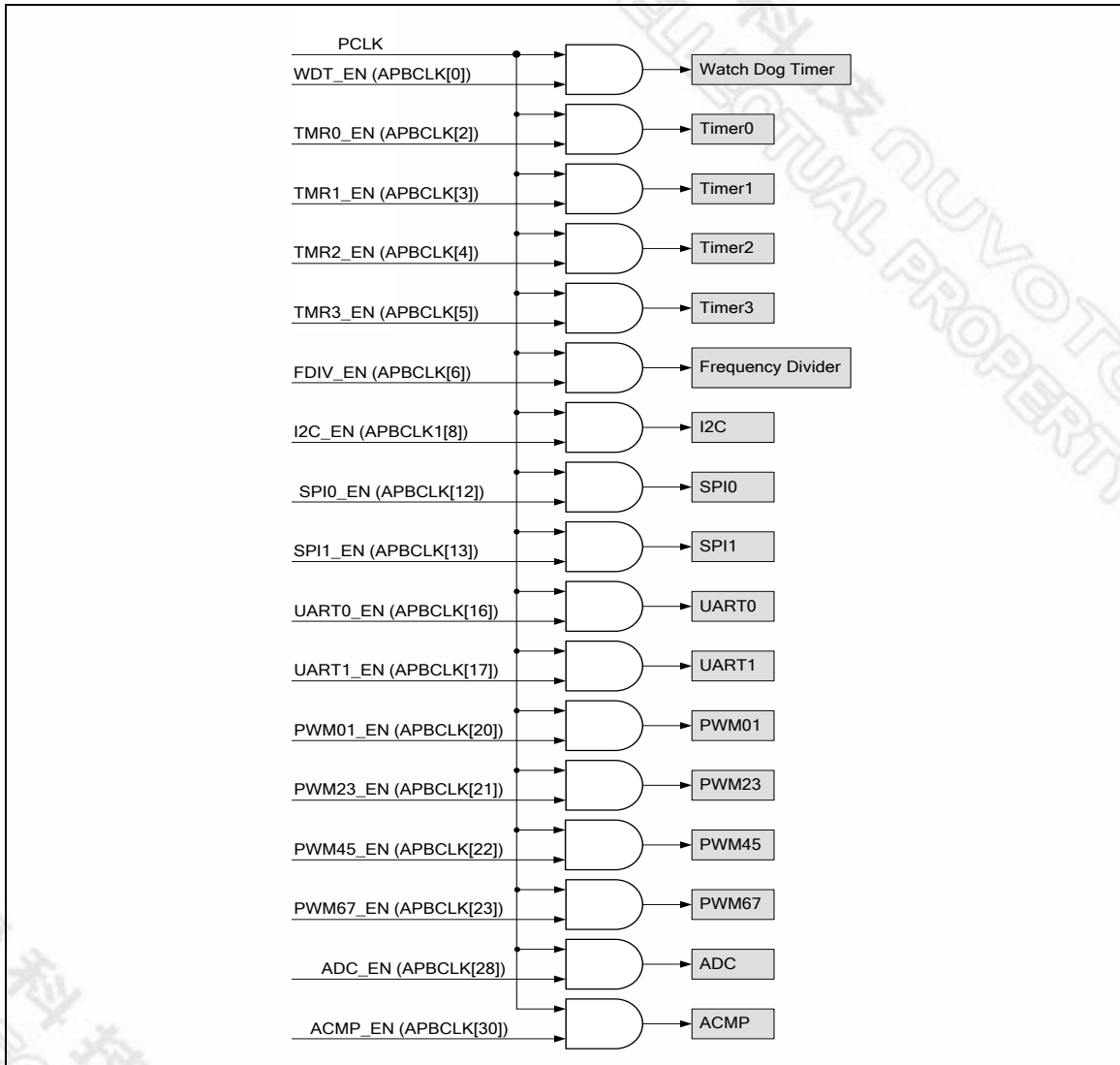


Figure 6-7 Peripherals Clock Source Select for PCLK

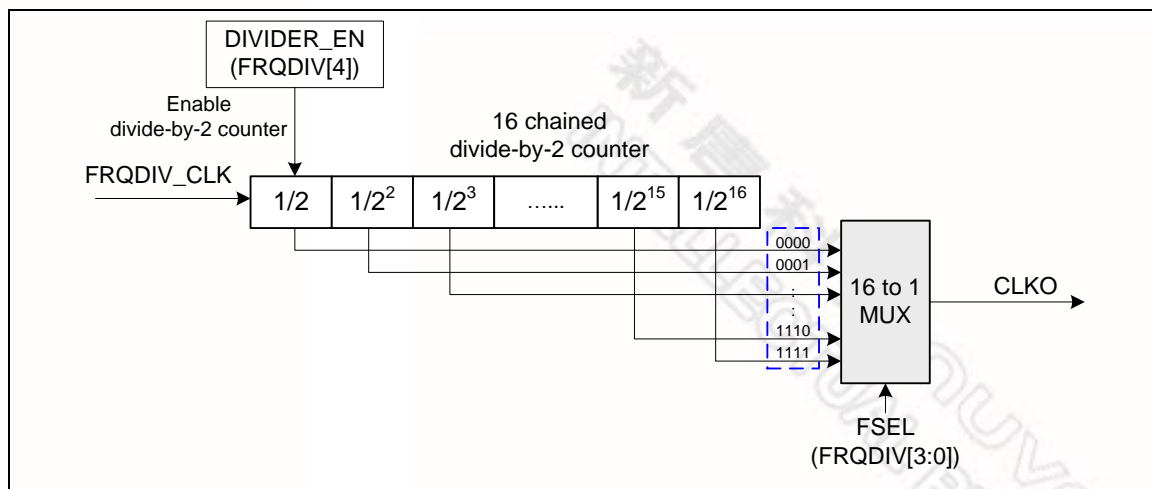


Figure 6-9 Block Diagram of Frequency Divider



6.6 PWM Generator and Capture Timer

6.6.1 Overview

NuMicro M051™ series has 2 sets of PWM group supports 4 sets of PWM Generators which can be configured as 8 independent PWM outputs, PWM0~PWM7, or as 4 complementary PWM pairs, (PWM0, PWM1), (PWM2, PWM3), (PWM4, PWM5) and (PWM6, PWM7) with 4 programmable dead-zone generators.

Each PWM Generator has one 8-bit prescaler, one clock divider with 5 divided frequencies (1, 1/2, 1/4, 1/8, 1/16), two PWM Timers including two clock selectors, two 16-bit PWM down-counters for PWM period control, two 16-bit comparators for PWM duty control and one dead-zone generator. The 4 sets of PWM Generators provide eight independent PWM interrupt flags which are set by hardware when the corresponding PWM period down counter reaches zero. Each PWM interrupt source with its corresponding enable bit can cause CPU to request PWM interrupt. The PWM generators can be configured as one-shot mode to produce only one PWM cycle signal or auto-reload mode to output PWM waveform continuously.

When PCR.DZEN01 is set, PWM0 and PWM1 perform complementary PWM paired function; the paired PWM timing, period, duty and dead-time are determined by PWM0 timer and Dead-zone generator 0. Similarly, the complementary PWM pairs of (PWM2, PWM3), (PWM4, PWM5) and (PWM6, PWM7) are controlled by PWM2, PWM4 and PWM6 timers and Dead-zone generator 2, 4 and 6, respectively. Refer to figures bellowed for the architecture of PWM Timers.

When the 16-bit period down counter reaches zero, the interrupt request is generated. If PWM-timer is set as auto-reload mode, when the down counter reaches zero, it is reloaded with PWM Counter Register (CNRx) automatically then start decreasing, repeatedly. If the PWM-timer is set as one-shot mode, the down counter will stop and generate one interrupt request when it reaches zero.

The value of PWM counter comparator is used for pulse high width modulation. The counter control logic changes the output to high level when down-counter value matches the value of compare register.

The alternate feature of the PWM-timer is digital input Capture function. If Capture function is enabled the PWM output pin is switched as capture input mode. The Capture0 and PWM0 share one timer which is included in PWM 0; and the Capture1 and PWM1 share PWM1 timer, and etc. Therefore user must setup the PWM-timer before enable Capture feature. After capture feature is enabled, the capture always latched PWM-counter to Capture Rising Latch Register (CRLR) when input channel has a rising transition and latched PWM-counter to Capture Falling Latch Register (CFLR) when input channel has a falling transition. Capture channel 0 interrupt is programmable by setting CCR0.CRL_IE0[1] (Rising latch Interrupt enable) and CCR0.CFL_IE0[2] (Falling latch Interrupt enable) to decide the condition of interrupt occur. Capture channel 1 has the same feature by setting CCR0.CRL_IE1[17] and CCR0.CFL_IE1[18]. And capture channel 0 to channel 3 on each group have the same feature by setting the corresponding control bits in CCR0 and CCR2. For each group, whenever Capture issues Interrupt 0/1/2/3, the PWM counter 0/1/2/3 will be reload at this moment.

The maximum captured frequency that PWM can capture is confined by the capture interrupt latency. When capture interrupt occurred, software will do at least three steps, they are: Read

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Revision V1.01



6.9 Watchdog Timer (WDT)

6.9.1 Overview

The purpose of Watchdog Timer is to perform a system reset when system runs into an unknown state. This prevents system from hanging for an infinite period of time. Besides, this Watchdog Timer supports another function to wakeup chip from power down mode. The watchdog timer includes an 18-bit free running counter with programmable time-out intervals. Table 6-2 show the watchdog timeout interval selection and Figure 6.9-1 shows the timing of watchdog interrupt signal and reset signal.

Setting WTE (WDTCR [7]) enables the watchdog timer and the WDT counter starts counting up. When the counter reaches the selected time-out interval, Watchdog timer interrupt flag WTIF will be set immediately to request a WDT interrupt if the watchdog timer interrupt enable bit WTIE is set, in the meanwhile, a specified delay time ($1024 * T_{WDT}$) follows the time-out event. User must set WTR (WDTCR [0]) (Watchdog timer reset) high to reset the 18-bit WDT counter to avoid chip from Watchdog timer reset before the delay time expires. WTR bit is cleared automatically by hardware after WDT counter is reset. There are eight time-out intervals with specific delay time which are selected by Watchdog timer interval select bits WTIS (WDTCR [10:8]). If the WDT counter has not been cleared after the specific delay time expires, the watchdog timer will set Watchdog Timer Reset Flag (WTRF) high and reset chip. This reset will last 63 WDT clocks (T_{RST}) then chip restarts executing program from reset vector (0x0000 0000). WTRF will not be cleared by Watchdog reset. User may poll WTRF by software to recognize the reset source. WDT also provides wakeup function. When chip is powered down and the Watchdog Timer Wake-up Function Enable bit (WDTR[4]) is set, if the WDT counter reaches the specific time interval defined by WTIS (WDTCR [10:8]), the chip is waken up from power down state. First example, if WTIS is set as 000, the specific time interval for chip to wake up from power down state is $2^4 * T_{WDT}$. When power down command is set by software, then, chip enters power down state. After $2^4 * T_{WDT}$ time is elapsed, chip is waken up from power down state. Second example, if WTIS (WDTCR [10:8]) is set as 111, the specific time interval for chip to wake up from power down state is $2^{18} * T_{WDT}$. If power down command is set by software, then, chip enters power down state. After $2^{18} * T_{WDT}$ time is elapsed, chip is waken up from power down state. Notice if WTRE (WDTCR [1]) is set to 1, after chip is waken up, software should chip the Watchdog Timer counter by setting WTR(WDTCR [0]) to 1 as soon as possible. Otherwise, if the Watchdog Timer counter is not cleared by setting WTR (WDTCR [0]) to 1 before time starting from waking up to software clearing Watchdog Timer counter is over $1024 * T_{WDT}$, the chip is reset by Watchdog Timer.

WTIS	Timeout Interval Selection T_{TIS}	Interrupt Period T_{INT}	WTR Timeout Interval (WDT_CLK=10 kHz) MIN. T_{WTR} ~ MAX. T_{WTR}
000	$2^4 * T_{WDT}$	$1024 * T_{WDT}$	1.6 ms ~ 104 ms
001	$2^6 * T_{WDT}$	$1024 * T_{WDT}$	6.4 ms ~ 108.8 ms
010	$2^8 * T_{WDT}$	$1024 * T_{WDT}$	25.6 ms ~ 128 ms
011	$2^{10} * T_{WDT}$	$1024 * T_{WDT}$	102.4 ms ~ 204.8 ms
100	$2^{12} * T_{WDT}$	$1024 * T_{WDT}$	409.6 ms ~ 512 ms
101	$2^{14} * T_{WDT}$	$1024 * T_{WDT}$	1.6384 s ~ 1.7408 s

6.10 UART Interface Controller (UART)

NuMicro M051™ series provides two channels of Universal Asynchronous Receiver/Transmitters (UART). UART0~1 performs Normal Speed UART, and support flow control function.

6.10.1 Overview

The Universal Asynchronous Receiver/Transmitter (UART) performs a serial-to-parallel conversion on data received from the peripheral, and a parallel-to-serial conversion on data transmitted from the CPU. The UART controller also supports IrDA SIR Function, LIN master/slave mode function and RS-485 mode functions. Each UART channel supports seven types of interrupts including transmitter FIFO empty interrupt (INT_THRE), receiver threshold level reaching interrupt (INT_RDA), line status interrupt (parity error or framing error or break interrupt) (INT_RLS), receiver buffer time out interrupt (INT_TOUT), MODEM/Wakeup status interrupt (INT_MODEM), Buffer error interrupt (INT_BUF_ERR) and LIN receiver break field detected interrupt (INT_LIN_RX_BREAK).

The UART0 and UART1 are built-in with a 16-byte transmitter FIFO (TX_FIFO) and a 16-byte receiver FIFO (RX_FIFO) that reduces the number of interrupts presented to the CPU. The CPU can read the status of the UART at any time during the operation. The reported status information includes the type and condition of the transfer operations being performed by the UART, as well as 3 error conditions (parity error, framing error, break interrupt) probably occur while receiving data. The UART includes a programmable baud rate generator that is capable of dividing clock input by divisors to produce the serial clock that transmitter and receiver need. The baud rate equation is $\text{Baud Rate} = \text{UART_CLK} / M * [\text{BRD} + 2]$, where M and BRD are defined in Baud Rate Divider Register (UA_BAUD). Table 6-3 lists the equations in the various conditions and Table 6-4 list the UART baud rate setting table.

Mode	DIV_X_EN	DIV_X_ONE	Divider X	BRD	M	Baud rate equation
0	0	0	B	A	16	$\text{UART_CLK} / [16 * (A+2)]$
1	1	0	B	A	B+1	$\text{UART_CLK} / [(B+1) * (A+2)]$, B must ≥ 8
2	1	1	Don't care	A	1	$\text{UART_CLK} / (A+2)$, A must ≥ 3

Table 6-3 UART Baud Rate Equation



- Channel 7 supports 3 input sources: external analog voltage, internal bandgap voltage, and internal temperature sensor output.

6.12 External Bus Interface (EBI)

6.12.1 Overview

NuMicro M051™ series equips an external bus interface (EBI) for external device used.

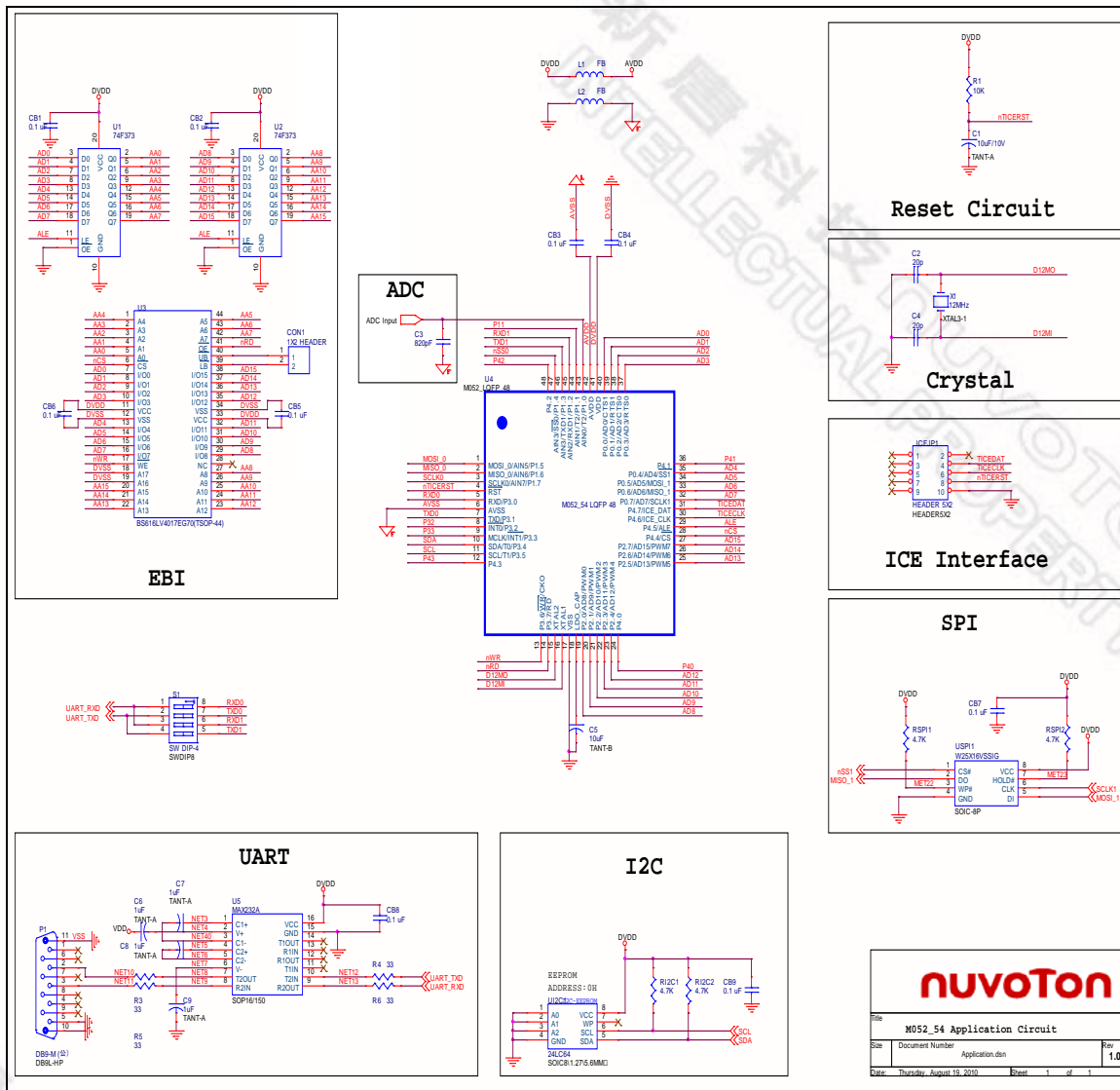
To save the connections between external device and this chip, EBI support address bus and data bus multiplex mode. And, address latch enable (ALE) signal supported differentiate the address and data cycle.

6.12.2 Features

External Bus Interface has the following functions:

1. External devices with max. 64K-byte size (8 bit data width)/128K-byte (16 bit data width) supported
2. Variable external bus base clock (MCLK) supported
3. 8 bit or 16 bit data width supported
4. Variable data access time (tACC), address latch enable time (tALE) and address hold time (tAHD) supported
5. Address bus and data bus multiplex mode supported to save the address pins
6. Configurable idle cycle supported for different access condition: Write command finish (W2X), Read-to-Read (R2R)

7 TYPICAL APPLICATION CIRCUIT



8.3.3 Typical Crystal Application Circuits

CRYSTAL	C1	C2
4 MHz ~ 24 MHz	Optional (Depend on crystal specification)	

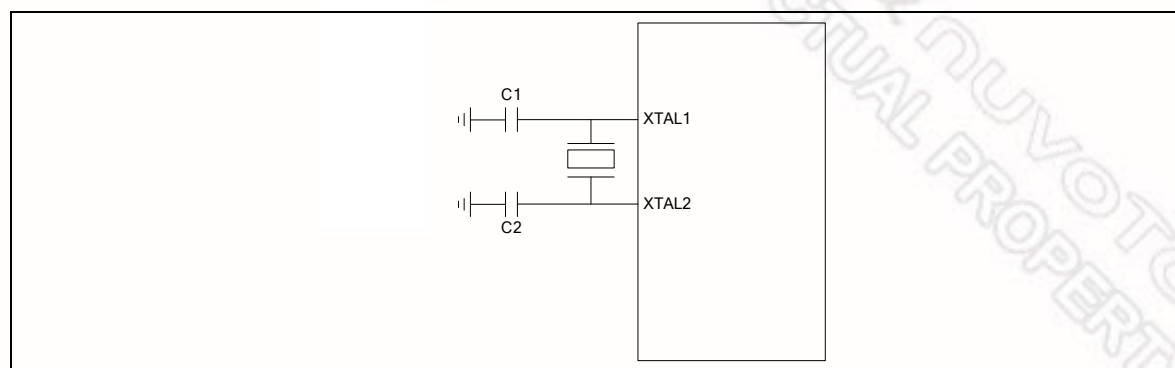


Figure 8-1 Typical Crystal Application Circuit

8.4.2 Specification of LDO & Power management

PARAMETER	MIN	TYP	MAX	UNIT	NOTE
Input Voltage	2.5	5	5.5	V	V _{DD} input voltage
Output Voltage	-10%	1.8	+10%	V	LDO output voltage
Temperature	-40	25	85	°C	
C	-	1u	-	F	Resr=1ohm

Note:

1. It is recommended a 100nF bypass capacitor is connected between V_{DD} and the closest V_{SS} pin of the device.
2. For ensuring power stability, a 1uF or higher capacitor must be connected between LDO pin and the closest V_{SS} pin of the device.

8.4.3 Specification of Low Voltage Reset

PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
Operation voltage	-	2.5	5	5.5	V
Temperature	-	-40	25	85	°C
Quiescent current	V _{DD} =5.5V	-	-	5	uA
Threshold voltage	Temperature=25°	1.7	2.0	2.3	V
	Temperature=-40°	-	2.3	-	V
	Temperature=85°	-	1.8	-	V
Hysteresis	-	0	0	0	V

8.4.4 Specification of Brown-Out Detector

Parameter	Condition	Min.	Typ.	Max.	Unit
Operation voltage	-	2.5	-	5.5	V
Quiescent current	AV _{DD} =5.5V	-	-	140	μA
Temperature	-	-40	25	85	°C
Brown-Out voltage	BOV_VL[1:0]=11	4.1	4.3	4.5	V
	BOV_VL [1:0]=10	3.5	3.7	3.9	V
	BOV_VL [1:0]=01	2.5	2.7	2.9	V
	BOV_VL [1:0]=00	2.0	2.2	2.4	V
Hysteresis	-	30m	-	150m	V

8.4.5 Specification of Power-On Reset (5V)

Parameter	Condition	Min.	Typ.	Max.	Unit
Temperature	-	-40	25	85	°C
Reset voltage	V+	-	2	-	V

9.2 QFN-33 (5X5 mm², Thickness 0.8mm, Pitch 0.5 mm)

