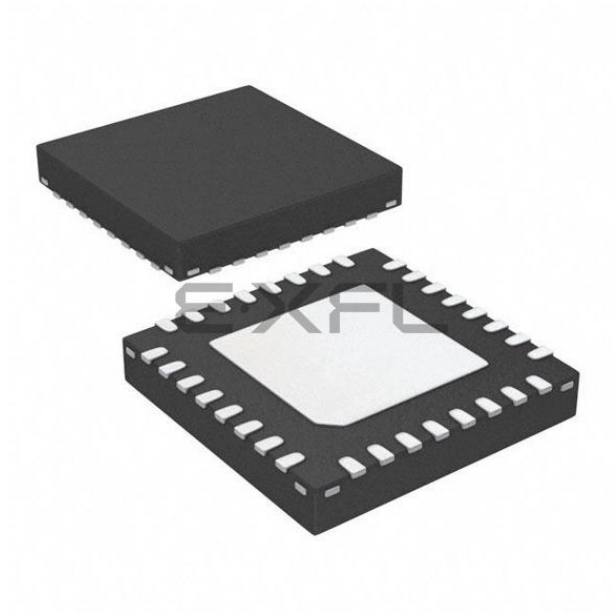

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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Obsolete |
| Core Processor | ARM® Cortex®-M0 |
| Core Size | 32-Bit Single-Core |
| Speed | 50MHz |
| Connectivity | I²C, IrDA, SPI, UART/USART |
| Peripherals | Brown-out Detect/Reset, LVD, POR, PWM, WDT |
| Number of I/O | 24 |
| Program Memory Size | 8KB (8K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 4K x 8 |
| Voltage - Supply (Vcc/Vdd) | 2.5V ~ 5.5V |
| Data Converters | A/D 5x12b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 32-WFQFN Exposed Pad |
| Supplier Device Package | - |
| Purchase URL | https://www.e-xfl.com/product-detail/nuvoton-technology-corporation-america/m052zan |

# 1 GENERAL DESCRIPTION

The NuMicro M051™ series is a 32-bit microcontroller with embedded ARM® Cortex™-M0 core for industrial control and applications which need rich communication interfaces. The Cortex™-M0 is the newest ARM embedded processor with 32-bit performance and at a cost equivalent to traditional 8-bit microcontroller. The NuMicro M051™ series includes M052, M054, M058 and M0516 families.

The M052/M054 can run up to 50 MHz. Thus it can afford to support a variety of industrial control and applications which need high CPU performance. The M052/M054 has 8K/16K-byte embedded flash, 4K-byte data flash, 4K-byte flash for the ISP, and 4K-byte embedded SRAM.

Many system level peripheral functions, such as I/O Port, EBI (External Bus Interface), Timer, UART, SPI, I2C, PWM, ADC, Watchdog Timer and Brownout Detector, have been incorporated into the M052/M054 in order to reduce component count, board space and system cost. These useful functions make the M052/M054 powerful for a wide range of applications.

Additionally, the M052/M054 is equipped with ISP (In-System Programming) and ICP (In-Circuit Programming) functions, which allow the user to update the program memory without removing the chip from the actual end product.

- Open-Drain output
- Input only with high impendence

- TTL/Schmitt trigger input selectable
- I/O pin can be configured as interrupt source with edge/level setting
- Supports high driver and high sink IO mode

- Timer
  - Provides four channel 32-bit timers, one 8-bit pre-scale counter with 24-bit up-timer for each timer.
  - Independent clock source for each timer.
  - 24-bit timer value is readable through TDR (Timer Data Register)
  - Provides one-shot, periodic and toggle operation modes.
  - Provide event counter function.
  - Provide external capture/reset counter function equivalent to 8051 Timer2.
- Watchdog Timer
  - Multiple clock sources
  - Supports wake up from power down or sleep mode
  - Interrupt or reset selectable on watchdog time-out
- PWM
  - Built-in up to four 16-bit PWM generators; providing eight PWM outputs or four complementary paired PWM outputs
  - Individual clock source, clock divider, 8-bit pre-scalar and dead-zone generator for each PWM generator
  - PWM interrupt synchronized to PWM period
  - 16-bit digital Capture timers (shared with PWM timers) with rising/falling capture inputs
  - Supports capture interrupt
- UART

- Up to two sets of UART device
- Programmable baud-rate generator
- Buffered receiver and transmitter, each with 15 bytes FIFO
- Optional flow control function (CTS and RTS)
- Supports IrDA(SIR) function
- Supports RS485 function
- Supports LIN function

- SPI
  - Up to two sets of SPI device.
  - Supports master/slave mode
  - Full duplex synchronous serial data transfer
  - Provide 3 wire function
  - Variable length of transfer data from 1 to 32 bits
  - MSB or LSB first data transfer
  - Rx latching data can be either at rising edge or at falling edge of serial clock
  - Tx sending data can be either at rising edge or at falling edge of serial clock
  - Supports Byte suspend mode in 32-bit transmission
- $I^2C$
  - Supports master/slave mode
  - Bidirectional data transfer between masters and slaves
  - Multi-master bus (no central master).
  - Arbitration between simultaneously transmitting masters without corruption of serial data on the bus
  - Serial clock synchronization allows devices with different bit rates to communicate via one serial bus.

- Serial clock synchronization can be used as a handshake mechanism to suspend and resume serial transfer.
- Programmable clocks allow versatile rate control.
- Supports multiple address recognition (four slave address with mask option)

- ADC
  - 12-bit SAR ADC with 760k SPS
  - Up to 8-ch single-ended input or 4-ch differential input
  - Supports single mode/burst mode/single-cycle scan mode/continuous scan mode
  - Supports 2' complement/un-signed format in differential mode conversion result
  - Each channel with an individual result register
  - Supports conversion value monitoring (or comparison) for threshold voltage detection
  - Conversion can be started either by software trigger or external pin trigger
- Analog Comparator
  - Up to 2 comparator analog modules
  - External input or internal band gap voltage selectable at negative node
  - Interrupt when compare result change
  - Power down wake up
- EBI (External Bus Interface) for external memory-mapped device access
  - Accessible space: 64KB in 8-bit mode or 128KB in 16-bit mode
  - Supports 8-bit/16-bit data width
  - Supports byte-write in 16-bit data width
- In-System Programming (ISP) and In-Circuit Programming (ICP)
- One built-in temperature sensor with 1℃ resolution
- Brown-Out Detector
  - With 4 levels: 4.3V/3.7V/2.7V/2.2V

- Supports Brown-Out interrupt and reset option

- 96-bit unique ID
- LVR (Low Voltage Reset)
  - Threshold voltage levels: 2.0V
- Operating Temperature: -40℃~85℃
- Packages:
  - Green package (RoHS)
  - 48-pin LQFP, 33-pin QFN

# 3 BLOCK DIAGRAM

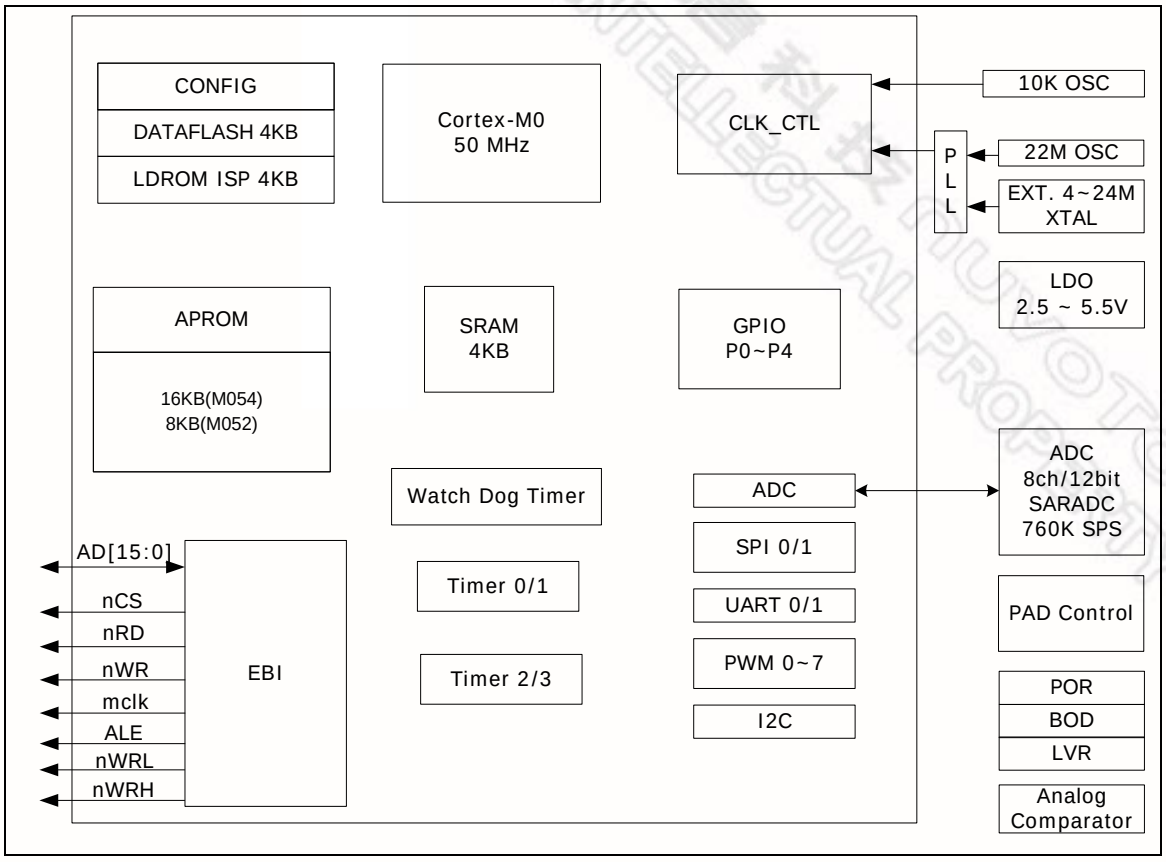



Figure 3-1 NuMicro™ M051 Series Block Diagram

## 5.2 LQFP 48 pin

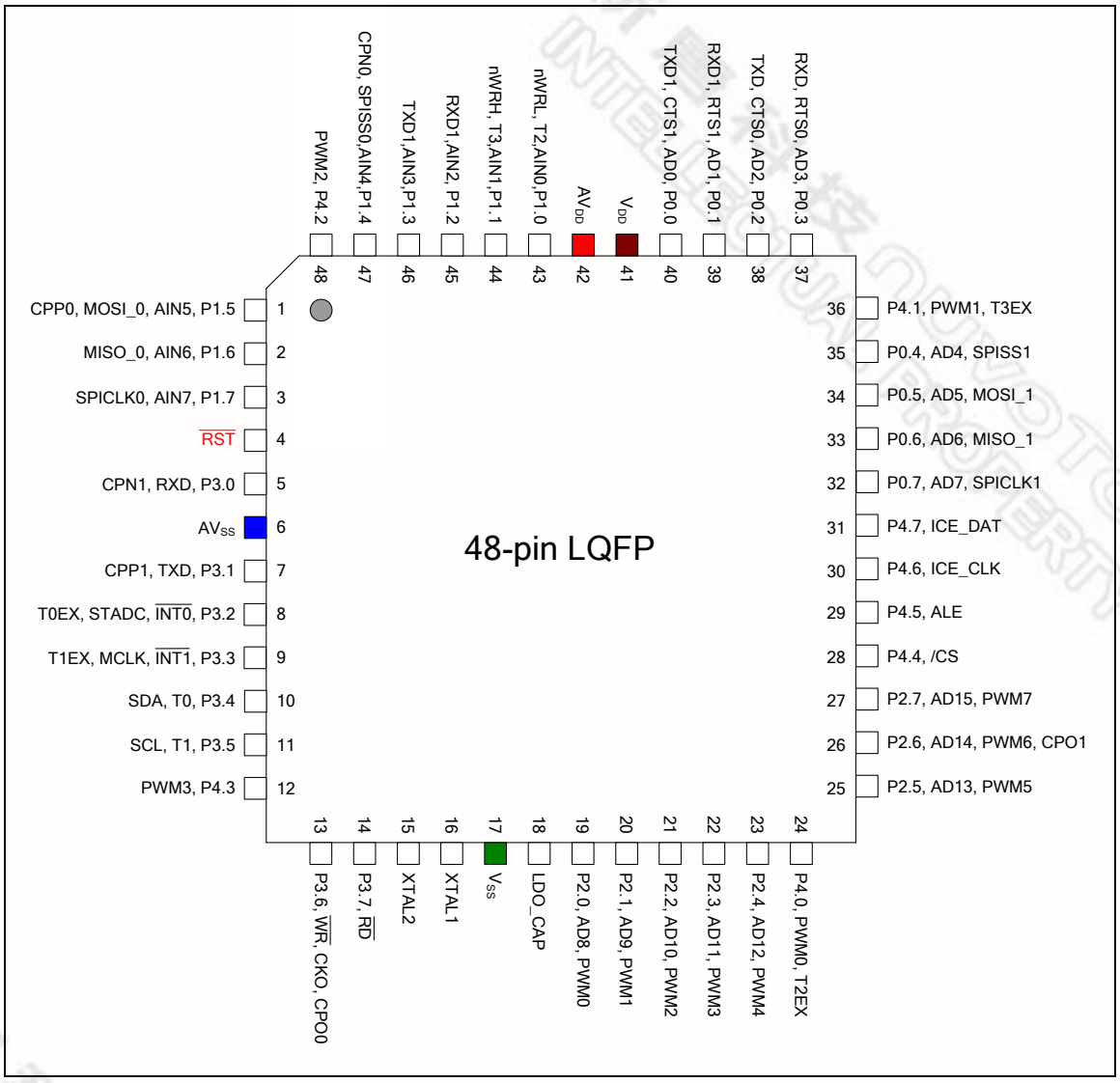



Figure 5-2 NuMicro™ M051 Series LQFP-48 Pin Diagram

## 5.3 Pin Description

| Pin number | | Symbol | Alternate Function | | | Type[1] | Description |
|---|---|---|---|---|---|---|---|
| QFN33 | LQFP48 | | 1 | 2 | 3 | | |
| 11 | 16 | XTAL1 | | | | I (ST) | **CRYSTAL1:** This is the input pin to the internal inverting amplifier. The system clock is from external crystal or resonator when FOSC[1:0] (CONFIG3[1:0]) are both logic 1 by default. |
| 10 | 15 | XTAL2 | | | | O | **CRYSTAL2:** This is the output pin from the internal inverting amplifier. It emits the inverted signal of XTAL1. |
| 27 | 41 | $V_{DD}$ | | | | P | **POWER SUPPLY:** Power supply to I/O ports and LDO source for internal PLL and digital circuit. |
| 12 | 17 | $V_{SS}$ | | | | P | **GROUND: Digital** Ground potential. |
| 33 | | | | | | | |
| 28 | 42 | $AV_{DD}$ | | | | P | **POWER SUPPLY:** Power supply to internal analog circuit. |
| 4 | 6 | $AV_{SS}$ | | | | P | **GROUND: Analog** Ground potential. |
| 13 | 18 | LDO_CAP | | | | P | **LDO:** LDO output pin<br>**Note: It needs to be connected with a 1uF capacitor.** |
| 2 | 4 | $\overline{RST}$ | | | | I (ST) | **RESET:** /RST pin is a Schmitt trigger input pin for hardware device reset. A "**Low**" on this pin for 768 clock counter of Internal RC 22M while the system clock is running will reset the device. /RST pin has an internal pull-up resistor allowing power-on reset by simply connecting an external capacitor to GND. |
| 26 | 40 | P0.0 | CTS1 | AD0 | TXD1[2] | D, I/O | **PORT0:** Port 0 is an 8-bit four mode output pin and two mode input. Its multifunction pins are for CTS1, RTS1, CTS0, RTS0, SPISS1, MOSI_1, MISO_1, and SPICLK1.<br>P0 has an alternative function as AD[7:0] while external memory accessing. During the external memory access, P0 will output high will be internal strong pulled-up rather than weak pull-up in order to drive out high byte |
| 25 | 39 | P0.1 | RTS1 | AD1 | RXD1[2] | D, I/O | |
| NC | 38 | P0.2 | CTS0 | AD2 | TXD[2] | D, I/O | |

- Load/store-multiples and multicycle-multiplies that can be abandoned and restarted to facilitate rapid interrupt handling.
- C Application Binary Interface compliant exception model.
  This is the ARMv6-M, C Application Binary Interface(C-ABI) compliant exception model that enables the use of pure C functions as interrupt handlers.
- Low power sleep-mode entry using Wait For Interrupt (WFI), Wait For Event(WFE) instructions, or the return from interrupt sleep-on-exit feature.

**NVIC features:**

- 32 external interrupt inputs, each with four levels of priority.
- Dedicated non-Maskable Interrupt (NMI) input.
- Support for both level-sensitive and pulse-sensitive interrupt lines
- Wake-up Interrupt Controller (WIC), supports ultra-low power sleep mode.

**Debug support:**

- Four hardware breakpoints.
- Two watchpoints.
- Program Counter Sampling Register (PCSR) for non-intrusive code profiling.
- Single step and vector catch capabilities.

**Bus interfaces:**

- Single 32-bit AMBA-3 AHB-Lite system interface that provides simple integration to all system peripherals and memory.
- Single 32-bit slave port that supports the DAP (Debug Access Port).

## 6.2 System Manager

### 6.2.1 Overview

The following functions are included in system manager section

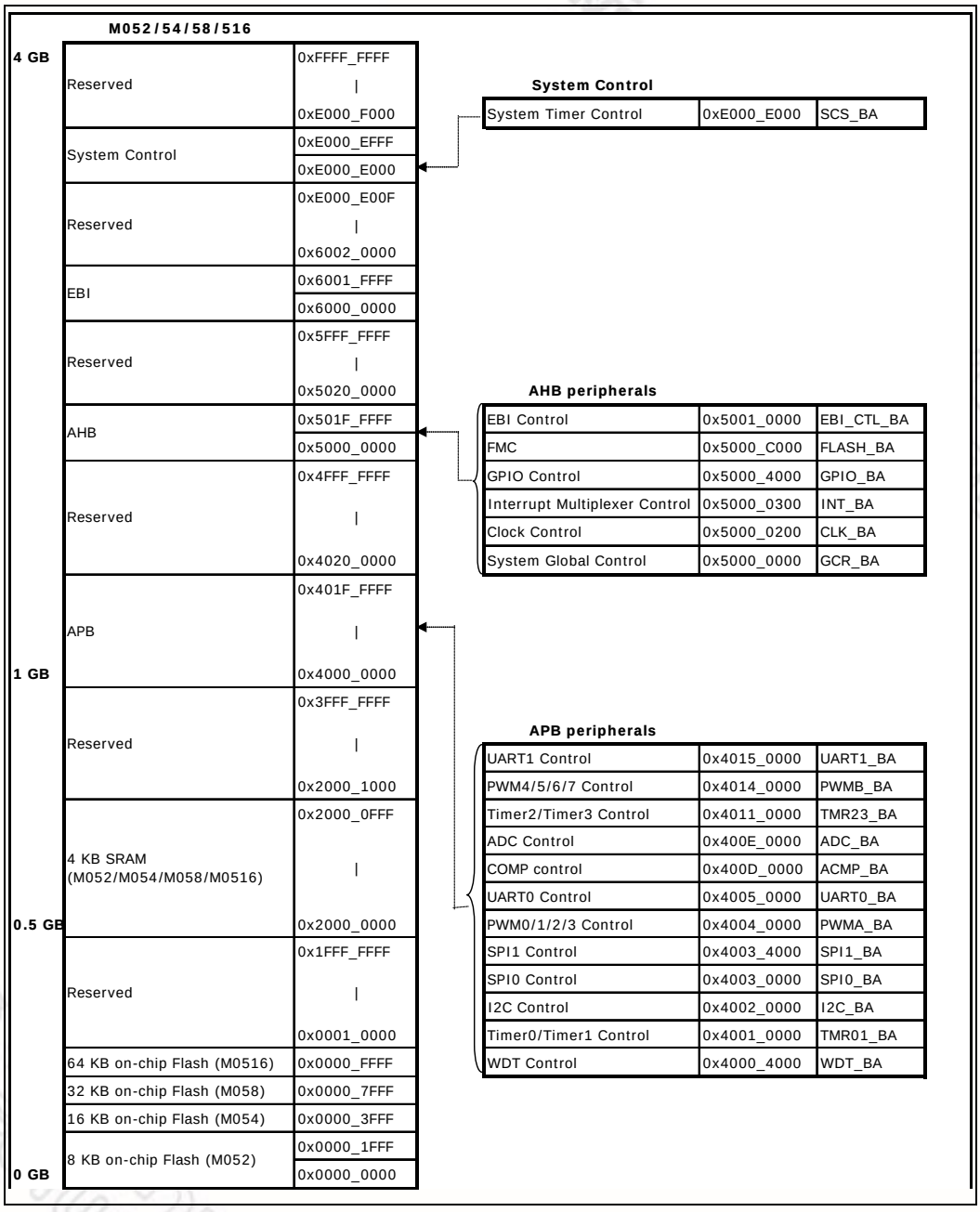
- System Resets
- System Memory Map
- System management registers for Part Number ID, chip reset and on-chip module reset , multi-functional pin control
- System Timer (SysTick)
- Nested Vectored Interrupt Controller (NVIC)
- System Control registers

### 6.2.2 System Reset

The system reset includes one of the list below event occurs. For these reset event flags can be read by RSTSRC register.

- The Power-On Reset (POR)
- The low level on the /RESET pin
- Watchdog Time Out Reset (WDT)
- Low Voltage Reset (LVR)
- Brown-Out Detected Reset (BOD)
- CPU Reset
- Software one shot Reset

### 6.2.5 Whole System Memory Mapping Table




### 6.2.6 System Timer (SysTick)

The Cortex-M0 includes an integrated system timer, SysTick. SysTick provides a simple, 24-bit

clear-on-write, decrementing, wrap-on-zero counter with a flexible control mechanism. The counter can be used as a Real Time Operating System (RTOS) tick timer or as a simple counter.

When system timer is enabled, it will count down from the value in the SysTick Current Value Register (SYST_CVR) to zero, and reload (wrap) to the value in the SysTick Reload Value Register (SYST_RVR) on the next clock edge, then decrement on subsequent clocks. When the counter transitions to zero, the COUNTFLAG status bit is set. The COUNTFLAG bit clears on reads.

The SYST_CVR value is UNKNOWN on reset. Software should write to the register to clear it to zero before enabling the feature. This ensures the timer will count from the SYST_RVR value rather than an arbitrary value when it is enabled.

If the SYST_RVR is zero, the timer will be maintained with a current value of zero after it is reloaded with this value. This mechanism can be used to disable the feature independently from the timer enable bit.

For more detailed information, please refer to the documents “ARM® Cortex™-M0 Technical Reference Manual” and “ARM® v6-M Architecture Reference Manual”.

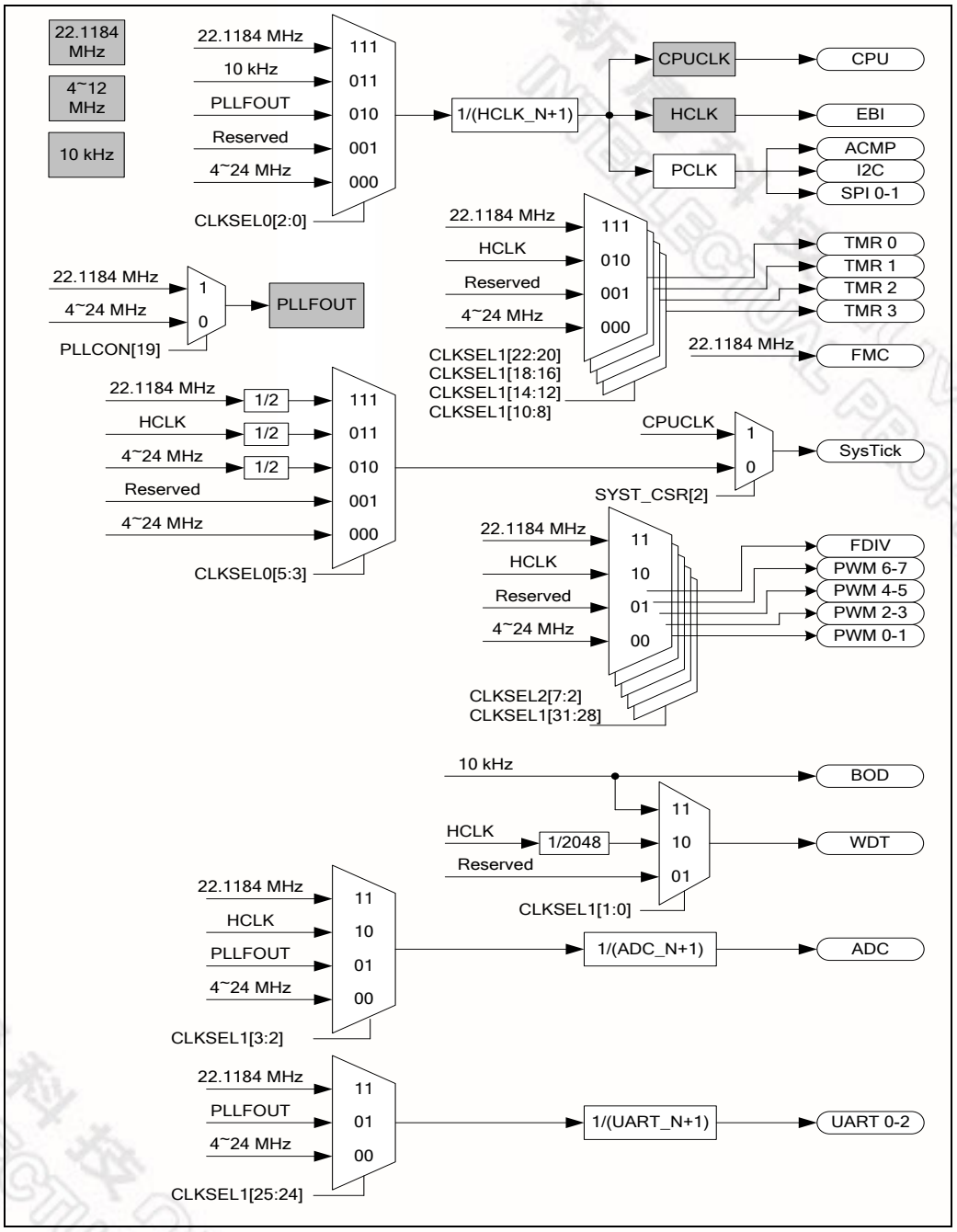



Figure 6-3 Clock generator block diagram

### 6.3.5 Peripherals Clock Source Select

The peripherals clock had different clock source switch setting which depends on the different peripheral.

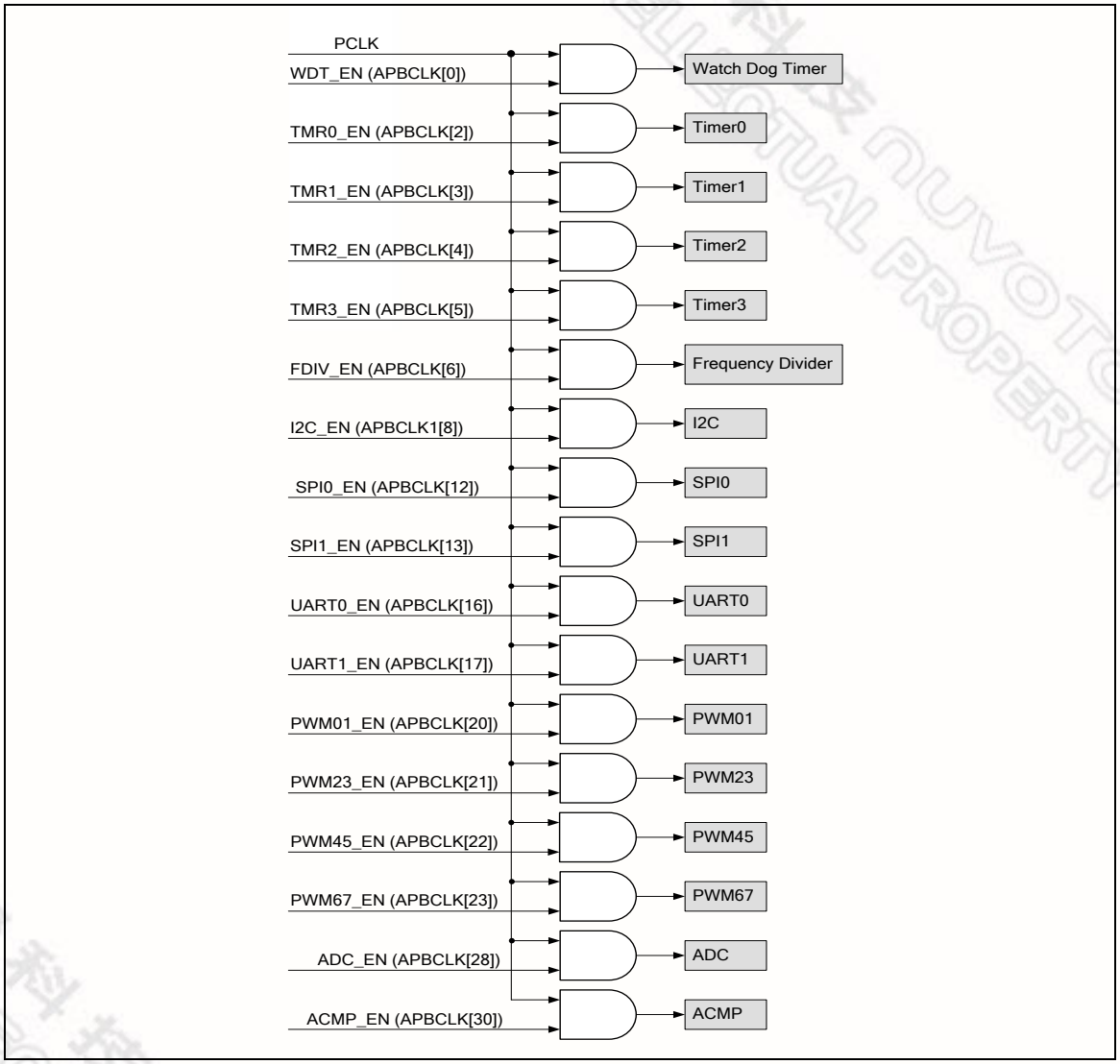



Figure 6-7 Peripherals Clock Source Select for PCLK

Figure 6-12 Quasi-bidirectional I/O Mode

## 6.8 Timer Controller

### 6.8.1 Overview

NuMicro M051™ series timer controller includes four 32-bit timers, which allows user to easily implement a timer control for applications. The timer can perform functions like frequency measurement, event counting, interval measurement, clock generation, delay timing, and so on. The timer can generates an interrupt signal upon timeout, or provide the current counting value during operation.

### 6.8.2 Features:

- 4 sets of 32-bit timers with 24-bit up-timer and one 8-bit pre-scale counter
- Independent clock source for each timer
- Provides one-shot, periodic, toggle and continuous counting operation modes
- Time out period = (Period of timer clock input) * (8-bit pre-scale counter + 1) * (24-bit TCMP)
- Maximum counting cycle time = (1 / T MHz) * ($2^8$) * ($2^{24}$), T is the period of timer clock
- 24-bit timer value is readable through TDR (Timer Data Register)
- Support event counting function to count the event from external pin
- Support input capture function to capture or reset counter value

## 6.9 Watchdog Timer (WDT)

### 6.9.1 Overview

The purpose of Watchdog Timer is to perform a system reset when system runs into an unknown state. This prevents system from hanging for an infinite period of time. Besides, this Watchdog Timer supports another function to wakeup chip from power down mode. The watchdog timer includes an 18-bit free running counter with programmable time-out intervals. Table 6-2 show the watchdog timeout interval selection and Figure 6.9-1 shows the timing of watchdog interrupt signal and reset signal.

Setting WTE (WDTCR [7]) enables the watchdog timer and the WDT counter starts counting up. When the counter reaches the selected time-out interval, Watchdog timer interrupt flag WTIF will be set immediately to request a WDT interrupt if the watchdog timer interrupt enable bit WTIE is set, in the meanwhile, a specified delay time (1024 * $T_{WDT}$) follows the time-out event. User must set WTR (WDTCR [0]) (Watchdog timer reset) high to reset the 18-bit WDT counter to avoid chip from Watchdog timer reset before the delay time expires. WTR bit is cleared automatically by hardware after WDT counter is reset. There are eight time-out intervals with specific delay time which are selected by Watchdog timer interval select bits WTIS (WDTCR [10:8]). If the WDT counter has not been cleared after the specific delay time expires, the watchdog timer will set Watchdog Timer Reset Flag (WTRF) high and reset chip. This reset will last 63 WDT clocks ($T_{RST}$) then chip restarts executing program from reset vector (0x0000 0000). WTRF will not be cleared by Watchdog reset. User may poll WTFR by software to recognize the reset source. WDT also provides wakeup function. When chip is powered down and the Watchdog Timer Wake-up Function Enable bit (WDTR[4]) is set, if the WDT counter reaches the specific time interval defined by WTIS (WDTCR [10:8]) , the chip is waken up from power down state. First example, if WTIS is set as 000, the specific time interval for chip to wake up from power down state is $2^4$ * $T_{WDT}$. When power down command is set by software, then, chip enters power down state. After $2^4$ * $T_{WDT}$ time is elapsed, chip is waken up from power down state. Second example, if WTIS (WDTCR [10:8]) is set as 111, the specific time interval for chip to wake up from power down state is $2^{18}$ * $T_{WDT}$. If power down command is set by software, then, chip enters power down state. After $2^{18}$ * $T_{WDT}$ time is elapsed, chip is waken up from power down state. Notice if WTRE (WDTCR [1]) is set to 1, after chip is waken up, software should chip the Watchdog Timer counter by setting WTR(WDTCR [0]) to 1 as soon as possible. Otherwise, if the Watchdog Timer counter is not cleared by setting WTR (WDTCR [0]) to 1 before time starting from waking up to software clearing Watchdog Timer counter is over 1024 * $T_{WDT}$ , the chip is reset by Watchdog Timer.

| WTIS | Timeout Interval Selection<br>$T_{TIS}$ | Interrupt Period<br>$T_{INT}$ | WTR Timeout Interval (WDT_CLK=10 kHz)<br>MIN. $T_{WTR}$ ~ MAX. $T_{WTR}$ |
|---|---|---|---|
| 000 | $2^4$ * $T_{WDT}$ | 1024 * $T_{WDT}$ | 1.6 ms ~ 104 ms |
| 001 | $2^6$ * $T_{WDT}$ | 1024 * $T_{WDT}$ | 6.4 ms ~ 108.8 ms |
| 010 | $2^8$ * $T_{WDT}$ | 1024 * $T_{WDT}$ | 25.6 ms ~ 128 ms |
| 011 | $2^{10}$ * $T_{WDT}$ | 1024 * $T_{WDT}$ | 102.4 ms ~ 204.8 ms |
| 100 | $2^{12}$ * $T_{WDT}$ | 1024 * $T_{WDT}$ | 409.6 ms ~ 512 ms |
| 101 | $2^{14}$ * $T_{WDT}$ | 1024 * $T_{WDT}$ | 1.6384 s ~ 1.7408 s |

# 8 ELECTRICAL CHARACTERISTICS

## 8.1 Absolute Maximum Ratings

| SYMBOL | PARAMETER | MIN | MAX | UNIT |
|---|---|---|---|---|
| DC Power Supply | $V_{DD}$ –$V_{SS}$ | -0.3 | +7.0 | V |
| Input Voltage | VIN | $V_{SS}$-0.3 | $V_{DD}$ +0.3 | V |
| Oscillator Frequency | $1/t_{CLCL}$ | 4 | 24 | MHz |
| Operating Temperature | TA | -40 | +85 | °C |
| Storage Temperature | TST | -55 | +150 | °C |
| Maximum Current into $V_{DD}$ | | - | 120 | mA |
| Maximum Current out of $V_{SS}$ | | | 120 | mA |
| Maximum Current sunk by a I/O pin | | | 35 | mA |
| Maximum Current sourced by a I/O pin | | | 35 | mA |
| Maximum Current sunk by total I/O pins | | | 100 | mA |
| Maximum Current sourced by total I/O pins | | | 100 | mA |

Note: Exposure to conditions beyond those listed under absolute maximum ratings may adversely affects the lift and reliability of the device.

### 8.4.3 Specification of Low Voltage Reset

| PARAMETER | CONDITION | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|
| Operation voltage | - | 2.5 | 5 | 5.5 | V |
| Temperature | - | -40 | 25 | 85 | ℃ |
| Quiescent current | $V_{DD}$ =5.5V | - | - | 5 | uA |
| Threshold voltage | Temperature=25° | 1.7 | 2.0 | 2.3 | V |
| | Temperature=-40° | - | 2.3 | - | V |
| | Temperature=85° | - | 1.8 | - | V |
| Hysteresis | - | 0 | 0 | 0 | V |

### 8.4.4 Specification of Brown-Out Detector

| Parameter | Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| Operation voltage | - | 2.5 | - | 5.5 | V |
| Quiescent current | $AV_{DD}$ =5.5V | - | - | 140 | μA |
| Temperature | - | -40 | 25 | 85 | ℃ |
| Brown-Out voltage | BOV_VL[1:0]=11 | 4.1 | 4.3 | 4.5 | V |
| | BOV_VL [1:0]=10 | 3.5 | 3.7 | 3.9 | V |
| | BOV_VL [1:0]=01 | 2.5 | 2.7 | 2.9 | V |
| | BOV_VL [1:0]=00 | 2.0 | 2.2 | 2.4 | V |
| Hysteresis | - | 30m | - | 150m | V |

### 8.4.5 Specification of Power-On Reset (5V)

| Parameter | Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| Temperature | - | -40 | 25 | 85 | ℃ |
| Reset voltage | V+ | - | 2 | - | V |

## Important Notice

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**Insecure usage includes, but is not limited to: equipment for surgical implementation, atomic energy control instruments, airplane or spaceship instruments, the control or operation of dynamic, brake or safety systems designed for vehicular use, traffic signal instruments, all types of safety devices, and other applications intended to support or sustain life.**

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