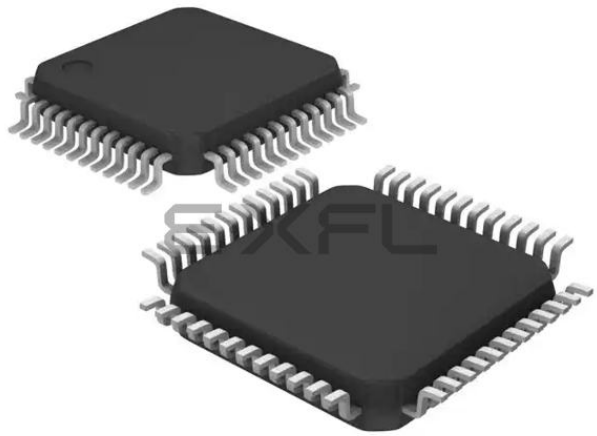

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	ARM® Cortex®-M0
Core Size	32-Bit Single-Core
Speed	50MHz
Connectivity	EBI/EMI, I²C, IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	40
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	2.5V ~ 5.5V
Data Converters	A/D 8x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/nuvoton-technology-corporation-america/m054lbn

1 GENERAL DESCRIPTION

The NuMicro M051™ series is a 32-bit microcontroller with embedded ARM® Cortex™-M0 core for industrial control and applications which need rich communication interfaces. The Cortex™-M0 is the newest ARM embedded processor with 32-bit performance and at a cost equivalent to traditional 8-bit microcontroller. The NuMicro M051™ series includes M052, M054, M058 and M0516 families.

The M052/M054 can run up to 50 MHz. Thus it can afford to support a variety of industrial control and applications which need high CPU performance. The M052/M054 has 8K/16K-byte embedded flash, 4K-byte data flash, 4K-byte flash for the ISP, and 4K-byte embedded SRAM.

Many system level peripheral functions, such as I/O Port, EBI (External Bus Interface), Timer, UART, SPI, I2C, PWM, ADC, Watchdog Timer and Brownout Detector, have been incorporated into the M052/M054 in order to reduce component count, board space and system cost. These useful functions make the M052/M054 powerful for a wide range of applications.

Additionally, the M052/M054 is equipped with ISP (In-System Programming) and ICP (In-Circuit Programming) functions, which allow the user to update the program memory without removing the chip from the actual end product.

2 FEATURES

- Core
  - ARM® Cortex™-M0 core runs up to 50 MHz.
  - One 24-bit system timer.
  - Supports low power sleep-mode.
  - A single-cycle 32-bit hardware multiplier.
  - NVIC for the 32 interrupt inputs, each with 4-levels of priority.
  - Supports Serial Wire Debug (SWD) interface and 2 watchpoints/4 breakpoints.
- Built-in LDO for Wide Operating Voltage Range: 2.5V to 5.5V
- Memory
  - 8KB/16KB Flash memory for program memory (APROM)
  - 4KB Flash memory for data memory (DataFlash)
  - 4KB Flash memory for loader (LDROM)
  - 4KB SRAM for internal scratch-pad RAM (SRAM)
- Clock Control
  - Programmable system clock source
  - 4~24 MHz external crystal input
  - 22.1184 MHz internal oscillator (trimmed to 3% accuracy)
  - 10 kHz low-power oscillator for Watchdog Timer and wake-up in sleep mode
  - PLL allows CPU operation up to the maximum 50MHz
- I/O Port
  - Up to 40 general-purpose I/O (GPIO) pins for LQFP-48 package
  - Four I/O modes:
    - Quasi bi-direction
    - Push-Pull output

- Open-Drain output
- Input only with high impendence

- TTL/Schmitt trigger input selectable
- I/O pin can be configured as interrupt source with edge/level setting
- Supports high driver and high sink IO mode

- Timer
  - Provides four channel 32-bit timers, one 8-bit pre-scale counter with 24-bit up-timer for each timer.
  - Independent clock source for each timer.
  - 24-bit timer value is readable through TDR (Timer Data Register)
  - Provides one-shot, periodic and toggle operation modes.
  - Provide event counter function.
  - Provide external capture/reset counter function equivalent to 8051 Timer2.
- Watchdog Timer
  - Multiple clock sources
  - Supports wake up from power down or sleep mode
  - Interrupt or reset selectable on watchdog time-out
- PWM
  - Built-in up to four 16-bit PWM generators; providing eight PWM outputs or four complementary paired PWM outputs
  - Individual clock source, clock divider, 8-bit pre-scalar and dead-zone generator for each PWM generator
  - PWM interrupt synchronized to PWM period
  - 16-bit digital Capture timers (shared with PWM timers) with rising/falling capture inputs
  - Supports capture interrupt
- UART

Pin number		Symbol	Alternate Function			Type[1]	Description
QFN33	LQFP48		1	2	3		
NC	37	P0.3	RTS0	AD3	RXD[2]	D, I/O	address for external devices. These pins which are SPISS1, MOSI_1, MISO_1, and SPICLK1 for the SPI function used. CTS0/1: Clear to Send input pin for UART0/1 RTS0/1: Request to Send output pin for UART0/1 The RXD/TXD pins are for UART0 function used. The RXD1/TXD1 pins are for UART1 function used.
24	35	P0.4	SPISS1	AD4		D, I/O	
23	34	P0.5	MOSI_1	AD5		D, I/O	
22	33	P0.6	MISO_1	AD6		D, I/O	
21	32	P0.7	SPICLK1	AD7		D, I/O	
29	43	P1.0	T2	AIN0	$\overline{\text{WRL}}$	I/O	**PORT1:** Port 1 is an 8-bit four mode output pin and two mode input. Its multifunction pins are for T2, T3, RXD1, TXD1, SPISS0, MOSI_0, MISO_0, and SPICLK0. These pins which are SPISS0, MOSI_0, MISO_0, and SCLK0 for the SPI function used. These pins which are AIN0~AIN7for the 12 bits ADC function used. The RXD1/TXD1 pins are for UART1 function used. The $\overline{\text{WRL}}$ / $\overline{\text{WRH}}$ pins are for low/high byte write enable output in 16-bit data width of EBI. The CPN0/CPP0 pins are for Comparator0 negative/positive inputs. The T2/T3 pins are for Timer2/3 external even counter input.
NC	44	P1.1	T3	AIN1	$\overline{\text{WRH}}$	I/O	
30	45	P1.2	RXD1[3]	AIN2		I/O	
31	46	P1.3	TXD1[3]	AIN3		I/O	
32	47	P1.4	SPISS0	AIN4	CPN0	I/O	
1	1	P1.5	MOSI_0	AIN5	CPP0	I/O	
NC	2	P1.6	MISO_0	AIN6		I/O	
NC	3	P1.7	SPICLK0	AIN7		I/O	
NC	19	P2.0	PWM0[2]	AD8		D, I/O	**PORT2:** Port 2 is an 8-bit four mode output pin and two mode input. It has an alternative function P2 has an alternative function as AD[15:8] while external memory accessing. During the external memory access, P2 will output high will be internal strong pulled-up rather than weak pull-up in order to drive out high byte address for external devices. These pins which are PWM0~PWM7 for the PWM function used in the LQFP48 package.
NC	20	P2.1	PWM1[2]	AD9		D, I/O	
14	21	P2.2	PWM2[2]	AD10		D, I/O	
15	22	P2.3	PWM3[2]	AD11		D, I/O	

0x4005_0000 – 0x4005_3FFF	UART0_BA	UART0 Control Registers
0x400D_0000 – 0x400D_3FFF	ACMP_BA	Analog Comparator Control Registers
0x400E_0000 – 0x400E_FFFF	ADC_BA	Analog-Digital-Converter (ADC) Control Registers
0x4011_0000 – 0x4011_3FFF	TMR23_BA	Timer2/Timer3 Control Registers
0x4014_0000 – 0x4014_3FFF	PWMB_BA	PWM4/5/6/7 Control Registers
0x4015_0000 – 0x4015_3FFF	UART1_BA	UART1 Control Registers
System Control Space (0xE000_E000 ~ 0xE000_EFFF)		
0xE000_E010 – 0xE000_E0FF	SCS_BA	System Timer Control Registers
0xE000_E100 – 0xE000_ECFF	SCS_BA	External Interrupt Controller Control Registers
0xE000_ED00 – 0xE000_ED8F	SCS_BA	System Control Registers

Table 6-1 Address Space Assignments for On-Chip Modules

clear-on-write, decrementing, wrap-on-zero counter with a flexible control mechanism. The counter can be used as a Real Time Operating System (RTOS) tick timer or as a simple counter.

When system timer is enabled, it will count down from the value in the SysTick Current Value Register (SYST_CVR) to zero, and reload (wrap) to the value in the SysTick Reload Value Register (SYST_RVR) on the next clock edge, then decrement on subsequent clocks. When the counter transitions to zero, the COUNTFLAG status bit is set. The COUNTFLAG bit clears on reads.

The SYST_CVR value is UNKNOWN on reset. Software should write to the register to clear it to zero before enabling the feature. This ensures the timer will count from the SYST_RVR value rather than an arbitrary value when it is enabled.

If the SYST_RVR is zero, the timer will be maintained with a current value of zero after it is reloaded with this value. This mechanism can be used to disable the feature independently from the timer enable bit.

For more detailed information, please refer to the documents “ARM® Cortex™-M0 Technical Reference Manual” and “ARM® v6-M Architecture Reference Manual”.

6.3 Clock Controller

6.3.1 Overview

The clock controller generates the clocks for the whole chip, including system clocks and all peripheral clocks. The clock controller also implements the power control function with the individually clock ON/OFF control, clock source selection and clock divider. The chip will not enter power-down mode until CPU sets the power down enable bit (PWR_DOWN_EN) and Cortex-M0 core executes the WFI instruction. After that, chip enter power-down mode and wait for wake-up interrupt source triggered to leave power-down mode. In the power down mode, the clock controller turns off the external crystal and internal 22.1184 MHz oscillator to reduce the overall system power consumption.

6.3.2 Clock Generator Block Diagram

The clock generator consists of 4 sources which list below:

- One external 4~24 MHz crystal
- One internal 22.1184 MHz RC oscillator
- One programmable PLL FOUT(PLL source consists of external 4~24 MHz crystal and internal 22.1184M)
- One internal 10 kHz oscillator

6.3.4 AHB Clock Source Select

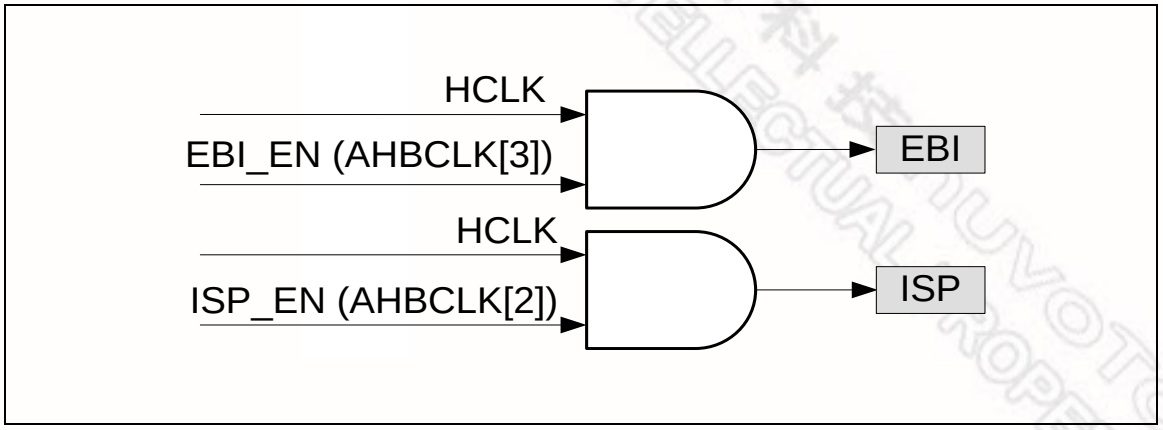


Figure 6-6 AHB Clock Source for HCLK

6.4 General Purpose I/O

6.4.1 Overview

There are 40 General Purpose I/O pins shared with special feature functions in this MCU. The 40 pins are arranged in 5 ports named with P0, P1, P2, P3 and P4. Each port equips maximum 8 pins. Each one of the 40 pins is independent and has the corresponding register bits to control the pin mode function and data

The I/O type of each of I/O pins can be software configured individually as input, output, open-drain or quasi-bidirectional mode. The all pins of I/O type stay in quasi-bidirectional mode and port data register Px_DOUT[7:0] resets to 0x000_00FF. Each I/O pin equips a very weakly individual pull-up resistor which is about 110KΩ~300KΩ for V_{DD} is from 5.0V to 2.5V.

6.4.1.1 Input Mode Explanation

Set Px_PMD(PMDn[1:0]) to 00b the Px[n] pin is in Input mode and the I/O pin is in tri-state(high impedance) without output drive capability. The Px_PIN value reflects the status of the corresponding port pins.

6.4.1.2 Output Mode Explanation

Set Px_PMD(PMDn[1:0]) to 2'b01 the Px[n] pin is in Output mode and the I/O pin supports digital output function with source/sink current capability. The bit value in the corresponding bit [n] of Px_DOUT is driven on the pin.

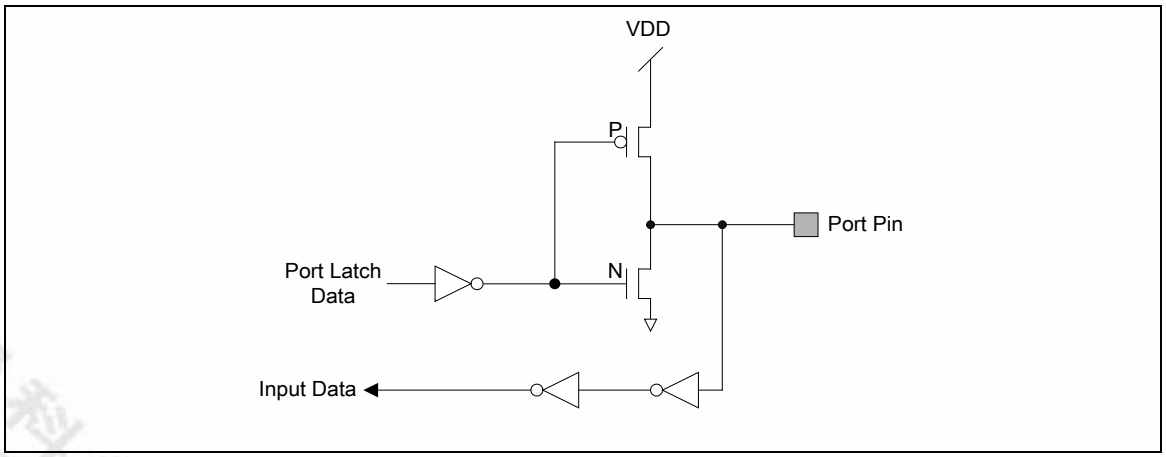


Figure 6-10 Push-Pull Output

6.5 I²C Serial Interface Controller (Master/Slave)

6.5.1 Overview

I²C is a two-wire, bi-directional serial bus that provides a simple and efficient method of data exchange between devices. The I²C standard is a true multi-master bus including collision detection and arbitration that prevents data corruption if two or more masters attempt to control the bus simultaneously.

Data is transferred between a Master and a Slave synchronously to SCL on the SDA line on a byte-by-byte basis. Each data byte is 8 bits long. There is one SCL clock pulse for each data bit with the MSB being transmitted first. An acknowledge bit follows each transferred byte. Each bit is sampled during the high period of SCL; therefore, the SDA line may be changed only during the low period of SCL and must be held stable during the high period of SCL. A transition on the SDA line while SCL is high is interpreted as a command (START or STOP). Please refer to the Figure 6-13 for more detail I²C BUS Timing.

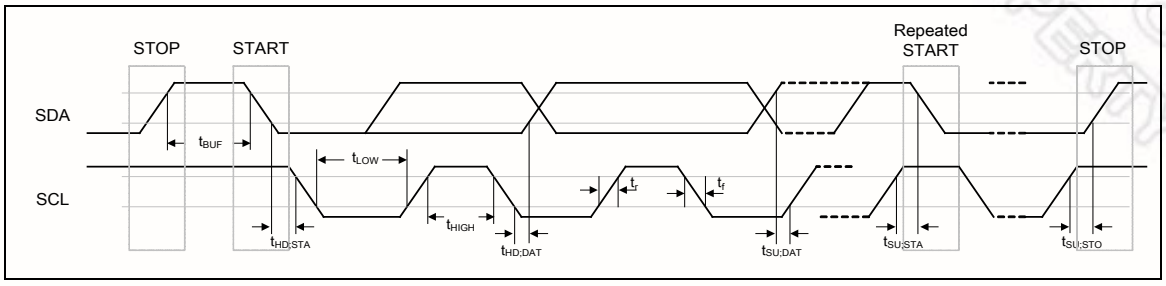


Figure 6-13 I²C Bus Timing

The device's on-chip I²C provides the serial interface that meets the I²C bus standard mode specification. The I²C port handles byte transfers autonomously. To enable this port, the bit ENS1 in I2CON should be set to '1'. The I²C H/W interfaces to the I²C bus via two pins: SDA (serial data line) and SCL (serial clock line). Pull up resistor is needed on pin SDA and SCL for I²C operation as these are open drain pins. When the I/O pins are used as I²C port, user must set the pins function to I²C in advance.

PIIR to get interrupt source and Read PWM_CRLx/PWM_CFLx(x=0 and 3) to get capture value and finally write 1 to clear PIIR. If interrupt latency will take time T0 to finish, the capture signal mustn't transition during this interval (T0). In this case, the maximum capture frequency will be 1/T0. For example:

HCLK = 50 MHz, PWM_CLK = 25 MHz, Interrupt latency is 900 ns

So the maximum capture frequency will is 1/900ns ≈ 1000 kHz

6.6.2 Features

6.6.2.1 PWM function features:

PWM group has two PWM generators. Each PWM generator supports one 8-bit prescaler, one clock divider, two PWM-timers (down counter), one dead-zone generator and two PWM outputs.

- Up to 16 bits resolution
- PWM Interrupt request synchronized with PWM period
- One-shot or Auto-reload mode PWM
- Up to 2 PWM group (PWMA/PWMB) to support 8 PWM channels

6.6.2.2 Capture Function Features:

- Timing control logic shared with PWM Generators
- 8 capture input channels shared with 8 PWM output channels
- Each channel supports one rising latch register (CRLR), one falling latch register (CFLR) and Capture interrupt flag (CAPIFx)

6.9 Watchdog Timer (WDT)

6.9.1 Overview

The purpose of Watchdog Timer is to perform a system reset when system runs into an unknown state. This prevents system from hanging for an infinite period of time. Besides, this Watchdog Timer supports another function to wakeup chip from power down mode. The watchdog timer includes an 18-bit free running counter with programmable time-out intervals. Table 6-2 show the watchdog timeout interval selection and Figure 6.9-1 shows the timing of watchdog interrupt signal and reset signal.

Setting WTE (WDTCR [7]) enables the watchdog timer and the WDT counter starts counting up. When the counter reaches the selected time-out interval, Watchdog timer interrupt flag WTIF will be set immediately to request a WDT interrupt if the watchdog timer interrupt enable bit WTIE is set, in the meanwhile, a specified delay time (1024 * T_{WDT}) follows the time-out event. User must set WTR (WDTCR [0]) (Watchdog timer reset) high to reset the 18-bit WDT counter to avoid chip from Watchdog timer reset before the delay time expires. WTR bit is cleared automatically by hardware after WDT counter is reset. There are eight time-out intervals with specific delay time which are selected by Watchdog timer interval select bits WTIS (WDTCR [10:8]). If the WDT counter has not been cleared after the specific delay time expires, the watchdog timer will set Watchdog Timer Reset Flag (WTRF) high and reset chip. This reset will last 63 WDT clocks (T_{RST}) then chip restarts executing program from reset vector (0x0000 0000). WTRF will not be cleared by Watchdog reset. User may poll WTFR by software to recognize the reset source. WDT also provides wakeup function. When chip is powered down and the Watchdog Timer Wake-up Function Enable bit (WDTR[4]) is set, if the WDT counter reaches the specific time interval defined by WTIS (WDTCR [10:8]) , the chip is waken up from power down state. First example, if WTIS is set as 000, the specific time interval for chip to wake up from power down state is 2^4 * T_{WDT}. When power down command is set by software, then, chip enters power down state. After 2^4 * T_{WDT} time is elapsed, chip is waken up from power down state. Second example, if WTIS (WDTCR [10:8]) is set as 111, the specific time interval for chip to wake up from power down state is 2^{18} * T_{WDT}. If power down command is set by software, then, chip enters power down state. After 2^{18} * T_{WDT} time is elapsed, chip is waken up from power down state. Notice if WTRE (WDTCR [1]) is set to 1, after chip is waken up, software should chip the Watchdog Timer counter by setting WTR(WDTCR [0]) to 1 as soon as possible. Otherwise, if the Watchdog Timer counter is not cleared by setting WTR (WDTCR [0]) to 1 before time starting from waking up to software clearing Watchdog Timer counter is over 1024 * T_{WDT} , the chip is reset by Watchdog Timer.

WTIS	Timeout Interval Selection T_{TIS}	Interrupt Period T_{INT}	WTR Timeout Interval (WDT_CLK=10 kHz) MIN. T_{WTR} ~ MAX. T_{WTR}
000	2^4 * T_{WDT}	1024 * T_{WDT}	1.6 ms ~ 104 ms
001	2^6 * T_{WDT}	1024 * T_{WDT}	6.4 ms ~ 108.8 ms
010	2^8 * T_{WDT}	1024 * T_{WDT}	25.6 ms ~ 128 ms
011	2^{10} * T_{WDT}	1024 * T_{WDT}	102.4 ms ~ 204.8 ms
100	2^{12} * T_{WDT}	1024 * T_{WDT}	409.6 ms ~ 512 ms
101	2^{14} * T_{WDT}	1024 * T_{WDT}	1.6384 s ~ 1.7408 s

110	$2^{16} * T_{WDT}$	$1024 * T_{WDT}$	6.5536 s ~ 6.656 s
111	$2^{18} * T_{WDT}$	$1024 * T_{WDT}$	26.2144 s ~ 26.3168 s

Table 6-2 Watchdog Timeout Interval Selection

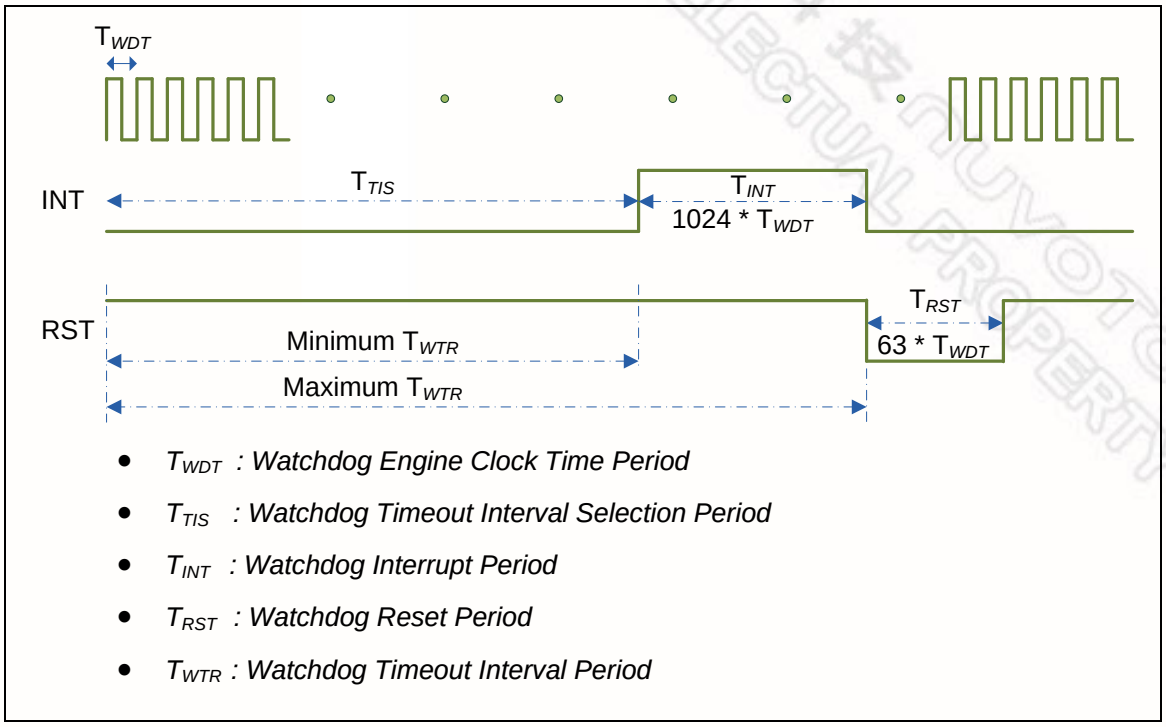


Figure 6-14 Timing of Interrupt and Reset Signal

6.9.2 Features

- 18-bit free running counter to avoid chip from Watchdog timer reset before the delay time expires.
- Selectable time-out interval (2^4 ~ 2^{18}) and the time out interval is 104 ms ~ 26.3168 s (if WDT_CLK = 10 kHz).
- Reset period = (1 / 10 kHz) * 63, if WDT_CLK = 10 kHz.

- Channel 7 supports 3 input sources: external analog voltage, internal bandgap voltage, and internal temperature sensor output.

6.12 External Bus Interface (EBI)

6.12.1 Overview

NuMicro M051™ series equips an external bus interface (EBI) for external device used.

To save the connections between external device and this chip, EBI support address bus and data bus multiplex mode. And, address latch enable (ALE) signal supported differentiate the address and data cycle.

6.12.2 Features

External Bus Interface has the following functions:

1. External devices with max. 64K-byte size (8 bit data width)/128K-byte (16 bit data width) supported
2. Variable external bus base clock (MCLK) supported
3. 8 bit or 16 bit data width supported
4. Variable data access time (tACC), address latch enable time (tALE) and address hold time (tAHD) supported
5. Address bus and data bus multiplex mode supported to save the address pins
6. Configurable idle cycle supported for different access condition: Write command finish (W2X), Read-to-Read (R2R)

8.2 DC Electrical Characteristics

(V_{DD} -V_{SS}=2.5~5.5V, TA = 25°C, F_{OSC} = 50 MHz unless otherwise specified.)

PARAMETER	SYM.	SPECIFICATION				TEST CONDITIONS
		MIN.	TYP.	MAX.	UNIT	
Operation voltage	V_{DD}	2.5		5.5	V	V_{DD} =2.5V ~ 5.5V up to 50 MHz
LDO Output Voltage	V_{LDO}	1.7	1.8	1.9	V	V_{DD} ≥ 2.5V
Band Gap Analog Input	V_{BG}	-5%	1.20	+5%	V	V_{DD} =2.5V ~ 5.5V
Analog Operating Voltage	AV_{DD}	0		V_{DD}	V	
Analog Reference Voltage	Vref	0		AV_{DD}	V	
Operating Current Normal Run Mode @ 50 MHz	IDD1		20.6		mA	V_{DD} = 5.5V@50MHz, enable all IP and PLL, XTAL=12MHz
	IDD2		14.4		mA	V_{DD} =5.5V@50MHz, disable all IP and enable PLL, XTAL=12MHz
	IDD3		18.9		mA	V_{DD} = 3.3V@50MHz, enable all IP and PLL, XTAL=12MHz
	IDD4		12.8		mA	V_{DD} = 3.3V@50MHz, disable all IP and enable PLL, XTAL=12MHz
Operating Current Normal Run Mode @ 22Mhz	IDD5		6.2		mA	V_{DD} = 5.5V@22MHz, enable all IP and IRC22M, disable PLL
	IDD6		3.4		mA	V_{DD} =5.5V@22MHz, disable all IP and enable IRC22M, disable PLL
	IDD7		6.1		mA	V_{DD} = 3.3V@22MHz, enable all IP and IRC22M, disable PLL
	IDD8		3.4		mA	V_{DD} = 3.3V@22MHz, disable all IP and enable IRC22M, disable PLL
Operating Current Normal Run Mode @ 12Mhz	IDD9		5.3		mA	V_{DD} = 5.5V@12MHz, enable all IP and disable PLL, XTAL=12MHz
	IDD10		3.7		mA	V_{DD} = 5.5V@12MHz, disable all IP and disable PLL, XTAL=12MHz
	IDD11		4.0		mA	V_{DD} = 3.3V@12MHz, enable all IP and disable PLL, XTAL=12MHz

	IDD12		2.3		mA	V_{DD} = 3.3V@12MHz, disable all IP and disable PLL, XTAL=12MHz
Operating Current Normal Run Mode @ 4 MHz	IDD13		3.4		mA	V_{DD} = 5.5V@4MHz, enable all IP and disable PLL, XTAL=4MHz
	IDD14		2.6		mA	V_{DD} = 5.5V@4MHz, disable all IP and disable PLL, XTAL=4MHz
	IDD15		2.0		mA	V_{DD} = 3.3V@4MHz, enable all IP and disable PLL, XTAL=4MHz
	IDD16		1.3		mA	V_{DD} = 3.3V@4MHz, disable all IP and disable PLL, XTAL=4MHz
Operating Current Normal Run Mode @10Khz	IDD17		98.7		uA	V_{DD} = 5.5V@10KHz, enable all IP and IRC10K, disable PLL
	IDD18		97.4		uA	V_{DD} = 5.5V@10KHz, disable all IP and enable IRC10K, disable PLL
	IDD19		86.4		uA	V_{DD} = 3.3V@10KHz, enable all IP and IRC10K, disable PLL
	IDD20		85.2		uA	V_{DD} = 3.3V@10KHz, disable all IP and enable IRC10K, disable PLL
Operating Current Idle Mode @ 50 MHz	IIDLE1		16.2		mA	V_{DD} = 5.5V@50 MHz, enable all IP and PLL, XTAL=12 MHz
	IIDLE2		10.0		mA	V_{DD} =5.5V@50 MHz, disable all IP and enable PLL, XTAL=12 MHz
	IIDLE3		14.6		mA	V_{DD} = 3V@50 MHz, enable all IP and PLL, XTAL=12 MHz
	IIDLE4		8.5		mA	V_{DD} = 3V@50 MHz, disable all IP and enable PLL, XTAL=12 MHz
Operating Current Idle Mode @ 22Mhz	IIDLE5		4.3		mA	V_{DD} = 5.5V@22MHz, enable all IP and IRC22M, disable PLL
	IIDLE6		1.5		mA	V_{DD} =5.5V@22MHz, disable all IP and enable IRC22M, disable PLL
	IIDLE7		4.2		mA	V_{DD} = 3.3V@22MHz, enable all IP and IRC22M, disable PLL
	IIDLE8		1.4		mA	V_{DD} = 3.3V@22MHz, disable all IP and enable IRC22M, disable PLL

8.4.2 Specification of LDO & Power management

RAMETER	MIN	TYP	MAX	UNIT	NOTE
Input Voltage	2.5	5	5.5	V	V_{DD} input voltage
Output Voltage	-10%	1.8	+10%	V	LDO output voltage
Temperature	-40	25	85	℃	
C	-	1u	-	F	Resr=1ohm

Note:

1. It is recommended a 100nF bypass capacitor is connected between V_{DD} and the closest V_{SS} pin of the device.
2. For ensuring power stability, a 1uF or higher capacitor must be connected between LDO pin and the closest V_{SS} pin of the device.

8.4.3 Specification of Low Voltage Reset

PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
Operation voltage	-	2.5	5	5.5	V
Temperature	-	-40	25	85	℃
Quiescent current	V_{DD} =5.5V	-	-	5	uA
Threshold voltage	Temperature=25°	1.7	2.0	2.3	V
	Temperature=-40°	-	2.3	-	V
	Temperature=85°	-	1.8	-	V
Hysteresis	-	0	0	0	V

8.4.4 Specification of Brown-Out Detector

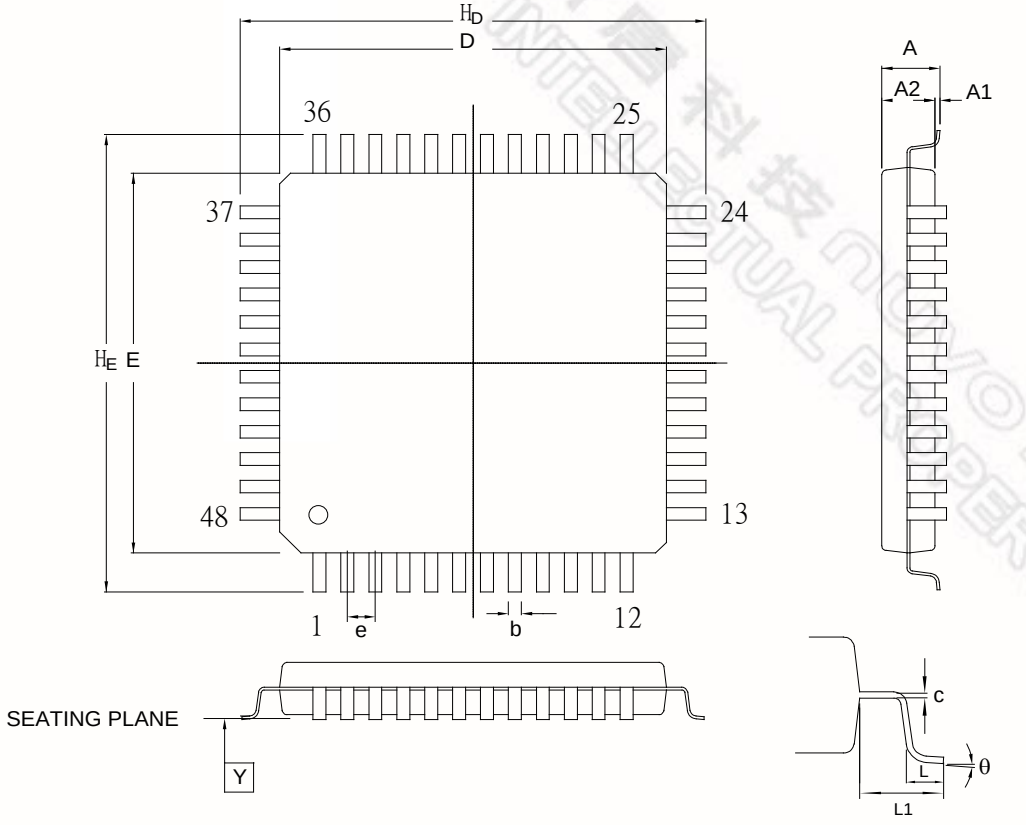
Parameter	Condition	Min.	Typ.	Max.	Unit
Operation voltage	-	2.5	-	5.5	V
Quiescent current	AV_{DD} =5.5V	-	-	140	μA
Temperature	-	-40	25	85	℃
Brown-Out voltage	BOV_VL[1:0]=11	4.1	4.3	4.5	V
	BOV_VL [1:0]=10	3.5	3.7	3.9	V
	BOV_VL [1:0]=01	2.5	2.7	2.9	V
	BOV_VL [1:0]=00	2.0	2.2	2.4	V
Hysteresis	-	30m	-	150m	V

8.4.5 Specification of Power-On Reset (5V)

Parameter	Condition	Min.	Typ.	Max.	Unit
Temperature	-	-40	25	85	℃
Reset voltage	V+	-	2	-	V

9 PACKAGE DIMENSIONS

9.1 LQFP-48 (7x7x1.4mm^2 Footprint 2.0mm)



Controlling dimension : Millimeters

Symbol	Dimension in inch			Dimension in mm		
	Min	Nom	Max	Min	Nom	Max
A	—	—	—	—	—	—
A_1	0.002	0.004	0.006	0.05	0.10	0.15
A_2	0.053	0.055	0.057	1.35	1.40	1.45
b	0.006	0.008	0.010	0.15	0.20	0.25
c	0.004	0.006	0.008	0.10	0.15	0.20
D	0.272	0.276	0.280	6.90	7.00	7.10
E	0.272	0.276	0.280	6.90	7.00	7.10
e	0.014	0.020	0.026	0.35	0.50	0.65
H_D	0.350	0.354	0.358	8.90	9.00	9.10
H_E	0.350	0.354	0.358	8.90	9.00	9.10
L	0.018	0.024	0.030	0.45	0.60	0.75
L_1	—	0.039	—	—	1.00	—
Y	—	—	0.004	—	—	0.10
θ	0°	—	7°	0°	—	7°

Important Notice

Nuvoton Products are neither intended nor warranted for usage in systems or equipment, any malfunction or failure of which may cause loss of human life, bodily injury or severe property damage. Such applications are deemed, "Insecure Usage".

Insecure usage includes, but is not limited to: equipment for surgical implementation, atomic energy control instruments, airplane or spaceship instruments, the control or operation of dynamic, brake or safety systems designed for vehicular use, traffic signal instruments, all types of safety devices, and other applications intended to support or sustain life.

All Insecure Usage shall be made at customer's risk, and in the event that third parties lay claims to Nuvoton as a result of customer's Insecure Usage, customer shall indemnify the damages and liabilities thus incurred by Nuvoton.