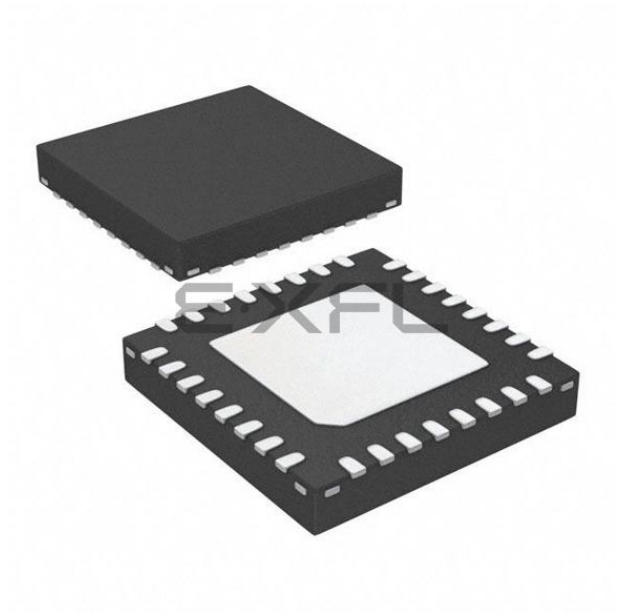

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	ARM® Cortex®-M0
Core Size	32-Bit Single-Core
Speed	50MHz
Connectivity	I²C, IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	24
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	2.5V ~ 5.5V
Data Converters	A/D 8x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	32-WFQFN Exposed Pad
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/nuvoton-technology-corporation-america/m054zbn

2 FEATURES

- Core
  - ARM® Cortex™-M0 core runs up to 50 MHz.
  - One 24-bit system timer.
  - Supports low power sleep-mode.
  - A single-cycle 32-bit hardware multiplier.
  - NVIC for the 32 interrupt inputs, each with 4-levels of priority.
  - Supports Serial Wire Debug (SWD) interface and 2 watchpoints/4 breakpoints.
- Built-in LDO for Wide Operating Voltage Range: 2.5V to 5.5V
- Memory
  - 8KB/16KB Flash memory for program memory (APROM)
  - 4KB Flash memory for data memory (DataFlash)
  - 4KB Flash memory for loader (LDROM)
  - 4KB SRAM for internal scratch-pad RAM (SRAM)
- Clock Control
  - Programmable system clock source
  - 4~24 MHz external crystal input
  - 22.1184 MHz internal oscillator (trimmed to 3% accuracy)
  - 10 kHz low-power oscillator for Watchdog Timer and wake-up in sleep mode
  - PLL allows CPU operation up to the maximum 50MHz
- I/O Port
  - Up to 40 general-purpose I/O (GPIO) pins for LQFP-48 package
  - Four I/O modes:
    - Quasi bi-direction
    - Push-Pull output

- Serial clock synchronization can be used as a handshake mechanism to suspend and resume serial transfer.
- Programmable clocks allow versatile rate control.
- Supports multiple address recognition (four slave address with mask option)

- ADC
  - 12-bit SAR ADC with 760k SPS
  - Up to 8-ch single-ended input or 4-ch differential input
  - Supports single mode/burst mode/single-cycle scan mode/continuous scan mode
  - Supports 2' complement/un-signed format in differential mode conversion result
  - Each channel with an individual result register
  - Supports conversion value monitoring (or comparison) for threshold voltage detection
  - Conversion can be started either by software trigger or external pin trigger
- Analog Comparator
  - Up to 2 comparator analog modules
  - External input or internal band gap voltage selectable at negative node
  - Interrupt when compare result change
  - Power down wake up
- EBI (External Bus Interface) for external memory-mapped device access
  - Accessible space: 64KB in 8-bit mode or 128KB in 16-bit mode
  - Supports 8-bit/16-bit data width
  - Supports byte-write in 16-bit data width
- In-System Programming (ISP) and In-Circuit Programming (ICP)
- One built-in temperature sensor with 1℃ resolution
- Brown-Out Detector
  - With 4 levels: 4.3V/3.7V/2.7V/2.2V

3 BLOCK DIAGRAM

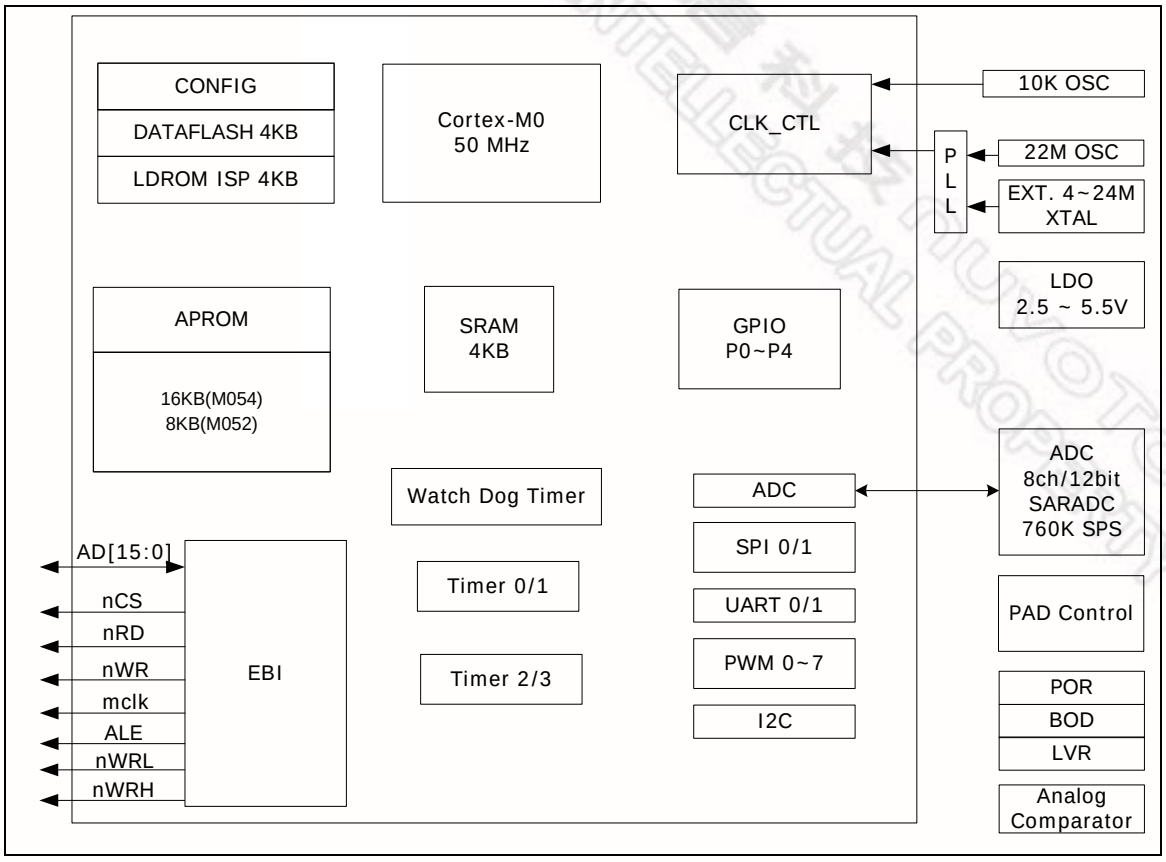


Figure 3-1 NuMicro™ M051 Series Block Diagram

4 SELECTION TABLE

NuMicro M051™ Series Selection Guide

Part number	APROM	RAM	Data Flash	LDROM	I/O	Timer	Connectivity			COMP	PWM	ADC	EBI	ISP ICP	Package
							UART	SPI	I2C						
M052LBN	8KB	4KB	4KB	4KB	40	4x32-bit	2	2	1	2	8	8X12-bit	v	v	LQFP48
M052ZBN	8KB	4KB	4KB	4KB	24	4x32-bit	2	1	1	2	5	8X12-bit		v	QFN33
M054LBN	16KB	4KB	4KB	4KB	40	4x32-bit	2	2	1	2	8	8X12-bit	v	v	LQFP48
M054ZBN	16KB	4KB	4KB	4KB	24	4x32-bit	2	1	1	2	5	8X12-bit		v	QFN33

Table 4-1 NuMicro™ M051 Series Product Selection Guide

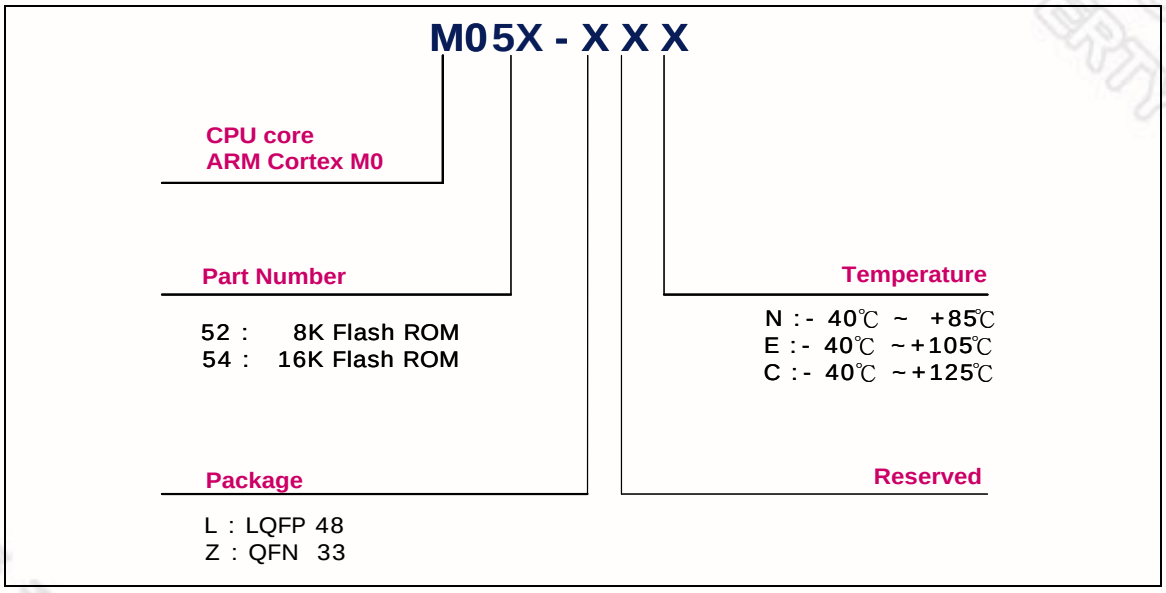


Figure 4-1 NuMicro™ Naming Rule

6 FUNCTIONAL DESCRIPTION

6.1 ARM® Cortex™-M0 Core

The Cortex™-M0 processor is a configurable, multistage, 32-bit RISC processor. It has an AMBA AHB-Lite interface and includes an NVIC component. It also has optional hardware debug functionality. The processor can execute Thumb code and is compatible with other Cortex-M profile processor. The profile supports two modes -Thread and Handler modes. Handler mode is entered as a result of an exception. An exception return can only be issued in Handler mode. Thread mode is entered on Reset, and can be entered as a result of an exception return. Figure 6-1 shows the functional controller of processor.

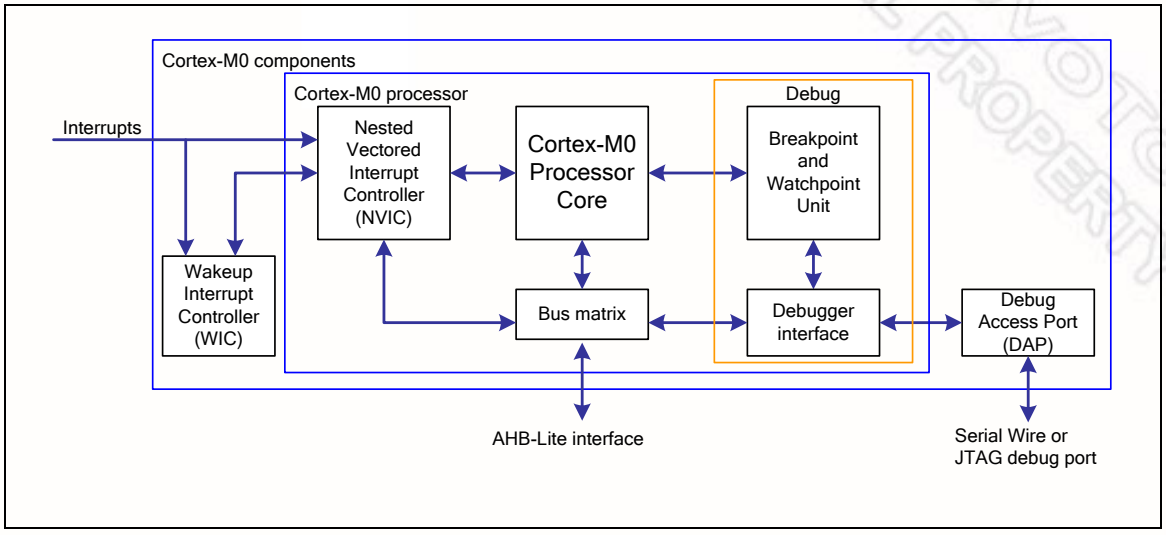


Figure 6-1 Functional Block Diagram

The implemented device provides:

A low gate count processor the features:

- The ARMv6-M Thumb® instruction set.
- Thumb-2 technology.
- ARMv6-M compliant 24-bit SysTick timer.
- A 32-bit hardware multiplier.
- The system interface supports little-endian data accesses.
- The ability to have deterministic, fixed-latency, interrupt handling.

- Load/store-multiples and multicycle-multiplies that can be abandoned and restarted to facilitate rapid interrupt handling.
- C Application Binary Interface compliant exception model.
  This is the ARMv6-M, C Application Binary Interface(C-ABI) compliant exception model that enables the use of pure C functions as interrupt handlers.
- Low power sleep-mode entry using Wait For Interrupt (WFI), Wait For Event(WFE) instructions, or the return from interrupt sleep-on-exit feature.

NVIC features:

- 32 external interrupt inputs, each with four levels of priority.
- Dedicated non-Maskable Interrupt (NMI) input.
- Support for both level-sensitive and pulse-sensitive interrupt lines
- Wake-up Interrupt Controller (WIC), supports ultra-low power sleep mode.

Debug support:

- Four hardware breakpoints.
- Two watchpoints.
- Program Counter Sampling Register (PCSR) for non-intrusive code profiling.
- Single step and vector catch capabilities.

Bus interfaces:

- Single 32-bit AMBA-3 AHB-Lite system interface that provides simple integration to all system peripherals and memory.
- Single 32-bit slave port that supports the DAP (Debug Access Port).

6.2.4 Whole System Memory Map

NuMicro M051™ series provides a 4G-byte address space. The memory locations assigned to each on-chip modules are shown in Table 6-1. The detailed register memory addressing and programming will be described in the following sections for1 individual on-chip peripherals. NuMicro M051™ series only supports little-endian data format.

Address Space	Token	Modules
Flash & SRAM Memory Space		
0x0000_0000 – 0x0000_FFFF	FLASH_BA	FLASH Memory Space (64KB)
0x2000_0000 – 0x2000_0FFF	SRAM_BA	SRAM Memory Space (4KB)
EBI Space (0x6000_0000 ~ 0x6001_FFFF)		
0x6000_0000 – 0x6001_FFFF	EBI_BA	External Memory Space (128KB)
AHB Modules Space (0x5000_0000 – 0x501F_FFFF)		
0x5000_0000 – 0x5000_01FF	GCR_BA	System Global Control Registers
0x5000_0200 – 0x5000_02FF	CLK_BA	Clock Control Registers
0x5000_0300 – 0x5000_03FF	INT_BA	Interrupt Multiplexer Control Registers
0x5000_4000 – 0x5000_7FFF	GPIO_BA	GPIO (P0~P4) Control Registers
0x5000_C000 – 0x5000_FFFF	FMC_BA	Flash Memory Control Registers
0x5001_0000 – 0x5001_03FF	EBI_CTL_BA	EBI Control Registers (128KB)
APB Modules Space (0x4000_0000 ~ 0x400F_FFFF)		
0x4000_4000 – 0x4000_7FFF	WDT_BA	Watch-Dog Timer Control Registers
0x4001_0000 – 0x4001_3FFF	TMR01_BA	Timer0/Timer1 Control Registers
0x4002_0000 – 0x4002_3FFF	I2C_BA	I^2C Interface Control Registers
0x4003_0000 – 0x4003_3FFF	SPI0_BA	SPI0 with master/slave function Control Registers
0x4003_4000 – 0x4003_7FFF	SPI1_BA	SPI1 with master/slave function Control Registers
0x4004_0000 – 0x4004_3FFF	PWMA_BA	PWM0/1/2/3 Control Registers

clear-on-write, decrementing, wrap-on-zero counter with a flexible control mechanism. The counter can be used as a Real Time Operating System (RTOS) tick timer or as a simple counter.

When system timer is enabled, it will count down from the value in the SysTick Current Value Register (SYST_CVR) to zero, and reload (wrap) to the value in the SysTick Reload Value Register (SYST_RVR) on the next clock edge, then decrement on subsequent clocks. When the counter transitions to zero, the COUNTFLAG status bit is set. The COUNTFLAG bit clears on reads.

The SYST_CVR value is UNKNOWN on reset. Software should write to the register to clear it to zero before enabling the feature. This ensures the timer will count from the SYST_RVR value rather than an arbitrary value when it is enabled.

If the SYST_RVR is zero, the timer will be maintained with a current value of zero after it is reloaded with this value. This mechanism can be used to disable the feature independently from the timer enable bit.

For more detailed information, please refer to the documents “ARM® Cortex™-M0 Technical Reference Manual” and “ARM® v6-M Architecture Reference Manual”.

6.4.1.3 Open-Drain Mode Explanation

Set Px_PMD(PMDn[1:0]) to 2'b10 the Px[n] pin is in Open-Drain mode and the I/O pin supports digital output function but only with sink current capability, an additional pull-up resister is needed for driving high state. If the bit value in the corresponding bit [n] of Px_DOUT is "0", the pin drive a "low" output on the pin. If the bit value in the corresponding bit [n] of Px_DOUT is "1", the pin output drives high that is controlled by the internal pull-up resistor or the external pull high resistor.

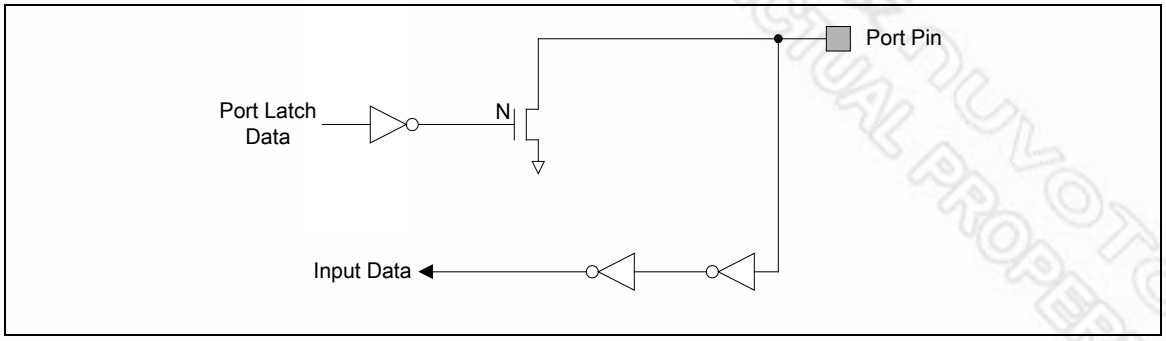
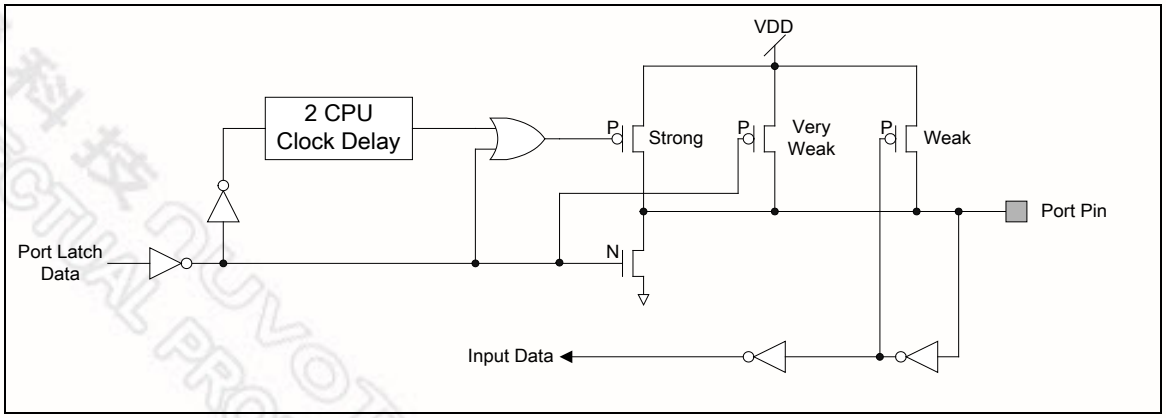


Figure 6-11 Open-Drain Output

6.4.1.4 Quasi-bidirectional Mode Explanation

Set Px_PMD(PMDn[1:0]) to 2'b11 the Px[n] pin is in Quasi-bidirectional mode and the I/O pin supports digital output and input function at the same time but the source current is only up to hundreds uA. Before the digital input function is performed the corresponding bit in Px_DOUT must be set to 1. The quasi-bidirectional output is common on the 80C51 and most of its derivatives. If the bit value in the corresponding bit [n] of Px_DOUT is "0", the pin drive a "low" output on the pin. If the bit value in the corresponding bit [n] of Px_DOUT is "1", the pin will check the pin value. If pin value is high, no action takes. If pin state is low, then pin will drive strong high with 2 clock cycles on the pin and then disable the strong output drive and then the pin status is control by internal pull-up resistor. Note that the source current capability in quasi-bidirectional mode is only about 200uA to 30uA for V_{DD} is form 5.0V to 2.5V



6.8 Timer Controller

6.8.1 Overview

NuMicro M051™ series timer controller includes four 32-bit timers, which allows user to easily implement a timer control for applications. The timer can perform functions like frequency measurement, event counting, interval measurement, clock generation, delay timing, and so on. The timer can generates an interrupt signal upon timeout, or provide the current counting value during operation.

6.8.2 Features:

- 4 sets of 32-bit timers with 24-bit up-timer and one 8-bit pre-scale counter
- Independent clock source for each timer
- Provides one-shot, periodic, toggle and continuous counting operation modes
- Time out period = (Period of timer clock input) * (8-bit pre-scale counter + 1) * (24-bit TCMP)
- Maximum counting cycle time = (1 / T MHz) * (2^8) * (2^{24}), T is the period of timer clock
- 24-bit timer value is readable through TDR (Timer Data Register)
- Support event counting function to count the event from external pin
- Support input capture function to capture or reset counter value

6.10 UART Interface Controller (UART)

NuMicro M051™ series provides two channels of Universal Asynchronous Receiver/Transmitters (UART). UART0~1 performs Normal Speed UART, and support flow control function.

6.10.1 Overview

The Universal Asynchronous Receiver/Transmitter (UART) performs a serial-to-parallel conversion on data received from the peripheral, and a parallel-to-serial conversion on data transmitted from the CPU. The UART controller also supports IrDA SIR Function, LIN master/slave mode function and RS-485 mode functions. Each UART channel supports seven types of interrupts including transmitter FIFO empty interrupt (INT_THRE), receiver threshold level reaching interrupt (INT_RDA), line status interrupt (parity error or framing error or break interrupt) (INT_RLS), receiver buffer time out interrupt (INT_TOUT), MODEM/Wakeup status interrupt (INT_MODEM), Buffer error interrupt (INT_BUF_ERR) and LIN receiver break field detected interrupt (INT_LIN_RX_BREAK).

The UART0 and UART1 are built-in with a 16-byte transmitter FIFO (TX_FIFO) and a 16-byte receiver FIFO (RX_FIFO) that reduces the number of interrupts presented to the CPU. The CPU can read the status of the UART at any time during the operation. The reported status information includes the type and condition of the transfer operations being performed by the UART, as well as 3 error conditions (parity error, framing error, break interrupt) probably occur while receiving data. The UART includes a programmable baud rate generator that is capable of dividing clock input by divisors to produce the serial clock that transmitter and receiver need. The baud rate equation is Baud Rate = UART_CLK / M * [BRD + 2], where M and BRD are defined in Baud Rate Divider Register (UA_BAUD). Table 6-3 lists the equations in the various conditions and Table 6-4 list the UART baud rate setting table.

Mode	DIV_X_EN	DIV_X_ONE	Divider X	BRD	M	Baud rate equation
0	0	0	B	A	16	UART_CLK / [16 * (A+2)]
1	1	0	B	A	B+1	UART_CLK / [(B+1) * (A+2)] , B must >= 8
2	1	1	Don't care	A	1	UART_CLK / (A+2), A must >=3

Table 6-3 UART Baud Rate Equation

The alternate function of UART controllers is LIN (Local Interconnect Network) function. The LIN mode is selected by setting UA_FUN_SEL [1:0] = '01'. In LIN mode, one start bit and 8-bit data format with 1-bit stop bit are required in accordance with the LIN standard.

Another alternate function of UART controllers is RS-485 9 bit mode function, and direction control provided by RTS pin or can program GPIO (P0.3 for RTS0 and P0.1 for RTS1) to implement the function by software. The RS-485 mode is selected by setting the UA_FUN_SEL register to select RS-485 function. The RS-485 driver control is implemented by using the RTS control signal from an asynchronous serial port to enable the RS-485 driver. In RS-485 mode, many characteristics of the RX and TX are same as UART.

6.10.2 Features

- Full duplex, asynchronous communications
- Separate receive / transmit 16/16 bytes entry FIFO for data payloads
- Support hardware auto flow control/flow control function (CTS, RTS) and programmable RTS flow control trigger level
- Programmable receiver buffer trigger level
- Support programmable baud-rate generator for each channel individually
- Support CTS wake up function
- Support 8 bit receiver buffer time out detection function
- Programmable transmitting data delay time between the last stop and the next start bit by setting UA_TOR [DLY] register
- Support break error, frame error, parity error and receive / transmit buffer overflow detect function
- Fully programmable serial-interface characteristics
  - Programmable number of data bit, 5, 6, 7, 8 bit character
  - Programmable parity bit, even, odd, no parity or stick parity bit generation and detection
  - Programmable stop bit, 1, 1.5, or 2 stop bit generation
- Support IrDA SIR function mode
  - Support for 3/16 bit duration for normal mode
- Support LIN function mode
  - Support LIN master/slave mode
  - Support programmable break generation function for transmitter
  - Support break detect function for receiver
- Support RS-485 function mode.
  - Support RS-485 9bit mode
  - Support hardware or software enable to program RTS pin to control RS-485 transmission direction directly

6.11 Analog-to-Digital Converter (ADC)

6.11.1 Overview

NuMicro M051™ series contain one 12-bit successive approximation analog-to-digital converters (SAR A/D converter) with 8 input channels. The A/D converter supports four operation modes: single, burst, single-cycle scan and continuous scan mode. The A/D converters can be started by software and external STADC/P3.2 pin.

6.11.2 Features

- Analog input voltage range: 0~AV_{DD} (Max to 5.0V).
- 12-bit resolution and 10-bit accuracy is guaranteed.
- Up to 8 single-end analog input channels or 4 differential analog input channels.
- Maximum ADC clock frequency is 16 MHz.
- Up to 760k SPS conversion rate.
- Four operating modes
  - Single mode: A/D conversion is performed one time on a specified channel.
  - Single-cycle scan mode: A/D conversion is performed one cycle on all specified channels with the sequence from the lowest numbered channel to the highest numbered channel.
  - Continuous scan mode: A/D converter continuously performs Single-cycle scan mode until software stops A/D conversion.
  - Burst mode: A/D conversion will sample and convert the specified single channel and sequentially store in FIFO.
- An A/D conversion can be started by
  - Software Write 1 to ADST bit
  - External pin STADC
- Conversion results are held in data registers for each channel with valid and overrun indicators.
- Conversion result can be compared with specify value and user can select whether to generate an interrupt when conversion result matches the compare register setting.

- Channel 7 supports 3 input sources: external analog voltage, internal bandgap voltage, and internal temperature sensor output.

6.12 External Bus Interface (EBI)

6.12.1 Overview

NuMicro M051™ series equips an external bus interface (EBI) for external device used.

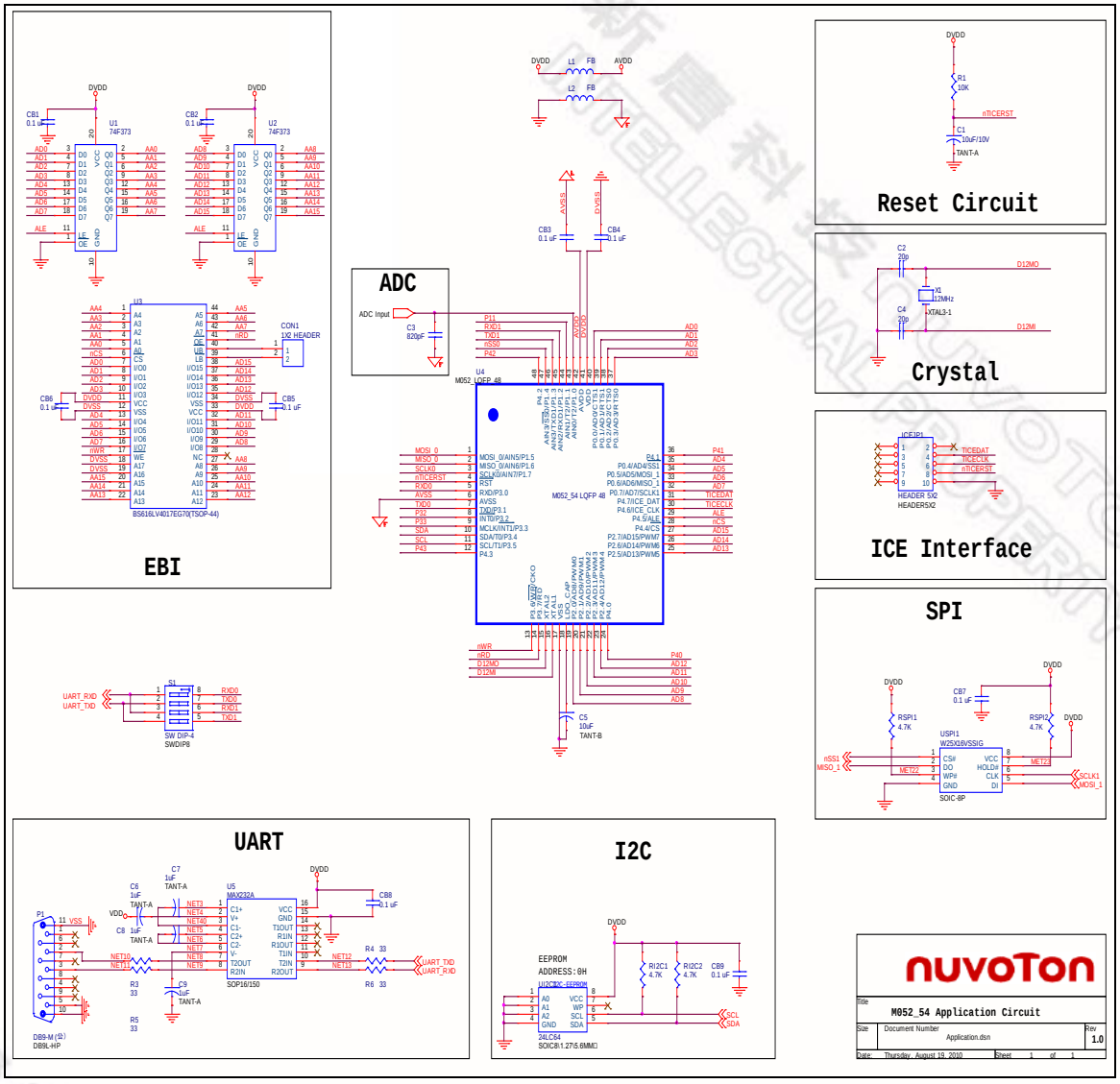
To save the connections between external device and this chip, EBI support address bus and data bus multiplex mode. And, address latch enable (ALE) signal supported differentiate the address and data cycle.

6.12.2 Features

External Bus Interface has the following functions:

1. External devices with max. 64K-byte size (8 bit data width)/128K-byte (16 bit data width) supported
2. Variable external bus base clock (MCLK) supported
3. 8 bit or 16 bit data width supported
4. Variable data access time (tACC), address latch enable time (tALE) and address hold time (tAHD) supported
5. Address bus and data bus multiplex mode supported to save the address pins
6. Configurable idle cycle supported for different access condition: Write command finish (W2X), Read-to-Read (R2R)

7 TYPICAL APPLICATION CIRCUIT



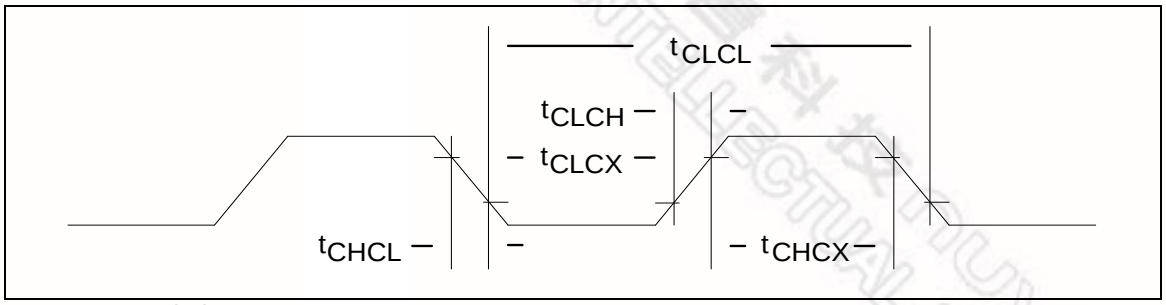
8.2 DC Electrical Characteristics

(V_{DD} -V_{SS}=2.5~5.5V, TA = 25°C, F_{OSC} = 50 MHz unless otherwise specified.)

PARAMETER	SYM.	SPECIFICATION				TEST CONDITIONS
		MIN.	TYP.	MAX.	UNIT	
Operation voltage	V_{DD}	2.5		5.5	V	V_{DD} =2.5V ~ 5.5V up to 50 MHz
LDO Output Voltage	V_{LDO}	1.7	1.8	1.9	V	V_{DD} ≥ 2.5V
Band Gap Analog Input	V_{BG}	-5%	1.20	+5%	V	V_{DD} =2.5V ~ 5.5V
Analog Operating Voltage	AV_{DD}	0		V_{DD}	V	
Analog Reference Voltage	Vref	0		AV_{DD}	V	
Operating Current Normal Run Mode @ 50 MHz	IDD1		20.6		mA	V_{DD} = 5.5V@50MHz, enable all IP and PLL, XTAL=12MHz
	IDD2		14.4		mA	V_{DD} =5.5V@50MHz, disable all IP and enable PLL, XTAL=12MHz
	IDD3		18.9		mA	V_{DD} = 3.3V@50MHz, enable all IP and PLL, XTAL=12MHz
	IDD4		12.8		mA	V_{DD} = 3.3V@50MHz, disable all IP and enable PLL, XTAL=12MHz
Operating Current Normal Run Mode @ 22Mhz	IDD5		6.2		mA	V_{DD} = 5.5V@22MHz, enable all IP and IRC22M, disable PLL
	IDD6		3.4		mA	V_{DD} =5.5V@22MHz, disable all IP and enable IRC22M, disable PLL
	IDD7		6.1		mA	V_{DD} = 3.3V@22MHz, enable all IP and IRC22M, disable PLL
	IDD8		3.4		mA	V_{DD} = 3.3V@22MHz, disable all IP and enable IRC22M, disable PLL
Operating Current Normal Run Mode @ 12Mhz	IDD9		5.3		mA	V_{DD} = 5.5V@12MHz, enable all IP and disable PLL, XTAL=12MHz
	IDD10		3.7		mA	V_{DD} = 5.5V@12MHz, disable all IP and disable PLL, XTAL=12MHz
	IDD11		4.0		mA	V_{DD} = 3.3V@12MHz, enable all IP and disable PLL, XTAL=12MHz

8.3 AC Electrical Characteristics

8.3.1 External Crystal



Note: Duty cycle is 50%.

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNITS	CONDITION
Clock High Time	t_{CHCX}	20	-	-	nS	
Clock Low Time	t_{CLCX}	20	-	-	nS	
Clock Rise Time	t_{CLCH}	-	-	10	nS	
Clock Fall Time	t_{CHCL}	-	-	10	nS	

8.3.2 External Oscillator

PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
Input clock frequency	External crystal	4	12	24	MHz
Temperature	-	-40	-	85	℃
V_{DD}	-	2.5	5	5.5	V
Operating current	12 MHz@ V_{DD} = 5V	-	1	-	mA

8.3.3 Typical Crystal Application Circuits

CRYSTAL	C1	C2
4 MHz ~ 24 MHz	Optional (Depend on crystal specification)	

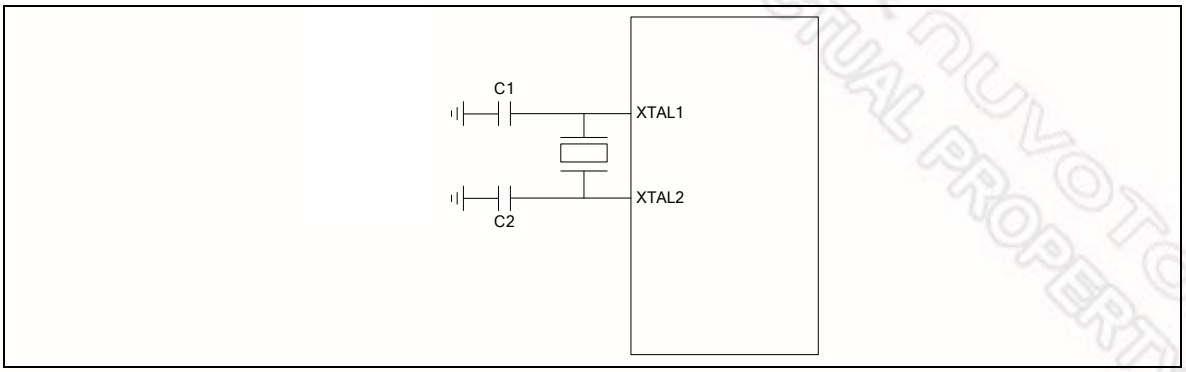


Figure 8-1 Typical Crystal Application Circuit

8.4 Analog Characteristics

8.4.1 Specification of 12-bit SARADC

PARAMETER	SYM.	MIN.	TYP.	MAX.	UNIT
Resolution	-	-	-	12	Bit
Differential nonlinearity error	DNL	-	±1.2	-	LSB
Integral nonlinearity error	INL	-	±1.2	-	LSB
Offset error	EO	-	+3	+5	LSB
Gain error (Transfer gain)	EG	-	-4	-6	-
Monotonic	-		Guaranteed		-
ADC clock frequency	FADC	-	-	16	MHz
Conversion time	TADC	-	13	-	Clock
Sample rate	FS	-	-	760	K SPS
Supply voltage	V_{LDO}	-	1.8	-	V
	VADD	3	-	5.5	V
Supply current (Avg.)	IDD	-	0.5	-	mA
	IDDA	-	1.5	-	mA
Input voltage range	VIN	0	-	AV_{DD}	V
Capacitance	CIN	-	5	-	pF