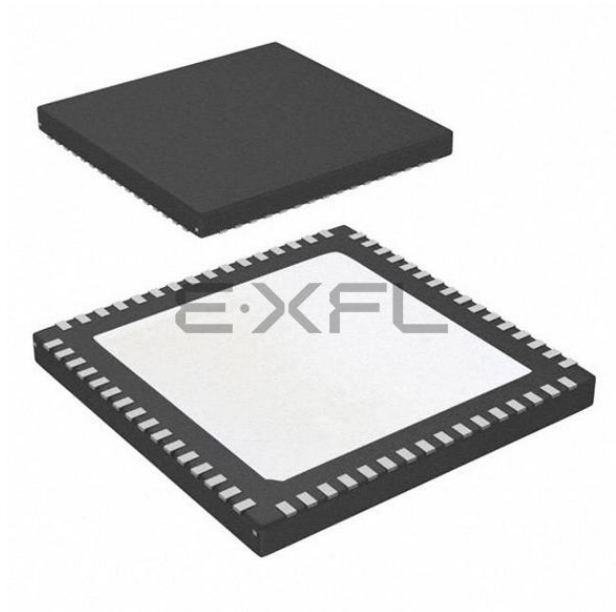
# Renesas Electronics America Inc - R5F10FLCANA#W0 Datasheet



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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Obsolete |
| Core Processor | RL78 |
| Core Size | 16-Bit |
| Speed | 32MHz |
| Connectivity | CSI, I²C, LINbus, UART/USART |
| Peripherals | DMA, LVD, POR, PWM, WDT |
| Number of I/O | 20 |
| Program Memory Size | 32KB (32K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | 4K x 8 |
| RAM Size | 2K x 8 |
| Voltage - Supply (Vcc/Vdd) | 1.6V ~ 5.5V |
| Data Converters | A/D 13x8/12b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 64-WFQFN Exposed Pad |
| Supplier Device Package | 64-WQFN (9x9) |
| Purchase URL | https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f10flcana-w0 |

**Table 1-1 Outline of Functions (Microcontroller Block)** (2/2)

| Item | | 64-pin products | 80-pin products |
|---|---|---|---|
| | | R5F10FLx | R5F10FMx |
| Serial interface | | • 64-pin products<br>CSI: 1 channel / simplified $I^2C$: 1 channel / UART: 1 channel<br>UART: 1 channel<br>CSI: 1 channel / UART (LIN-bus supported): 1 channel<br>• 80-pin products<br>CSI: 1 channel / simplified $I^2C$: 1 channel / UART: 1 channel<br>CSI: 1 channel / simplified $I^2C$: 1 channel / UART: 1 channel<br>CSI: 2 channels / simplified $I^2C$: 1 channel / UART (LIN-bus supported): 1 channel | |
| | $I^2C$ bus | – | |
| Multiplier and divider / multiply accumulator | | Multiplier: 16 bits × 16 bits (Unsigned or signed)<br>Divider: 32 bits ÷ 32 bits (Unsigned)<br>Multiply accumulator: 16 bits × 16 bits + 32 bits (Unsigned or signed) | |
| DMA controller | | 2 channels | |
| Vectored interrupt sources | Internal | 25 | |
| | External | 2 | 5 |
| Key interrupt | | 4 ch (7) Note 1 | 4 ch (8) Note 1 |
| Reset | | • Reset by $\overline{\text{RESET}}$ pin<br>• Internal reset by watchdog timer<br>• Internal reset by power-on-reset<br>• Internal reset by voltage detector<br>• Internal reset by illegal instruction execution Note 2<br>• Internal reset by RAM parity error<br>• Internal reset by illegal-memory access | |
| Power-on-reset circuit | | • Power-on-reset: 1.51 ±0.03 V<br>• Power-down-reset: 1.50 ±0.03 V | |
| Voltage detector | | Detection level: 3 stages | |
| On-chip debug function | | Provided | |

<R>

**Notes 1.** The number in parentheses is the channels of key interrupt when using the peripheral I/O redirection register (PIOR).

**2.** The illegal instruction is generated when instruction code FFH is executed. Rest by the illegal instruction execution is not issued by emulation with the in-circuit emulator or on-chip debug emulator.

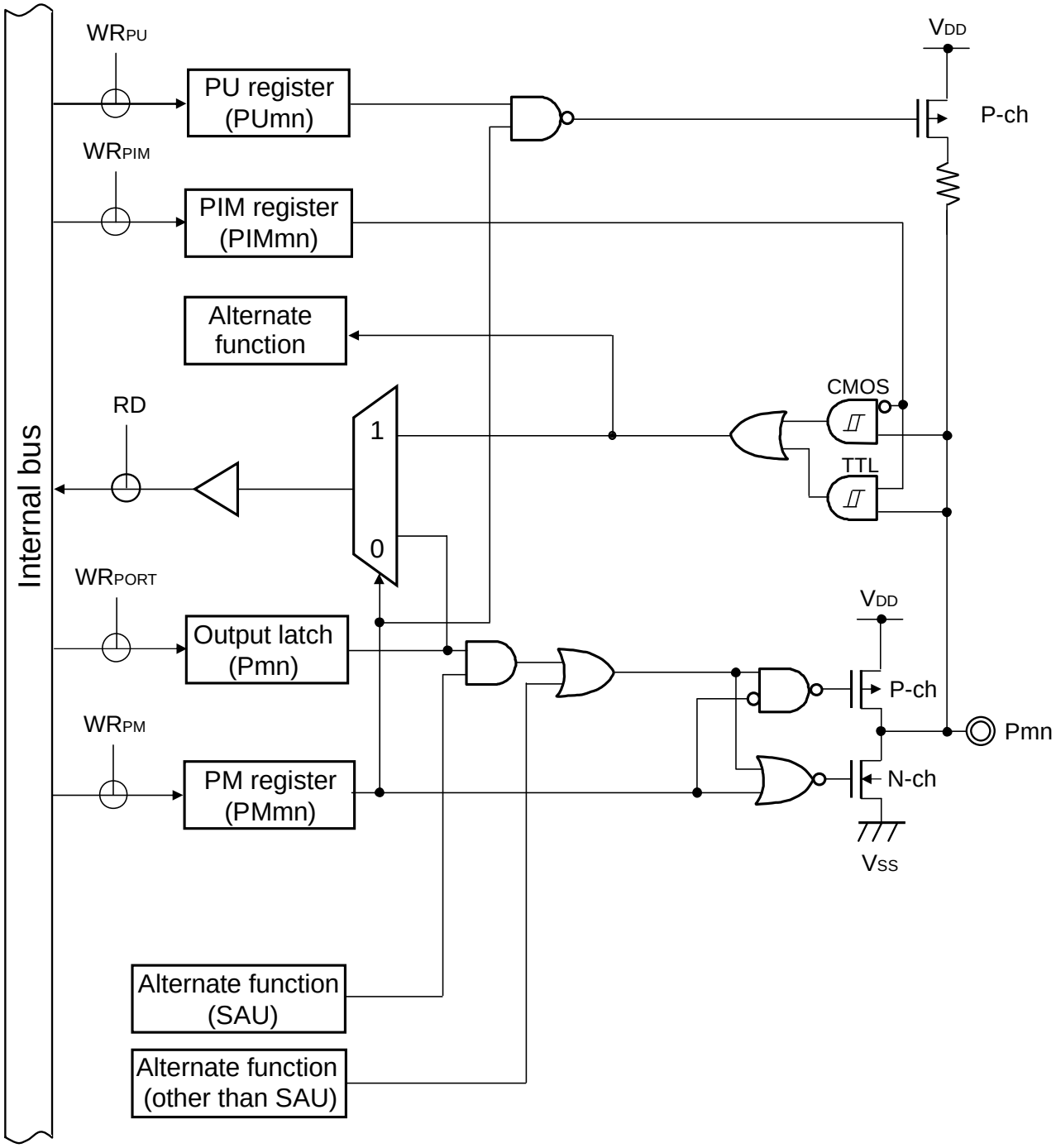
(2/3)

<R>

| Function Name | RL78/G1E (64-pin) | RL78/G1E (80-pin) | RL78/G1A (64-pin) |
|---|---|---|---|
| KR0 | √ | √ | √ |
| KR1 | √ | √ | √ |
| KR2 | √ | √ | √ |
| KR3 | √ | √ | √ |
| KR4 | (√) | (√) | √ |
| KR5 | (√) | (√) | √ |
| KR6 | (√) | (√) | √ |
| KR7 | – | (√) | √ |
| KR8 | – | – | √ |
| KR9 | – | – | √ |
| PCLBUZ0 | – | √ | √ |
| PCLBUZ1 | – | – | √ |
| REGC | √ | √ | √ |
| RTC1HZ | – | – | √ |
| $\overline{\text{RESET}}$ | √ | √ | √ |
| RXD0 | √ | √ | √ |
| RXD1 | √ | √ | √ |
| RXD2 | √ | √ | √ |
| SCK00 | √ | √ | √ |
| SCK01 | – | – | √ |
| SCK10 | – | √ | √ |
| SCK11 | – | – | √ |
| SCK20 | – | √ | √ |
| SCK21 | √ | √ | √ |
| SCLA0 | – | – | √ |
| SCL00 | √ | √ | √ |
| SCL01 | – | – | √ |
| SCL10 | – | √ | √ |
| SCL11 | – | – | √ |
| SCL20 | – | √ | √ |
| SCL21 | – | – | √ |
| SDAA0 | – | – | √ |
| SDA00 | √ | √ | √ |
| SDA01 | – | – | √ |
| SDA10 | – | √ | √ |
| SDA11 | – | – | √ |
| SDA20 | – | √ | √ |
| SDA21 | – | – | √ |
| SI00 | √ | √ | √ |
| SI01 | – | – | √ |
| SI10 | – | √ | √ |
| SI11 | – | – | √ |
| SI20 | – | √ | √ |
| SI21 | √ | √ | √ |

<R> **Remark** Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR).

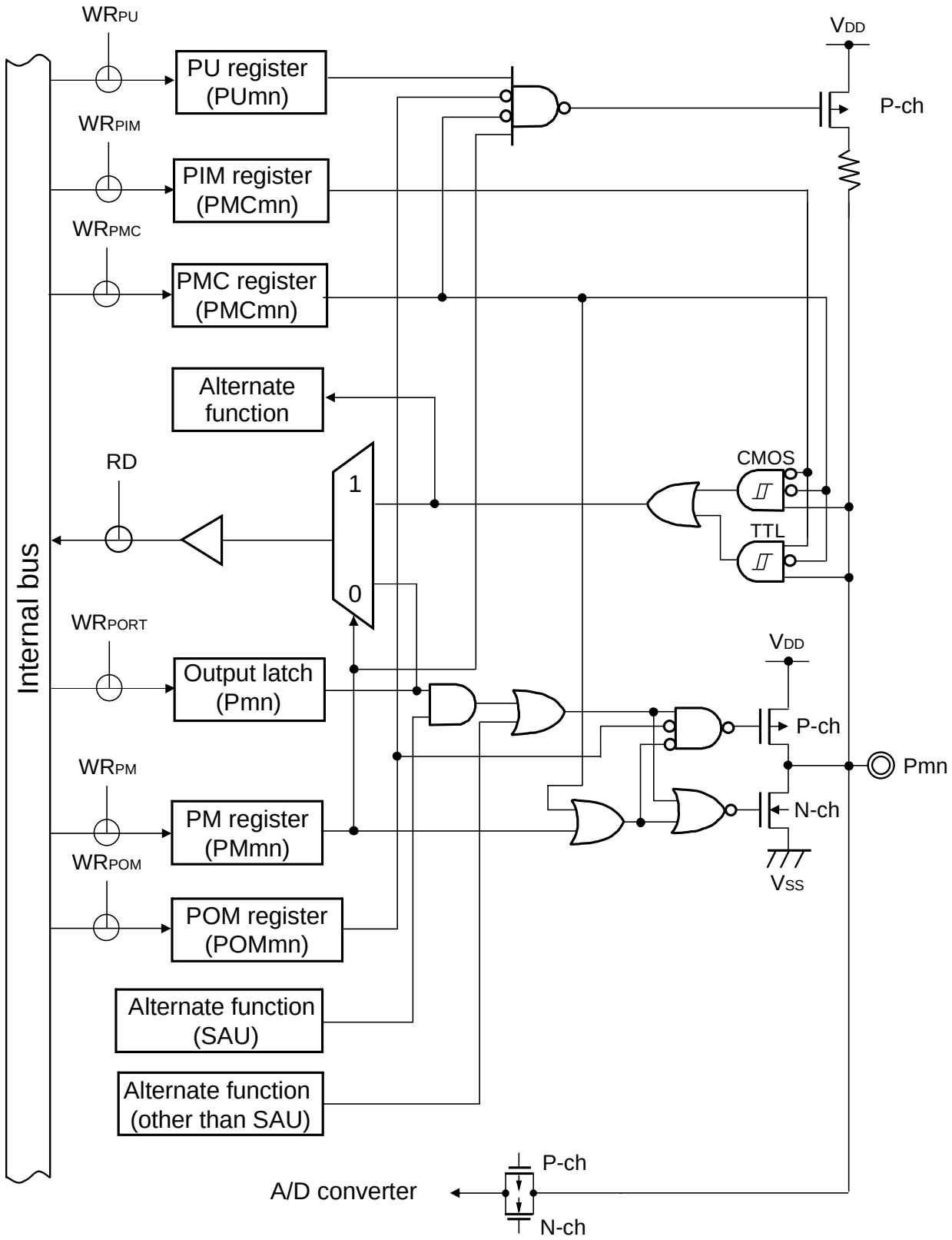
<R> **Figure 2-10. Pin Block Diagram for Pin Type 8-1-1**




**Remarks 1.** For alternate functions, see **2. 1. 1 Port functions**.

**2.** SAU: Serial array unit

<R> **Figure 2-12. Pin Block Diagram for Pin Type 8-3-2**




**Remarks 1.** For alternate functions, see **2. 1. 1 Port functions**.

**2.** SAU: Serial array unit

### 2. 5. 8 Port 13 (P130, P137)

**(1) Port mode**

P130 functions as an output port.

P137 functions as an input port.

**(2) Control mode**

P137 functions as external interrupt request input.

**(a) INTP0**

This is an external interrupt request input pin for which the valid edge (rising edge, falling edge, or both rising and falling edges) can be specified.

### 3. 4. 3. 1 Port mode register (PMxx)

#### (1) 64-pin products

| Symbol | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | Address | After Reset | R/W |
|---|---|---|---|---|---|---|---|---|---|---|---|
| PM0 | 1 | PM06 | PM05 | PM04 | PM03 | PM02 | PM01 | PM00 | FFF20H | FFH | R/W |
| PM1 | 1 | PM16 | 1 | PM14 | PM13 | PM12 | PM11 | PM10 | FFF21H | FFH | R/W |
| PM2 | PM27 | PM26 | PM25 | PM24 | PM23 | PM22 | PM21 | PM20 | FFF22H | FFH | R/W |
| PM4 | 1 | 1 | 1 | 1 | PM43 | PM42 | PM41 | PM40 | FFF24H | FFH | R/W |
| PM6 | 1 | 1 | 1 | 1 | PM63 | PM62 | PM61 | PM60 | FFF26H | FFH | R/W |
| PM7 | PM77 | PM76 | PM75 | PM74 | PM73 | PM72 | PM71 | PM70 | FFF27H | FFH | R/W |
| PM14 | 1 | 1 | 1 | 1 | 1 | 1 | PM141 | PM140 | FFF2EH | FFH | R/W |
| PM15 | 1 | 1 | 1 | PM154 | PM153 | PM152 | PM151 | PM150 | FFF2FH | FFH | R/W |

**Cautions 1. Be sure to clear bits 4 to 6 of the PM0 register, bit 6 of the PM1 register, bits 4 to 7 of the PM2 register, bit 3 of the PM4 register, bits 0 to 3 of the PM6 register, bits 4 to 7 of the PM7 register, bits 0 and 1 of the PM14 register, and bits 0 to 4 of the PM15 register to “0”.**

**2. Be sure to set bit 7 of the PM0 register, bits 5 and 7 of the PM1 register, bits 4 to 7 of the PM4 register, bits 4 to 7 of the PM6 register, bits 2 to 7 of the PM14 register, and bits 5 to 7 of the PM15 register to “1”.**

#### (2) 80-pin products

| Symbol | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | Address | After Reset | R/W |
|---|---|---|---|---|---|---|---|---|---|---|---|
| PM0 | 1 | PM06 | PM05 | PM04 | PM03 | PM02 | PM01 | PM00 | FFF20H | FFH | R/W |
| PM1 | 1 | PM16 | PM15 | PM14 | PM13 | PM12 | PM11 | PM10 | FFF21H | FFH | R/W |
| PM2 | PM27 | PM26 | PM25 | PM24 | PM23 | PM22 | PM21 | PM20 | FFF22H | FFH | R/W |
| PM4 | 1 | 1 | 1 | 1 | PM43 | PM42 | PM41 | PM40 | FFF24H | FFH | R/W |
| <R> PM5 | 1 | 1 | 1 | 1 | 1 | 1 | PM51 | PM50 | FFF25H | FFH | R/W |
| PM6 | 1 | 1 | 1 | 1 | PM63 | PM62 | PM61 | PM60 | FFF26H | FFH | R/W |
| PM7 | PM77 | PM76 | PM75 | PM74 | PM73 | PM72 | PM71 | PM70 | FFF27H | FFH | R/W |
| PM14 | 1 | 1 | 1 | 1 | 1 | 1 | PM141 | PM140 | FFF2EH | FFH | R/W |
| PM15 | 1 | 1 | 1 | PM154 | PM153 | PM152 | PM151 | PM150 | FFF2FH | FFH | R/W |

**Cautions 1. Be sure to clear bits 5 and 6 of the PM0 register, bit 6 of the PM1 register, bits 5 to 7 of the PM2 register, bit 3 of the PM4 register, bits 0 to 3 of the PM6 register, bits 4 to 7 of the PM7 register, bit 1 of the PM14 register, and bits 0 to 4 of the PM15 register to “0”.**

**2. Be sure to set bit 7 of the PM0 register, bit 7 of the PM1 register, bits 4 to 7 of the PM4 register,**
<R> **bits 2 to 7 of the PM5 register, bits 4 to 7 of the PM6 register, bits 2 to 7 of the PM14 register, and bits 5 to 7 of the PM15 register to “1”.**

## 3. 6 Timer Array Unit

In this section, the differences of the functions and registers from RL78/G1A (64-pin products) are described. For details, see **CHAPTER 6 TIMER ARRAY UNIT** in **RL78/G1A Hardware User's Manual (R01UH0305E)**.

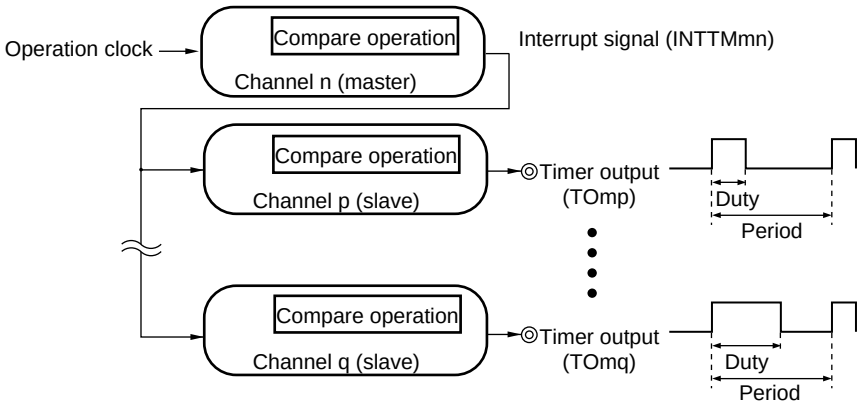
The timer array unit is provided in all products (Unit 0, Channels 0 to 7).

| Units | Channels | 64-pin products, 80-pin products |
|---|---|---|
| Unit 0 | Channel 0 | √ |
| | Channel 1 | √ |
| | Channel 2 | √ |
| | Channel 3 | √ |
| | Channel 4 | √ |
| | Channel 5 | √ |
| | Channel 6 | √ |
| | Channel 7 | √ |

**Caution Most of the following descriptions in this section use the case of 80-pin products as an example.**

<3> Multiple PWM (Pulse Width Modulation) output

By extending the PWM function and using one master channel and two or more slave channels, up to seven types of PWM signals that have a specific period and a specified duty factor can be generated.




**Caution For details about the rules of simultaneous channel operation function, see 3. 6. 4 Basic rules of timer array unit.**

**Remark** m: Unit number (m = 0), n: Channel number (n = 0 to 7 (however, timer input pin (TImn) , timer output pin (TOmn) : n = 0, 4, 7)), p, q: Slave channel number (4, 7)

### 3. 6. 1. 3 8-bit timer operation function (channels 1 and 3 only)

The 8-bit timer operation function makes it possible to use a 16-bit timer channel in a configuration consisting of two 8-bit timer channels. This function can only be used for channels 1 and 3.

**Caution There are several rules for using 8-bit timer operation function. For details, see 3. 6. 4 Basic rules of timer array unit.**

### 3. 6. 2 Configuration of timer array unit

Timer array unit includes the following hardware.

**Table 3-8. Configuration of Timer Array Unit**

| Item | Configuration |
|---|---|
| Timer/counter | Timer count register mn (TCRmn) |
| Register | Timer data register mn (TDRmn) |
| Timer input | TI00, TI04, TI07, RxD2 pin (for LIN-bus) |
| Timer output | TO00, TO04, TO07, output controller |
| Control registers | <Registers of unit setting block><br>• Peripheral enable register 0 (PER0)<br>• Timer clock select register m (TPSm)<br>• Timer channel enable status register m (TEm)<br>• Timer channel start register m (TSm)<br>• Timer channel stop register m (TTm)<br>• Timer input select register 0 (TIS0)<br>• Timer output enable register m (TOEm)<br>• Timer output register m (TOm)<br>• Timer output level register m (TOLm)<br>• Timer output mode register m (TOMm) |
| | <Registers of each channel><br>• Timer mode register mn (TMRmn)<br>• Timer status register mn (TSRmn)<br>• Input switch control register (ISC)<br>• Noise filter enable register 1 (NFEN1)<br>• Port mode control register (PMCxx)<br>• Port mode register (PMxx)<br>• Port register (Pxx) |

**Remark** m: Unit number (m = 0), n: Channel number (n = 0 to 7)

The presence or absence of timer I/O pins in each timer array unit channel is as follows.

**Table 3-9. Timer I/O Pins provided in Each Product**

| Timer array unit channels | | 64-pin products, 80-pin products |
|---|---|---|
| Unit 0 | Channel 0 | P00/TI00, P01/TO00 |
| | Channel 1 | – |
| | Channel 2 | – |
| | Channel 3 | – |
| | Channel 4 | P42/TI04/TO04 |
| | Channel 5 | – |
| | Channel 6 | – |
| | Channel 7 | P41/TI07/TO07 |

**Remarks 1.** When timer input and timer output are shared by the same pin, either only timer input or only timer output can be used.

**2.** –: here is no timer I/O pin, but the channel is available. (However, the channel can only be used as an interval timer.)

Figures 3-3 show the block diagrams of the timer array unit of the 80-pin products.

### 3. 12. 1 Functions of serial array unit

Each serial interface supported by the RL78/G1E (64-pin products, 80-pin products) has the following features.

#### 3. 12. 1. 1 3-wire serial I/O (CSI00, CSI10, CSI20, CSI21)

Data is transmitted or received in synchronization with the serial clock (SCK) output from the master channel.

3-wire serial communication is clocked communication performed by using three communication lines: one for the serial clock (SCK), one for transmitting serial data (SO), one for receiving serial data (SI).

For details about the settings, see **3. 12. 5 Operation of 3-Wire serial I/O (CSI00, CSI10, CSI20, CSI21) Communication**.

[Data transmission/reception]

- Data length of 7 or 8 bits
- Phase control of transmit/receive data
- MSB/LSB first selectable
- Level setting of transmit/receive data

[Clock control]

- Master/slave selection
- Phase control of I/O clock
- Setting of transfer period by prescaler and internal counter of each channel
- Maximum transfer rate During master communication (CSI00): Max. $f_{CLK}/2$ **Note**
  During master communication (other than CSI00): Max. $f_{CLK}/4$ **Note**
  During slave communication: Max. $f_{MCK}/6$ **Note**

[Interrupt function]

- Transfer end interrupt/buffer empty interrupt

[Error detection flag]

- Overrun error

In addition, CSI00 of following channels supports the SNOOZE mode. When SCK input is detected while in the STOP mode, the SNOOZE mode makes data reception that does not require the CPU possible. Only CSI00 can be specified for asynchronous reception.

**Note** Use the clocks within a range satisfying the SCK cycle time ($t_{KCY}$) characteristics (see **CHAPTER 5 ELECTRICAL SPECIFICATIONS**).

## 3. 17 Key Interrupt Function

The number of key interrupt input channels differs, depending on the product.

| | 64-pin products | 80-pin products |
|---|---|---|
| Key interrupt input channels | 4 ch (7 ch) | 4 ch (8 ch) |

**Remarks 1.** Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR).

**2.** Most of the following descriptions in this section use the case of 80-pin products as an example.

### 3. 17. 1 Functions of key interrupt

A key interrupt (INTKR) can be generated by inputting a rising/falling edge to the key interrupt input pins (KR0 to KR7).

There are two ways to identify the channel(s) to which a valid edge has been input:

- Identify the channel(s) (KR0 to KR7) by using the port input level.
- Identify the channel(s) (KR0 to KR5) by using the key interrupt flag.

**Table 3-16. Assignment of Key Interrupt Detection Pins**

| Key Interrupt Pins | Key return mode register (KRM0) | Key return flag register (KRF) |
|---|---|---|
| KR0 | KRM00 | KRF0 |
| KR1 | KRM01 | KRF1 |
| KR2 | KRM02 | KRF2 |
| KR3 | KRM03 | KRF3 |
| KR4 | KRM04 | KRF4 |
| KR5 | KRM05 | KRF5 |
| KR6 | KRM06 | – |
| KR7 | KRM07 | – |

**Remark** KR0 to KR3 (KR0 to KR6): 64-pin products
KR0 to KR3 (KR0 to KR7): 80-pin products
Functions in parentheses can be assigned via settings in the peripheral I/O redirection register (PIOR)

**(5) Gain control register 1 (GC1)**

This register is used to specify the gain and feedback resistance of configurable amplifier Ch1.

The value to specify depends on the configuration of configurable amplifier Ch1.

When using configurable amplifiers Ch1 to Ch3 together as an instrumentation amplifier, be sure to set gain control register 1 (GC1) to 03H.

Reset signal input clears this register to 00H.

Address: 06H After reset: 00H R/W

| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| GC1 | 0 | 0 | 0 | AMPG14 | AMPG13 | AMPG12 | AMPG11 | AMPG10 |

**Table 4-1. Gain of Configurable Amplifier Ch1 (Non-Inverting Amplifier)**

| AMPG14 | AMPG13 | AMPG12 | AMPG11 | AMPG10 | Gain of Configurable Amplifier Ch1 (Typ.) |
|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 9.5 dB |
| 0 | 0 | 0 | 0 | 1 | 10.9 dB |
| 0 | 0 | 0 | 1 | 0 | 12.4 dB |
| 0 | 0 | 0 | 1 | 1 | 14.0 dB |
| 0 | 0 | 1 | 0 | 0 | 15.6 dB |
| 0 | 0 | 1 | 0 | 1 | 17.3 dB |
| 0 | 0 | 1 | 1 | 0 | 19.0 dB |
| 0 | 0 | 1 | 1 | 1 | 20.8 dB |
| 0 | 1 | 0 | 0 | 0 | 22.7 dB |
| 0 | 1 | 0 | 0 | 1 | 24.5 dB |
| 0 | 1 | 0 | 1 | 0 | 26.4 dB |
| 0 | 1 | 0 | 1 | 1 | 28.3 dB |
| 0 | 1 | 1 | 0 | 0 | 30.3 dB |
| 0 | 1 | 1 | 0 | 1 | 32.2 dB |
| 0 | 1 | 1 | 1 | 0 | 34.2 dB |
| 0 | 1 | 1 | 1 | 1 | 36.1 dB |
| 1 | 0 | 0 | 0 | 0 | 38.1 dB |
| 1 | 0 | 0 | 0 | 1 | 40.1 dB |
| Other than above | | | | | Setting prohibited |

<R> **Remark** Bits 7 to 5 are fixed at 0 of read only.

# CHAPTER 5 ELECTRICAL SPECIFICATIONS

In this capter, the electrical specification is described for the target products shown below.

Target products A: Consumer applications $T_A$ = −40 to +85°C
R5F10FLCANA, R5F10FLCANA, R5F10FLDANA, R5F10FLDANA,
R5F10FLEANA, R5F10FLEANA, R5F10FMCAFB, R5F10FMCAFB,
R5F10FMDAFB, R5F10FMDAFB, R5F10FMEAFB, R5F10FMEAFB

Target products D: Industrial applications $T_A$ = −40 to +85°C
R5F10FLCDNA, R5F10FLCDNA, R5F10FLDDNA, R5F10FLDDNA,
R5F10FLEDNA, R5F10FLEDNA, R5F10FMCDFB, R5F10FMCDFB,
R5F10FMDDFB, R5F10FMDDFB, R5F10FMEDFB, R5F10FMEDFB

**Cautions 1. The RL78/G1E microcontrollers have an on-chip debug function, which is provided for development and evaluation. Do not use the on-chip debug function in products designated for mass production, because the guaranteed number of rewritable times of the flash memory may be exceeded when this function is used, and product reliability therefore cannot be guaranteed. Renesas Electronics is not liable for problems occurring when the on-chip debug function is used.**

**2. The pins mounted depend on the product, so that refer to CHAPTER 2 PIN FUNCTIONS. In this Chapter, most of the descriptions use the case of 80-pin products as an example.**

**Notes 1.** Total current flowing into $V_{DD}$, including the input leakage current flowing when the level of the input pin is fixed to $V_{DD}$ or $V_{SS}$. The values below the MAX. column include the peripheral operation current. However, not including the current flowing into the A/D converter, LVD circuit, I/O port, on-chip pullup/pull-down resistors, and data flash rewriting.

**2.** When the HALT instruction is executed for the flash memory.

**3.** When the high-speed on-chip oscillator is stopped.

**4.** When the high-speed system clock is stopped.

**5.** Not including the current flowing into 12-bit interval timer, watchdog timer.

**6.** The relationship between the operation voltage range, CPU operating frequency, and operating mode is as below.

| | |
|---|---|
| HS (High-speed main) mode: | $V_{DD}$ = 2.7 to 5.5 V @ 1 MHz to 32 MHz |
| | $V_{DD}$ = 2.4 to 5.5 V @ 1 MHz to 16 MHz |
| LS (Low-speed main) mode: | $V_{DD}$ = 1.8 to 5.5 V @ 1 MHz to 8 MHz |
| LV (Low-voltage main) mode: | $V_{DD}$ = 1.6 to 5.5 V @ 1 MHz to 4 MHz |

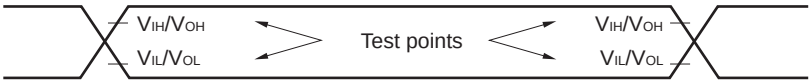
**Remarks 1.** $f_{MX}$: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)

**2.** $f_{IH}$: High-speed on-chip oscillator clock frequency

**3.** The TYP. temperature condition in modes other than STOP mode is $T_A$ = 25°C.

## <R> 5. 2. 4 Peripheral functions characteristics

### AC Timing Test Points




### <R> 5. 2. 4. 1 Serial array unit

#### (1) Communication between devices at same potential (UART mode) (dedicated baud rate generator output)

($T_A$ = –40 to +85°C, 1.6 V ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = 0 V)

| Parameter | Symbol | Conditions | HS Note 1 | | LS Note 2 | | LV Note 3 | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | MIN. | MAX. | MIN. | MAX. | MIN. | MAX. | |
| Transfer rate Note 4 | | 2.4 V ≤ $V_{DD}$ ≤ 5.5 V | | $f_{MCK}$/6 | | $f_{MCK}$/6 | | $f_{MCK}$/6 | bps |
| | | Theoretical value of the maximum transfer rate: $f_{MCK}$ = $f_{CLK}$ Note 6 | | 5.3 Note 5 | | 1.3 | | 0.6 | Mbps |
| | | 1.8 V ≤ $V_{DD}$ ≤ 5.5 V | | $f_{MCK}$/6 | | $f_{MCK}$/6 | | $f_{MCK}$/6 | bps |
| | | Theoretical value of the maximum transfer rate: $f_{MCK}$ = $f_{CLK}$ Note 6 | | 5.3 Note 5 | | 1.3 | | 0.6 | Mbps |
| | | 1.7 V ≤ $V_{DD}$ ≤ 5.5 V | | $f_{MCK}$/6 | | $f_{MCK}$/6 | | $f_{MCK}$/6 | bps |
| | | Theoretical value of the maximum transfer rate: $f_{MCK}$ = $f_{CLK}$ Note 6 | | 5.3 Note 5 | | 1.3 Note 5 | | 0.6 | Mbps |
| | | 1.6 V ≤ $V_{DD}$ ≤ 5.5 V | | – | | $f_{MCK}$/6 | | $f_{MCK}$/6 | bps |
| | | Theoretical value of the maximum transfer rate: $f_{MCK}$ = $f_{CLK}$ Note 6 | | – | | 1.3 Note 5 | | 0.6 | Mbps |

**Notes 1.** HS is condition of HS (high-speed main) mode.

**2.** LS is condition of LS (low-speed main) mode.

**3.** LV is condition of LV (low-voltage main) mode.

**4.** Transfer rate in the SNOOZE mode is 4800 bps.

**5.** The following conditions are required for low voltage interface.
2.4 V ≤ $V_{DD}$ < 2.7 V: 2.6 Mbps max.
1.8 V ≤ $V_{DD}$ < 2.4 V: 1.3 Mbps max.
1.6 V ≤ $V_{DD}$ < 1.8 V: 0.6 Mbps max.

**6.** $f_{CLK}$ in each operating mode is as below.
HS (high-speed main) mode : $f_{CLK}$ = 32 MHz
LS (low-speed main) mode : $f_{CLK}$ = 8 MHz
LV (low-voltage main) mode : $f_{CLK}$ = 4 MHz

**Caution Select the normal input buffer for the RxDq pin and the normal output mode for the TxDq pin by using port input mode register g (PIMg) and port output mode register g (POMg).**

<R> **(10) Communication between devices at different potential (1.8 V, 2.5 V or 3 V) (simplified $I^2C$ mode) (1/2)**

($T_A$ = –40 to +85°C, 1.8 V ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = 0 V) (1/2)

| Parameter | Symbol | Conditions | HS Note 1 | | LS Note 2 | | LV Note 3 | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | MIN. | MAX. | MIN. | MAX. | MIN. | MAX. | |
| SCLr clock frequency | $f_{SCL}$ | 4.0 V ≤ $V_{DD}$ ≤ 5.5 V, 2.7 V ≤ Vb ≤ 4.0 V, Cb = 50 pF, Rb = 2.7 kΩ | | 1000 Note 4 | | 300 Note 4 | | 300 Note 4 | kHz |
| | | 2.7 V ≤ $V_{DD}$ ≤ 4.0 V, 2.3 V ≤ Vb ≤ 2.7 V, Cb = 50 pF, Rb = 2.7 kΩ | | 1000 Note 4 | | 300 Note 4 | | 300 Note 4 | kHz |
| | | 4.0 V ≤ $V_{DD}$ ≤ 5.5 V, 2.7 V ≤ Vb ≤ 4.0 V, Cb = 100 pF, Rb = 2.8 kΩ | | 400 Note 4 | | 300 Note 4 | | 300 Note 4 | kHz |
| | | 2.7 V ≤ $V_{DD}$ ≤ 4.0 V, 2.3 V ≤ Vb ≤ 2.7 V, Cb = 100 pF, Rb = 2.7 kΩ | | 400 Note 4 | | 300 Note 4 | | 300 Note 4 | kHz |
| | | 1.8 V ≤ $V_{DD}$ < 3.3 V, 1.6 V ≤ Vb ≤ 2.0 V Note 5, Cb = 100 pF, Rb = 5.5 kΩ | | 300 Note 4 | | 300 Note 4 | | 300 Note 4 | kHz |
| Hold time when SCLr = L | $t_{LOW}$ | 4.0 V ≤ $V_{DD}$ ≤ 5.5 V, 2.7 V ≤ Vb ≤ 4.0 V, Cb = 50 pF, Rb = 2.7 kΩ | 475 | | 1550 | | 1550 | | ns |
| | | 2.7 V ≤ $V_{DD}$ ≤ 4.0 V, 2.3 V ≤ Vb ≤ 2.7 V, Cb = 50 pF, Rb = 2.7 kΩ | 475 | | 1550 | | 1550 | | ns |
| | | 4.0 V ≤ $V_{DD}$ ≤ 5.5 V, 2.7 V ≤ Vb ≤ 4.0 V, Cb = 100 pF, Rb = 2.8 kΩ | 1150 | | 1550 | | 1550 | | ns |
| | | 2.7 V ≤ $V_{DD}$ ≤ 4.0 V, 2.3 V ≤ Vb ≤ 2.7 V, Cb = 100 pF, Rb = 2.7 kΩ | 1150 | | 1550 | | 1550 | | ns |
| | | 1.8 V ≤ $V_{DD}$ < 3.3 V, 1.6 V ≤ Vb ≤ 2.0 V Note 5, Cb = 100 pF, Rb = 5.5 kΩ | 1550 | | 1550 | | 1550 | | ns |
| Hold time when SCLr = H | $t_{HIGH}$ | 4.0 V ≤ $V_{DD}$ ≤ 5.5 V, 2.7 V ≤ Vb ≤ 4.0 V, Cb = 50 pF, Rb = 2.7 kΩ | 245 | | 610 | | 610 | | ns |
| | | 2.7 V ≤ $V_{DD}$ ≤ 4.0 V, 2.3 V ≤ Vb ≤ 2.7 V, Cb = 50 pF, Rb = 2.7 kΩ | 200 | | 610 | | 610 | | ns |
| | | 4.0 V ≤ $V_{DD}$ ≤ 5.5 V, 2.7 V ≤ Vb ≤ 4.0 V, Cb = 100 pF, Rb = 2.8 kΩ | 675 | | 610 | | 610 | | ns |
| | | 2.7 V ≤ $V_{DD}$ ≤ 4.0 V, 2.3 V ≤ Vb ≤ 2.7 V, Cb = 100 pF, Rb = 2.7 kΩ | 600 | | 610 | | 610 | | ns |
| | | 1.8 V ≤ $V_{DD}$ < 3.3 V, 1.6 V ≤ Vb ≤ 2.0 V Note 5, Cb = 100 pF, Rb = 5.5 kΩ | 610 | | 610 | | 610 | | ns |

(**Notes** are listed on the next page.)

**Note** Total current flowing to internal power supply pins $AV_{DD1}$, $AV_{DD2}$, $AV_{DD3}$, and $DV_{DD}$. Current flowing through the pull-up resistor is not included. The input leakage current flowing when the level of the input pin is fixed to $AV_{DD1}$, $AV_{DD2}$, $AV_{DD3}$ or $DV_{DD}$, or AGND1, AGND2, AGND3, AGND4, or DGND is included. See the table below to check the definition of those symbols of the current flowing.

| Parameter | Symbol | Analog function with power on | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Configurable amplifier | | | Gain adjustment amplifier | D/A converter | | | | Low-pass filter | High-pass filter | Temperature sensor | Variable output voltage regulator |
| | | Ch1 | Ch2 | Ch3 | | Ch1 | Ch2 | Ch3 | Ch4 | | | | |
| Supply current | Im111 Note 1 | ON | ON | ON | – | – | – | ON | – | – | – | – | – |
| | Im112 Note 1 | ON | ON | ON | ON | ON | ON | ON | ON | – | – | ON | ON |
| | Im113 Note 1 | ON | ON | ON | – | ON | ON | ON | ON | ON | ON | ON | ON |
| | Im114 Note1 | ON | ON | ON | ON | ON | ON | ON | ON | ON | ON | ON | ON |
| | Im121 Note 2 | ON | ON | ON | – | – | – | ON | – | – | – | – | – |
| | Im122 Note 2 | ON | ON | ON | ON | ON | ON | ON | ON | – | – | ON | ON |
| | Im123 Note 2 | ON | ON | ON | – | ON | ON | ON | ON | ON | ON | ON | ON |
| | Im124 Note 2 | ON | ON | ON | ON | ON | ON | ON | ON | ON | ON | ON | ON |

**Notes 1.** CC1, CC0 = 0, 0

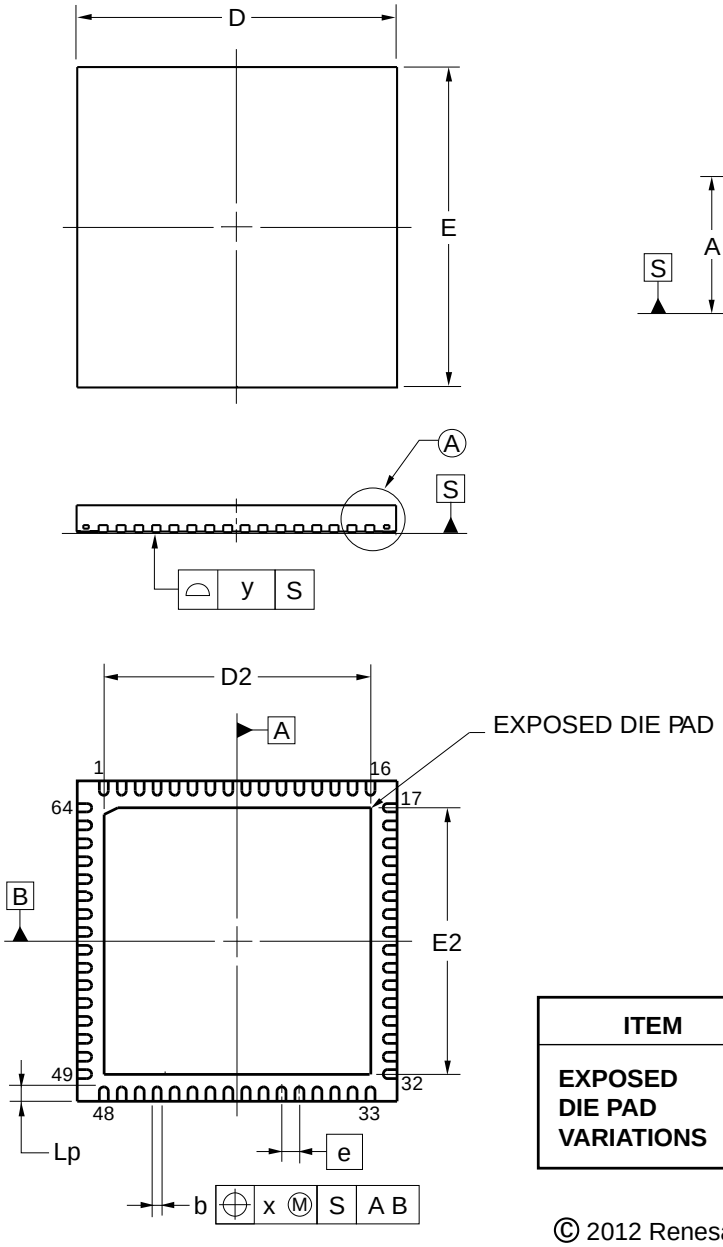
**2.** CC1, CC0 = 1, 1

# CHAPTER 6 PACKAGE DRAWINGS

R5F10FLCANA, R5F10FLDANA, R5F10FLEANA, R5F10FLCDNA, R5F10FLDDNA, R5F10FLEDNA

## 64-PIN PLASTIC WQFN (9 x 9)

| JEITA Package Code | RENESAS Code | Previous Code | MASS (TYP.) [g] |
|---|---|---|---|
| P-HWQFN64-9x9-0.50 | PWQN0064KD-A | P64K8-50-6BA-1 | 0.21 |




(UNIT: mm)

| ITEM | DIMENSIONS |
|---|---|
| D | 9.00±0.05 |
| E | 9.00±0.05 |
| A | 0.75±0.05 |
| b | $0.25^{+0.05}_{-0.07}$ |
| e | 0.50 |
| Lp | 0.40±0.10 |
| x | 0.50 |
| y | 0.50 |

| ITEM | | D2 | | | E2 | | |
|---|---|---|---|---|---|---|---|
| EXPOSED DIE PAD VARIATIONS | A | MIN | NOM | MAX | MIN | NOM | MAX |
| | | 7.45 | 7.50 | 7.55 | 7.45 | 7.50 | 7.55 |