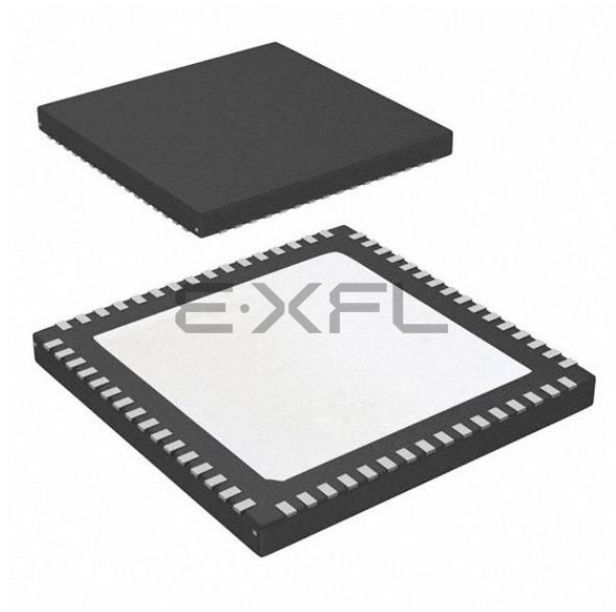
Renesas Electronics America Inc - R5F10FLCDNA#U0 Datasheet



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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	RL78
Core Size	16-Bit
Speed	32MHz
Connectivity	CSI, I²C, LINbus, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	20
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	1.6V ~ 5.5V
Data Converters	A/D 13x8/12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-WFQFN Exposed Pad
Supplier Device Package	64-HWQFN (9x9)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f10flcdna-u0

How to Read This Manual

It is assumed that the readers of this manual have general knowledge of electrical engineering, logic circuits, and microcontrollers.

- To gain a general understanding of functions:
  → Read this manual in the order of the **CONTENTS**. The mark "<R>" shows major revised points. The revised points can be easily searched by copying an "<R>" in the PDF file and specifying it in the "Find what:" field.

- How to interpret the register format:
  → For a bit number enclosed in angle brackets, the bit name is defined as a reserved word in the assembler, and is defined as an sfr variable using the #pragma sfr directive in the compiler.

- To know details of the microcontroller block:
  →Refer to the separate document **RL78/G1A Hardware User's Manual (R01UH0305E)**.

- To know details of the RL78 microcontroller instructions:
  → Refer to the separate document **RL78 family User's Manual Software (R01US0015E)**.

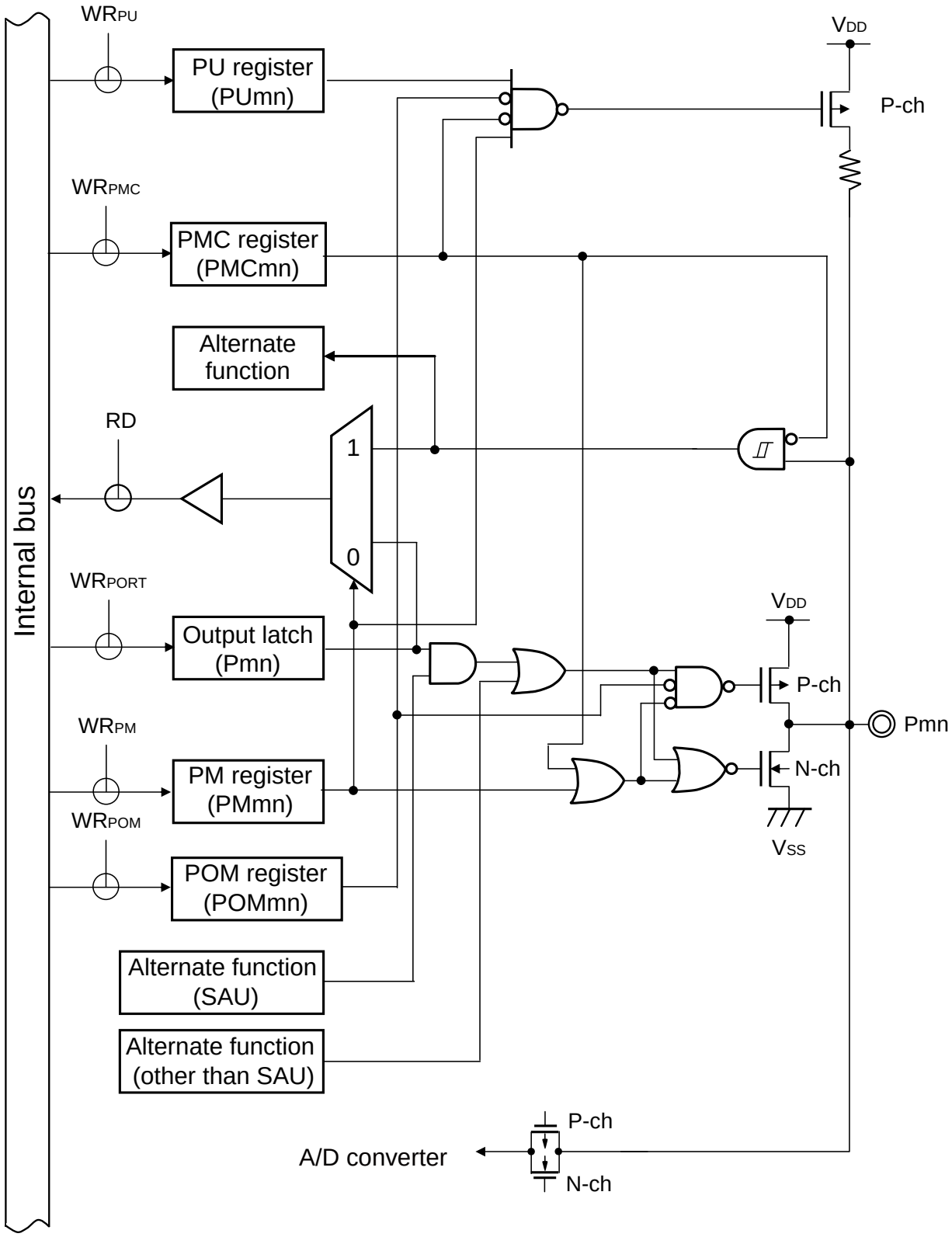
Conventions

Data significance:	Higher digits on the left and lower digits on the right	
Active low representations:	$\overline{\times\times\times}$ (overscore over pin and signal name)	
Note:	Footnote for item marked with **Note** in the text	
Caution:	Information requiring particular attention	
Remark:	Supplementary information	
Numerical representations:	Binary	···×××× or ××××B
	Decimal	···××××
	Hexadecimal	···××××H

(2/2)

<R>	P121	2-2-1	Input	Input port	X1	Port 12. 2-bit input port.
	P122				X2/EXCLK	
	P130	1-1-1	Output	Output port	–	Port 13. 1-bit output port and 1-bit input port.
	P137	2-1-2	Input	Input port	INTP0	
	RESET	2-1-1	Input	–	–	Input only pin for external reset. When external reset is not used, connect this pin to V_{DD} directly or via a resistor.

<R> **Figure 2-9. Pin Block Diagram for Pin Type 7-3-2**



Remarks 1. For alternate functions, see **2. 1. 1 Port functions**.

2. SAU: Serial array unit

2. 5. 9 Port 14 (P140)

(1) Port mode

P140 functions as an I/O port. P140 can be set to input or output port in 1-bit units using port mode register 14 (PM14).

(2) Control mode

P140 functions as clock/buzzer output, and external interrupt request input.

(a) INTP6

This is the external interrupt request input pin for which the valid edge (rising edge, falling edge, or both rising and falling edges) can be specified.

(b) PCLBUZ0

This is the clock/buzzer output pin.

3. 4. 2. 1 Port 0

Port 0 is an I/O port with an output latch. Port 0 can be set to the input mode or output mode in 1-bit units using port mode register 0 (PM0). When the P00 to P04 pins are used as an input port, use of an on-chip pull-up resistor can be specified in 1-bit units by pull-up resistor option register 0 (PU0). Input to the P00, P01, P03 and P04 pins can be specified through a normal input buffer or a TTL input buffer in 1-bit units using port input mode register 0 (PIM0). Output from the P02 to P04 pins can be specified as normal CMOS output or N-ch open-drain output (V_{DD} tolerance) in
<R> 1-bit units using port output mode register 0 (POM0). The P02 and P03 pins can be specified as digital input/output or analog input in 1-bit units, using port mode control register 0 (PMC0). This port can be also used for timer I/O, A/D converter analog input, serial interface data I/O, clock I/O, and key interrupt input.

When reset signal is generated, the following configuration will be set.

- P00, P01 and P04 pins ⋯ Input mode
- P02 and P03 pins ⋯ Analog input

3. 4. 2. 2 Port 1

Port 1 is an I/O port with an output latch. Port 1 can be set to the input mode or output mode in 1-bit units using port mode register 1 (PM1). When the P10 to P15 pins are used as an input port, use of an on-chip pull-up resistor can be specified in 1-bit units by pull-up resistor option register 1 (PU1). Input to the P10, P11, P14 to P15 pins can be specified through a normal input buffer or a TTL input buffer in 1-bit units using port input mode register 1 (PIM1). Output from the P10 to P15 pins can be specified as normal CMOS output or N-ch open-drain output (V_{DD} tolerance) in
<R> 1-bit units using port output mode register 1 (POM1). The P10 to P15 pins can be specified as digital input/output or analog input in 1-bit units, using port mode control register 1 (PMC1). This port can be also used for A/D converter analog input, serial interface data I/O, programming UART I/O, and key return input.

When reset signal is generated, the P10 to P15 pins will be set to analog input.

3. 4. 2. 3 Port 2

Port 2 is an I/O port with an output latch. Port 2 can be set to the input mode or output mode in 1-bit units using port mode register 2 (PM2). This port can be also used for A/D converter analog input and reference voltage input, and key return input pin. Setting digital or analog to each pin can be done in A/D port configuration register (ADPC).

When reset signal is generated, the P20/ANI0 to P24/ANI4 pins will be set to analog input.

3. 5 Clock Generator

In this section, the differences of the functions and registers from RL78/G1A (64-pin products) are described. For details, see **CHAPTER 5 CLOCK GENERATOR** in **RL78/G1A Hardware User's Manual (R01UH0305E)**.

3. 5. 1 Functions of clock generator

The clock generator generates the clock to be supplied to the CPU and peripheral hardware.

The following two kinds of system clocks and clock oscillators are selectable.

Caution The subsystem clock is not provided in the RL78/G1E (64-pin products, 80-pin products).

(1) Main system clock

<1> X1 oscillator

This circuit oscillates a clock of f_X = 1 to 20 MHz by connecting a resonator to X1 and X2.

Oscillation can be stopped by executing the STOP instruction or setting of the MSTOP bit (bit 7 of the clock operation status control register (CSC)).

<2> High-speed on-chip oscillator (High-speed OCD)

<R> The frequency at which to oscillate can be selected from among f_{IH} = 32, 24, 16, 12, 8, 6, 4, 3, 2 or 1 MHz (typ.) by using the option byte (000C2H). After a reset release, the CPU always starts operating with this high-speed on-chip oscillator clock. Oscillation can be stopped by executing the STOP instruction or setting the HIOSTOP bit (bit 0 of the CSC register).

The frequency specified by using an option byte can be changed by using the high-speed on-chip oscillator frequency select register (HOCODIV). For details about the frequency, see **3. 5. 3. 8 High-speed on-chip oscillator frequency select register (HOCODIV)**.

The frequencies that can be specified for the high-speed on-chip oscillator by using the option byte and the high-speed on-chip oscillator frequency select register (HOCODIV) are shown below.

Power Supply Voltage	Flash Operation Mode	Oscillation Frequency (MHz)									
		1	2	3	4	6	8	12	16	24	32
2.7 V ≤ V_{DD} ≤ 5.5 V	HS (high-speed main) mode	√	√	√	√	√	√	√	√	√	√
2.4 V ≤ V_{DD} ≤ 5.5 V		√	√	√	√	√	√	√	√	–	–
1.8 V ≤ V_{DD} ≤ 5.5 V	LS (low-speed main) mode	√	√	√	√	√	√	–	–	–	–
1.6 V ≤ V_{DD} ≤ 5.5 V	LV (low-voltage main) mode	√	√	–	√	–	–	–	–	–	–

An external main system clock (f_{EX} = 1 to 20 MHz) can also be supplied from the EXCLK/X2/P122 pin. An external main system clock input can be disabled by executing the STOP instruction or setting of the MSTOP bit.

As the main system clock, a high-speed system clock (X1 clock or external main system clock) or high-speed on-chip oscillator clock can be selected by setting of the MCM0 bit (bit 4 of the system clock control register (CKC)).

(1) X1 oscillation: **As of March, 2013(4/4)**

Manufacturer	Resonator	Part Number	SMD/ Lead	Frequency (MHz)	Flash operation mode Note 1	Recommended Circuit Constants Note 2 (reference)			Oscillation Voltage Range (V)	
						C1 (pF)	C2 (pF)	Rd (kΩ)	MIN.	MAX.
Nihon Dempa Kogyo Co., Ltd. Note 3	Crystal resonator	NX8045GB	SMD	8	LS	1	1	0	1.8	5.5
		NX8045GB	SMD	8	HS	1	1	0	2.4	5.5
		NX3225GB	SMD	16		2	2	0	2.4	5.5
		NX2520SA	SMD	20		1	1	0	2.7	5.5

<R> **Notes 1.** Set the flash operation mode by using CMODE1 and CMODE0 bits of the option byte (000C2H).

2. C1, C2 columns indicate a reference value.

3. When using these oscillators, contact Nihon Dempa Kogyo Co., Ltd. (http://www.ndk.com/jp/).

Remark Relationship between operation voltage width, operation frequency of CPU and operation mode is as below.

HS (High speed main) mode: 2.7 V ≤ V_{DD} ≤ 5.5 V@1 MHz to 32 MHz (When X1 oscillation: 1 MHz to 20 MHz)
2.4 V ≤ V_{DD} ≤ 5.5 V@1 MHz to 16 MHz

LS (Low speed main) mode: 1.8 V ≤ V_{DD} ≤ 5.5 V@1 MHz to 8 MHz

LV (Low voltage main) mode: 1.6 V ≤ V_{DD} ≤ 5.5 V@1 MHz to 4 MHz

3. 11. 2 Configuration of A/D converter

The A/D converter includes the following hardware.

(1) ANI0 to ANI4, ANI16 to ANI18, ANI20 to ANI26, ANI28, and ANI30 pins

These are the analog input pins of the 17 channels of the A/D converter. They input analog signals to be converted into digital signals. Pins other than the one selected as the analog input pin can be used as I/O port pins.

(2) Sample & hold circuit

The sample & hold circuit samples each of the analog input voltages sequentially sent from the input circuit, and sends them to the A/D voltage comparator. This circuit also holds the sampled analog input voltage during A/D conversion.

(3) A/D voltage comparator

This A/D voltage comparator compares output from the voltage tap of the comparison voltage generator with the sampled voltage value.

If the analog input voltage is found to be greater than the reference voltage (1/2 AV_{REF}) as a result of the comparison, the most significant bit (MSB) of the successive approximation register (SAR) is set. If the analog input voltage is less than the reference voltage (1/2 AV_{REF}), the MSB bit of the SAR is reset.

After that, bit 10 of the SAR register is automatically set, and the next comparison is made. The voltage tap of the comparison voltage generator is selected by the value of bit 11, to which the result has been already set.

Bit 11 = 0: (1/4 AV_{REF})
Bit 11 = 1: (3/4 AV_{REF})

The voltage tap of the comparison voltage generator and the analog input voltage are compared and bit 10 of the SAR register is manipulated according to the result of the comparison.

Analog input voltage ≥ Voltage tap of comparison voltage generator: Bit 10 = 1
Analog input voltage ≤ Voltage tap of comparison voltage generator: Bit 10 = 0

Comparison is continued like this to bit 0 of the SAR register.

When performing A/D conversion at a resolution of 8 bits, the comparison continues until bit 4 of the SAR register.

Remark AV_{REF}: The + side reference voltage of the A/D converter.
(This can be selected from AV_{REFP}, the internal reference voltage (1.45 V), and AV_{DD}.)

(4) Comparison voltage generator

The comparison voltage generator generates the comparison voltage input from an analog input pin.

- Setting of serial communication operation setting register mn (SCRmn) (2/2)

<R> Address: F0118H, F0119H (SCR00) - F011EH, F011FH (SCR03), After reset: 0087H R/W
F0158H, F0159H (SCR10), F015AH, F015BH (SCR11)

Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SCRmn	TXE mn	RXE mn	DAP mn	CKP mn	0	EOC mn	PTC mn1	PTC mn0	DIR mn	0	SLC mn1 Note 1	SLC mn0	0	1	DLS mn1 Note 2	DLS mn0

PTCmn1	PTCmn0	Setting of parity bit in UART mode	
		Transmission	Reception
0	0	Does not output the parity bit.	Receives without parity
0	1	Outputs 0 parity Note 3.	No parity judgment
1	0	Outputs even parity.	Judged as even parity.
1	1	Outputs odd parity.	Judges as odd parity.
Be sure to set PTCmn1, PTCmn0 = 0, 0 in the CSI mode and simplified I^2C mode.			

DIRmn	Selection of data transfer sequence in CSI and UART modes
0	Inputs/outputs data with MSB first.
1	Inputs/outputs data with LSB first.
Be sure to clear DIRmn = 0 in the simplified I^2C mode.	

SLCmn1 Note 1	SLCmn0	Setting of stop bit in UART mode
0	0	No stop bit
0	1	Stop bit length = 1 bit
1	0	Stop bit length = 2 bits (mn = 00, 02, 10 only)
1	1	Setting prohibited
When the transfer end interrupt is selected, the interrupt is generated when all stop bits have been completely transferred. Set 1 bit (SLCmn1, SLCmn0 = 0, 1) during UART reception and in the simplified I^2C mode. Set no stop bit (SLCmn1, SLCmn0 = 0, 0) in the CSI mode.		

DLSmn1 Note 2	DLSmn0	Setting of data length in CSI and UART modes
0	1	9-bit data length (stored in bits 0 to 8 of the SDRmn register) (settable in UART mode only)
1	0	7-bit data length (stored in bits 0 to 6 of the SDRmn register)
1	1	8-bit data length (stored in bits 0 to 7 of the SDRmn register)
Other than above		Setting prohibited
Be sure to set DLSmn1, DLSmn0 = 1, 1 in the simplified I^2C mode.		

(**Notes**, **Caution** and **Remark** are on the next page.)

Notes 1. If one of the interrupt sources INTST1, INTCSI10, and INTIIC10 is generated, bit 0 of the IF1L register is set to 1. Bit 0 of the MK1L, PR01L, and PR11L registers can be used for all three of these interrupt sources.

2. If one of the interrupt sources INTSR1, INTCSI11, and INTIIC11 is generated, bit 1 of the IF1L register is set to 1. Bit 1 of the MK1L, PR01L, and PR11L registers can be used for all three of these interrupt sources.

<R> **3.** Do not use the error interrupt of UART1 reception and the interrupt of channel 3 of TAU0 (while the higher 8 bits are operating at a timer) at the same time because they share flags for the interrupt request sources. If the error interrupt of UART1 reception is not used (EOC03 = 0), UART1 and channel 3 of TAU0 (while the higher 8 bits are operating at a timer) can be used at the same time. If the interrupt source INTSRE1 or INTTM03H is generated, bit 2 of the IF1L register is set to 1. Bit 2 of the MK1L, PR01L, and PR11L registers can be used for both these interrupt sources.

- 80-pin products

Address: FFFE4H After reset: FFH R/W

Symbol	7	6	5	<4>	<3>	<2>	<1>	<0>
MK0L	1	1	1	PMK2	PMK1	PMK0	LVIMK	WDTIMK

Address: FFFE5H After reset: FFH R/W

Symbol	<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>
MK0H	TMMK01H SREMK0	SRMK0	STMK0 CSIMK00 IICMK00	DMAMK1	DMAMK0	SREMK2	SRMK2 CSIMK21	STMK2 CSIMK20 IICMK20

Address: FFFE6H After reset: FFH R/W

Symbol	<7>	<6>	<5>	<4>	3	<2>	<1>	<0>
MK1L	TMMK03	TMMK02	TMMK01	TMMK00	1	SREMK1 TMMK03H	SRMK1	STMK1 CSIMK10 IICMK10

Address: FFFE7H After reset: FFH R/W

Symbol	<7>	6	5	4	<3>	<2>	1	<0>
MK1H	TMMK04	1	1	1	KRMK	ITMK	1	ADMK

Address: FFFD4H After reset: FFH R/W

Symbol	7	6	5	4	<3>	<2>	<1>	<0>
MK2L	1	1	1	1	PMK6	TMMK07	TMMK06	TMMK05

Address: FFFD5H After reset: FFH R/W

Symbol	<7>	6	<5>	4	3	2	1	0
MK2H	FLMK	1	MDMK	1	1	1	1	1

Cautions 1. Be sure to set bits 5 to 7 of the MK0L register to “1”.

2. Be sure to set bit 3 of the MK1L register to “1”.

3. Be sure to set bits 1 and 4 to 6 of the MK1H register to “1”.

4. Be sure to set bits 4 to 7 of the MK2L register to “1”.

5. Be sure to set bits 0 to 4 and 6 of the MK2H register to “1”.

3. 16. 3. 3 Priority specification flag registers (PR00L, PR00H, PR01L, PR01H, PR10L, PR10H, PR11L, PR11H, PR12L, PR12H, PR02L, PR02H)

- 64-pin products

Address: FFFE8H After reset: FFH R/W

Symbol	7	6	5	4	3	<2>	<1>	<0>
PR00L	1	1	1	1	1	PPR00	LVIPR0	WDTIPR0

Address: FFFECH After reset: FFH R/W

Symbol	7	6	5	4	3	<2>	<1>	<0>
PR10L	1	1	1	1	1	PPR10	LVIPR1	WDTIPR1

Address: FFFE9H After reset: FFH R/W

Symbol	<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>
PR00H	TMPR001H SREPR00	SRPR00	STPR00 CSIPR000 IICPR00	DMAPR01	DMAPR00	SREPR02	SRPR02 CSIPR021	STPR02

Address: FFFEDH After reset: FFH R/W

Symbol	<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>
PR10H	TMPR101H SREPR10	SRPR10	STPR10 CSIPR100 IICPR100	DMAPR11	DMAPR10	SREPR12	SRPR12 CSIPR121	STPR12

Address: FFFEAH After reset: FFH R/W

Symbol	<7>	<6>	<5>	<4>	3	<2>	<1>	<0>
PR01L	TMPR003	TMPR002	TMPR001	TMPR000	1	SREPR01 TMPR003H	SRPR01	STPR01

Address: FFFEEH After reset: FFH R/W

Symbol	<7>	<6>	<5>	<4>	3	<2>	<1>	<0>
PR11L	TMPR103	TMPR102	TMPR101	TMPR100	1	SREPR11 TMPR103H	SRPR11	STPR11

Address: FFFEBH After reset: FFH R/W

Symbol	<7>	6	5	4	<3>	<2>	1	<0>
PR01H	TMPR004	1	1	1	KRPR0	ITPR0	1	ADPR0

Address: FFFEFH After reset: FFH R/W

Symbol	<7>	6	5	4	<3>	<2>	1	<0>
PR11H	TMPR104	1	1	1	KRPR1	ITPR1	1	ADPR1

- 80-pin products

Address: FFFE8H After reset: FFH R/W

Symbol	7	6	5	<4>	<3>	<2>	<1>	<0>
PR00L	1	1	1	PPR02	PPR01	PPR00	LVIPR0	WDTIPR0

Address: FFFECH After reset: FFH R/W

Symbol	7	6	5	4	<3>	<2>	<1>	<0>
PR10L	1	1	1	PPR12	PPR11	PPR10	LVIPR1	WDTIPR1

Address: FFFE9H After reset: FFH R/W

Symbol	<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>
PR00H	TMPR001H SREPR00	SRPR00	STPR00 IICPR000	DMAPR01	DMAPR00	SREPR02	SRPR02 CSIPR021	STPR02 CSIPR020 IICPR020

Address: FFFEDH After reset: FFH R/W

Symbol	<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>
PR10H	TMPR101H SREPR10	SRPR10	STPR10 CSIPR100 IICPR100	DMAPR11	DMAPR10	SREPR12	SRPR12 CSIPR121	STPR12 CSIPR120 IICPR120

Address: FFFEAH After reset: FFH R/W

Symbol	<7>	<6>	<5>	<4>	3	<2>	<1>	<0>
PR01L	TMPR003	TMPR002	TMPR001	TMPR000	1	SREPR01 TMPR003H	SRPR01	STPR01 CSIPR010 IICPR010

Address: FFFEEH After reset: FFH R/W

Symbol	<7>	<6>	<5>	<4>	3	<2>	<1>	<0>
PR11L	TMPR103	TMPR102	TMPR101	TMPR100	1	SREPR11 TMPR103H	SRPR11	STPR11 CSIPR110 IICPR110

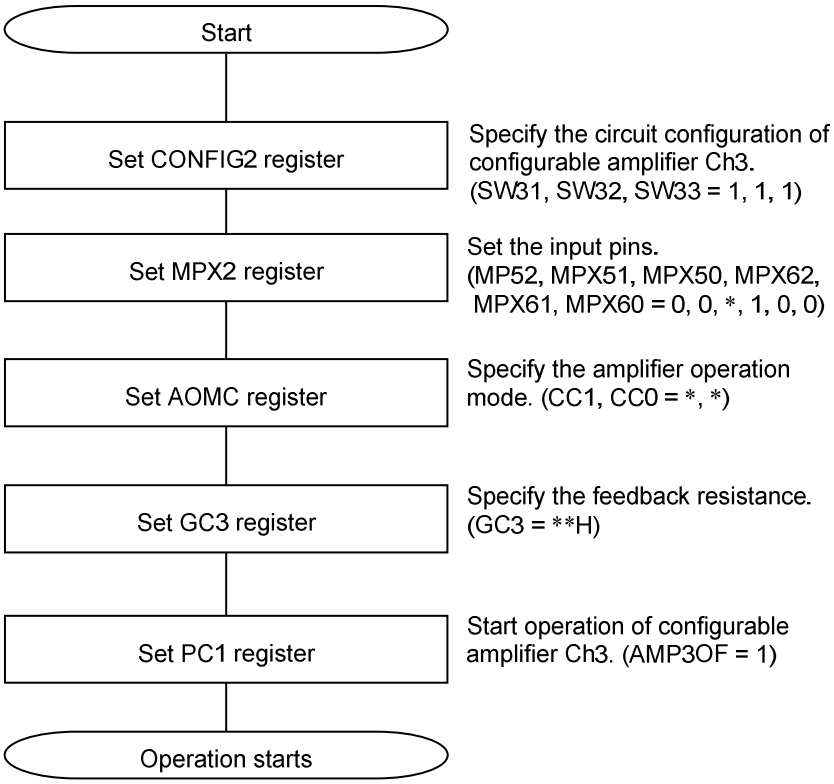
Address: FFFEBH After reset: FFH R/W

Symbol	<7>	6	5	4	<3>	<2>	1	<0>
PR01H	TMPR004	1	1	1	KRPR0	ITPR0	1	ADPR0

Address: FFFEFH After reset: FFH R/W

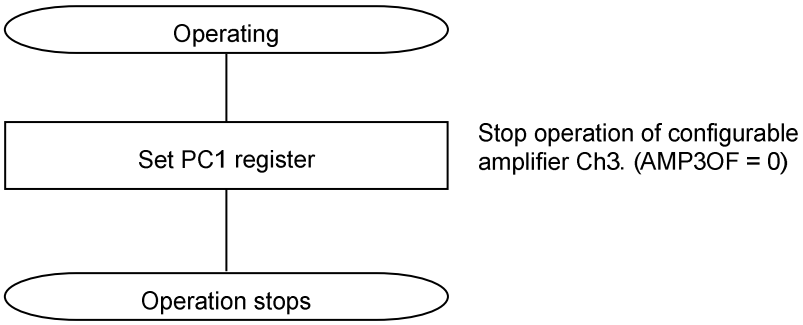
Symbol	<7>	6	5	4	<3>	<2>	1	<0>
PR11H	TMPR104	1	1	1	KRPR1	ITPR1	1	ADPR1

Example of procedure for starting configurable amplifier Ch3 (transimpedance amplifier)



Remark *: don't care

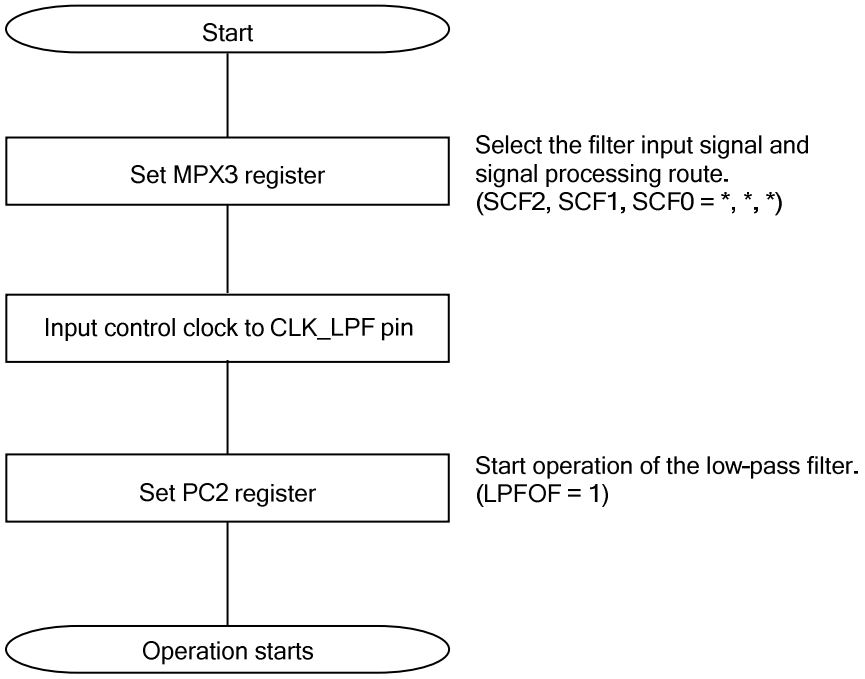
Example of procedure for stopping configurable amplifier Ch3 (transimpedance amplifier)



4. 4. 4 Procedure for operating the low-pass filter

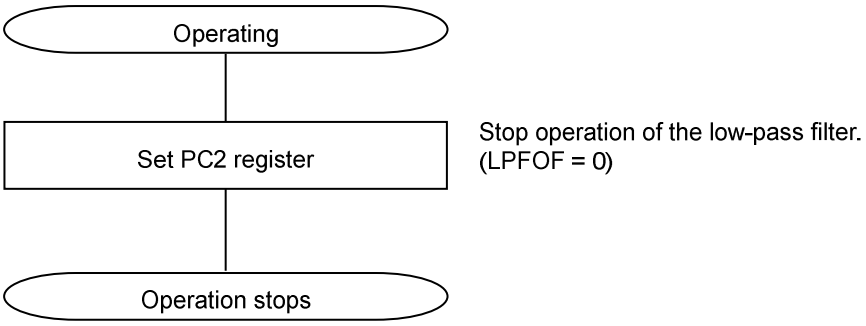
Follow the procedures below to start and stop the low-pass filter.

Example of procedure for starting the low-pass filter



Remark *: don't care

Example of procedure for stopping the low-pass filter



4. 7 Variable Output Voltage Regulator

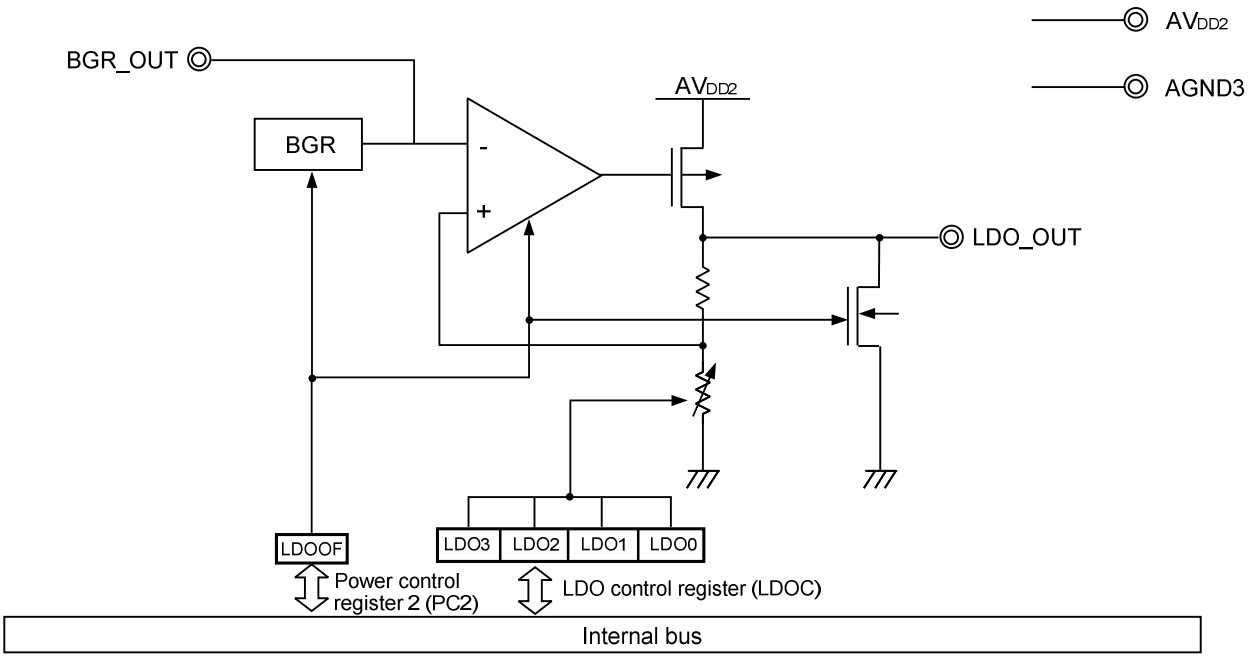
The RL78/G1E (64-pin products, 80-pin products) has one on-chip variable output voltage regulator channel. This is a series regulator that generates a voltage of 3.3 V (default) from a supplied voltage of 5 V.

4. 7. 1 Overview of variable output voltage regulator features

The features of variable output voltage regulator are described below.

- Output voltage range: 2.0 to 3.3 V (Typ.)
- Output current: 15 mA (Max.)
- Includes a power-off function.

4. 7. 2 Block diagram



(T_A = –40 to +85°C, 1.6 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V) (2/3)

Parameter	Symbol	Conditions				MIN.	TYP.	MAX.	Unit
Supply current[Note 1]	I_{DD2}[Note 2]	HALT mode	HS (High-speed main) mode[Note 6]	f_{IH} = 32 MHz[Note 4]	V_{DD} = 5.0 V		0.54	1.63	mA
					V_{DD} = 3.0 V		0.54	1.63	
				f_{IH} = 24 MHz[Note 4]	V_{DD} = 5.0 V		0.44	1.28	mA
					V_{DD} = 3.0 V		0.44	1.28	
				f_{IH} = 16 MHz[Note 4]	V_{DD} = 5.0 V		0.40	1.00	mA
					V_{DD} = 3.0 V		0.40	1.00	
			LS (Low-speed main) mode[Note 6]	f_{IH} = 8 MHz[Note 4]	V_{DD} = 3.0 V		260	530	μA
					V_{DD} = 2.0 V		260	530	
			LV (Low-voltage main) mode[Note 6]	f_{IH} = 4 MHz[Note 4]	V_{DD} = 3.0 V		420	640	μA
					V_{DD} = 2.0 V		420	640	
			HS (High-speed main) mode[Note 6]	f_{MX} = 20 MHz[Note 3], V_{DD} = 5.0 V	Square wave input		0.28	1.00	mA
					Resonator connection		0.45	1.17	
				f_{MX} = 20 MHz[Note 3], V_{DD} = 3.0 V	Square wave input		0.28	1.00	
					Resonator connection		0.45	1.17	
				f_{MX} = 10 MHz[Note 3], V_{DD} = 5.0 V	Square wave input		0.19	0.60	mA
					Resonator connection		0.26	0.67	
				f_{MX} = 10 MHz[Note 3], V_{DD} = 3.0 V	Square wave input		0.19	0.60	
					Resonator connection		0.26	0.67	
			LS (Low-speed main) mode[Note 6]	f_{MX} = 8 MHz[Note 3], V_{DD} = 3.0 V	Square wave input		95	330	μA
					Resonator connection		145	380	
				f_{MX} = 8 MHz[Note 3], V_{DD} = 2.0 V	Square wave input		95	330	
					Resonator connection		145	380	
	I_{DD3}[Note 5]	STOP mode	T_A = –40°C				0.15	0.50	μA
			T_A = +25°C				0.22	0.50	
			T_A = +50°C				0.34	1.10	
			T_A = +70°C				0.46	1.90	
			T_A = +85°C				0.75	3.30	

(**Notes** and **Remarks** are listed on the next page.)

(-40°C ≤ T_A ≤ 85°C, AV_{DD1} = AV_{DD2} = AV_{DD3} = DV_{DD} = 5.0 V, VREFIN1 = VREFIN2 = VREFIN3 = 1.7 V, AMP1OF = AMP2OF = AMP3OF = 1, DAC1OF = DAC2OF = DAC3OF = 0, inverting amplifier) (2/2)

Parameter	Symbol	Conditions	Ratings			Unit
			MIN	TYP	MAX	
Input conversion offset voltage	VOFF00	CC1, CC0 = 0, 0, T_A = 25°C GCn = 07H (20 dB)	-7	–	7	mV
	VOFF01	CC1, CC0 = 0, 1, T_A = 25°C GCn = 07H (20 dB)	-10	–	10	mV
	VOFF10	CC1, CC0 = 1, 0, T_A = 25°C GCn = 07H (20 dB)	-10	–	10	mV
	VOFF11	CC1, CC0 = 1, 1, T_A = 25°C GCn = 07H (20 dB)	-12	–	12	mV
Input conversion offset voltage temperature coefficient	VOTC		–	±6	–	μV/°C
Slew rate	SR00	CC1, CC0 = 0, 0, CL = 30 pF, GCn = 00H (6 dB)	–	0.68	–	V/μs
	SR01	CC1, CC0 = 0, 1, CL = 30 pF, GCn = 00H (6 dB)	–	0.35	–	V/μs
	SR10	CC1, CC0 = 1, 0, CL = 30 pF, GCn = 00H (6 dB)	–	0.25	–	V/μs
	SR11	CC1, CC0 = 1, 1, CL = 30 pF, GCn = 00H (6 dB)	–	0.09	–	V/μs
Power supply rejection ratio	PSRR00	CC1, CC0 = 0, 0 GCn = 00H (6 dB), f = 1 kHz	–	70	–	dB
	PSRR01	CC1, CC0 = 0, 1 GCn = 00H (6 dB), f = 1 kHz	–	68	–	dB
	PSRR10	CC1, CC0 = 1, 0 GCn = 00H (6 dB), f = 1 kHz	–	62	–	dB
	PSRR11	CC1, CC0 = 1, 1 GCn = 00H (6 dB), f = 1 kHz	–	50	–	dB
Gain setting error	GAIN_Accu1	T_A = 25°C	-0.6	–	0.6	dB
	GAIN_Accu2	T_A = –40 to 85°C	-1.0	–	1.0	dB

Remark n = 1 to 3

(-40°C ≤ T_A ≤ 85°C, AV_{DD1} = AV_{DD2} = AV_{DD3} = DV_{DD} = 5.0 V, VREFIN1 = VREFIN2 = VREFIN3 = 1.7 V, AMP1OF = AMP2OF = AMP3OF = 1, DAC1OF = DAC2OF = DAC3OF = 0, transimpedance amplifier) (2/2)

Parameter	Symbol	Conditions	Ratings			Unit
			MIN	TYP	MAX	
Input conversion offset voltage	VOFF00	CC1, CC0 = 0, 0, T_A = 25°C, GCn = 07H (Rfb = 80 kΩ)	-7	–	7	mV
	VOFF01	CC1, CC0 = 0, 1, T_A = 25°C, GCn = 07H (Rfb = 80 kΩ)	-10	–	10	mV
	VOFF10	CC1, CC0 = 1, 0, T_A = 25°C, GCn = 07H (Rfb = 80 kΩ)	-10	–	10	mV
	VOFF11	CC1, CC0 = 1, 1, T_A = 25°C, GCn = 07H (Rfb = 80 kΩ)	-12	–	12	mV
Input conversion offset voltage temperature coefficient	VOTC		–	±6	–	μV/°C
Slew rate	SR00	CC1, CC0 = 0, 0, CL = 30 pF, GCn = 00H (Rfb = 20 kΩ)	–	0.68	–	V/μs
	SR01	CC1, CC0 = 0, 1, CL = 30 pF, GCn = 00H (Rfb = 20 kΩ)	–	0.35	–	V/μs
	SR10	CC1, CC0 = 1, 0, CL = 30 pF, GCn = 00H (Rfb = 20 kΩ)	–	0.25	–	V/μs
	SR11	CC1, CC0 = 1, 1, CL = 30 pF, GCn = 00H (Rfb = 20 kΩ)	–	0.09	–	V/μs
Power supply rejection ratio	PSRR00	CC1, CC0 = 0, 0, GCn = 00H (Rfb = 20 kΩ)	–	70	–	dB
	PSRR01	CC1, CC0 = 0, 1, GCn = 00H (Rfb = 20 kΩ)	–	68	–	dB
	PSRR10	CC1, CC0 = 1, 0, GCn = 00H (Rfb = 20 kΩ)	–	62	–	dB
	PSRR11	CC1, CC0 = 1, 1, GCn = 00H (Rfb = 20 kΩ)	–	50	–	dB
Rfb setting error	Rfb_Accu1	T_A = 25°C	-25	–	25	%
	Rfb_Accu2	T_A = –40 to 85°C	-35	–	35	%

Remark n = 1 to 3

5. 3. 3. 5 High-pass filter characteristics

($-40°C \le T_A \le 85°C$, $AV_{DD1} = AV_{DD2} = AV_{DD3} = AV_{DD4} = DV_{DD} = 5.0$ V, HPFOF = 1)

Parameter	Symbol	Conditions	Ratings			Unit
			MIN.	TYP.	MAX.	
Current consumption	IccA		–	800	1800	μA
Input voltage	V_{ILHPF}		AGND4 +0.2	–	–	V
	V_{IHHPF}		–	–	AV_{DD3} - 1.5	V
<R> Output voltage	V_{OLHPF}	IOL = –200 μA	–	AGND4 +0.22	AGND4 +0.25	V
	V_{OHHPF}	IOH = 200 μA	AV_{DD3} -1.55	AV_{DD3} -1.52	–	V
Cutoff frequency	fc1	f_{CLK_HPF} = 2 kHz	–	8	–	Hz
	fc2	f_{CLK_HPF} = 200 kHz	–	800	–	Hz
CLK_HPF low-level input voltage	V_{ILCLK_HPF}				$0.3 \times AV_{DD3}$	V
CLK_HPF high-level input voltage	V_{IHCLK_HPF}		$0.7 \times AV_{DD3}$			V
CLK_HPF Input frequency	f_{CLK_HPF}		2	–	200	kHz
CLK_HPF Input low-level-width Input high-level-width	t_{ILW_HPF} t_{IHW_HPF}		200	–	–	ns

Clock Timing