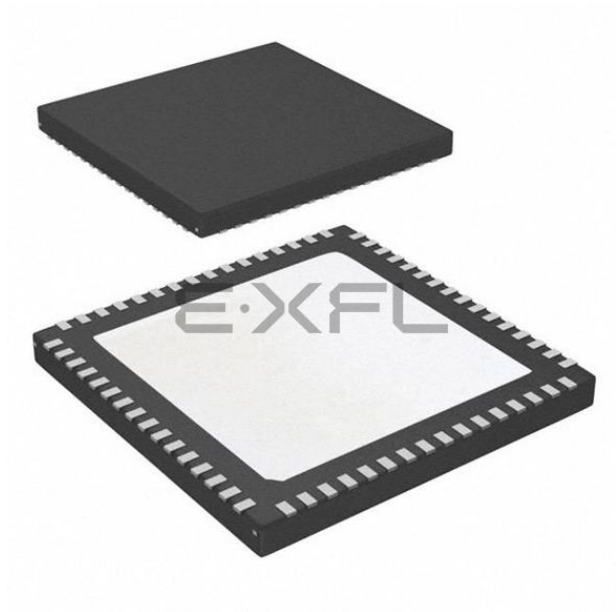
Renesas Electronics America Inc - R5F10FLDANA#U0 Datasheet



Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	RL78
Core Size	16-Bit
Speed	32MHz
Connectivity	CSI, I²C, LINbus, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	20
Program Memory Size	48KB (48K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	3K x 8
Voltage - Supply (Vcc/Vdd)	1.6V ~ 5.5V
Data Converters	A/D 13x8/12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-WFQFN Exposed Pad
Supplier Device Package	64-WQFN (9x9)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f10fldana-u0

3. 6. 3. 15 Registers controlling port functions of pins to be used for timer I/O 144
3. 6. 4 Basic rules of timer array unit 145
3. 6. 5 Operation of counter 145
3. 6. 6 Channel output (TOmn pin) control 145
3. 6. 7 Timer input (TImn) control 145
3. 6. 8 Independent channel operation function of timer array unit 145
3. 6. 9 Simultaneous channel operation function of timer array unit 145
3. 6. 10 Cautions when using timer array unit 145
3. 7 Real-Time Clock 146
3. 8 12-bit Interval Timer 147
3. 8. 1 Functions of 12-bit interval timer 147
3. 8. 2 Configuration of 12-bit interval timer 147
3. 8. 3 Registers controlling 12-bit interval timer 148
3. 8. 3. 1 Peripheral enable register0 (PER0) 148
3. 8. 3. 2 Subsystem clock supply mode control register (OSMC) 148
3. 8. 3. 3 Interval timer control register (ITMC) 149
3. 8. 4 12- bit interval timer operation 149
3. 9 Clock Output/Buzzer Output Controller 150
3. 9. 1 Functions of clock output/buzzer output controller 150
3. 9. 2 Configuration of clock output/buzzer output controller 151
3. 9. 3 Registers controlling clock output/buzzer output controller 151
3. 9. 3. 1 Clock output select register 0 (CKS0) 152
3. 9. 3. 2 Registers controlling port functions of pins to be used for clock or buzzer output 153
3. 9. 4 Operations of clock output/buzzer output controller 153
3. 9. 5 Cautions of clock output/buzzer output controller 153
3. 10 Watchdog Timer 154
3. 11 A/D Converter 155
3. 11. 1 Function of A/D converter 155
3. 11. 2 Configuration of A/D converter 158
3. 11. 3 Registers used in A/D converter 160
3. 11. 3. 1 Peripheral enable register 0 (PER0) 160
3. 11. 3. 2 A/D converter mode register 0 (ADM0) 160
3. 11. 3. 3 A/D converter mode register 1 (ADM1) 161
3. 11. 3. 4 A/D converter mode register 2 (ADM2) 162
3. 11. 3. 5 12-bit A/D conversion result register (ADCR) 162
3. 11. 3. 6 8-bit A/D conversion result register (ADCRH) 162
3. 11. 3. 7 Analog input channel specification register (ADS) 163
3. 11. 3. 8 Conversion result comparison upper limit setting register (ADUL) 167
3. 11. 3. 9 Conversion result comparison lower limit setting register (ADLL) 167
3. 11. 3. 10 A/D test register (ADTES) 167
3. 11. 3. 11 Registers controlling port function of analog input pins 167

(2) Block diagram in analog block (80-pin products)

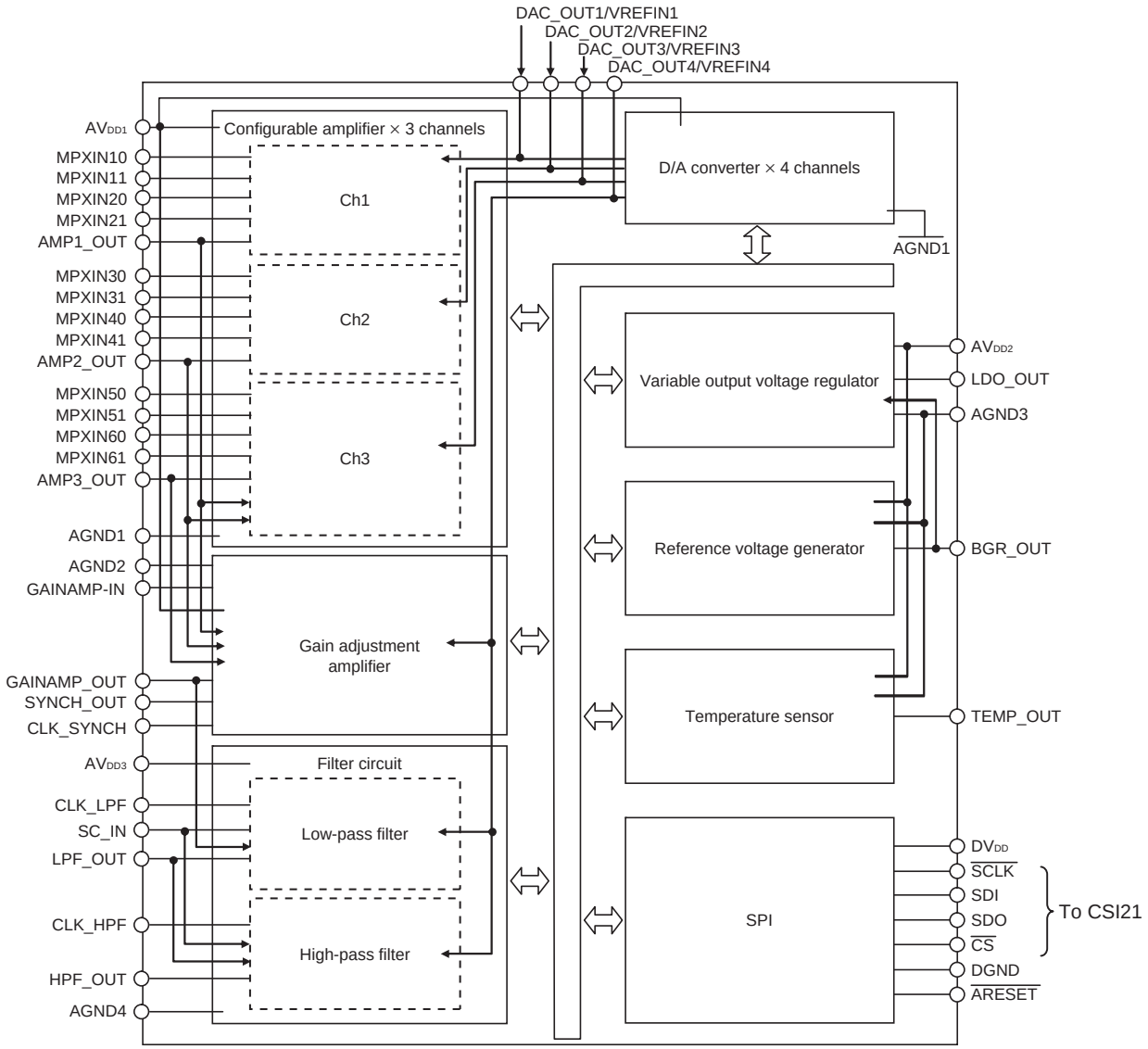
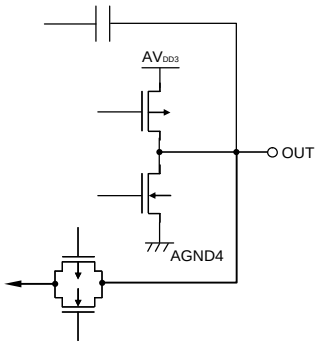


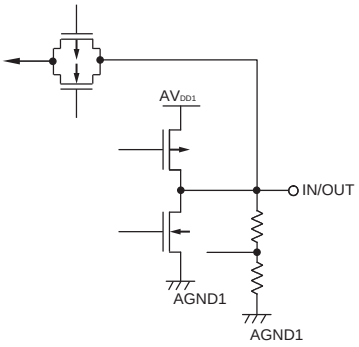
Figure 2-13. Pin I/O Circuit List (1/2)

<R>

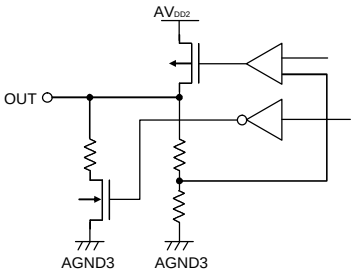
ANALOG1



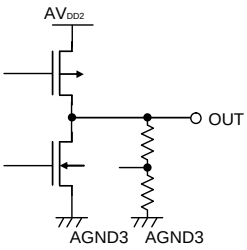
ANALOG2



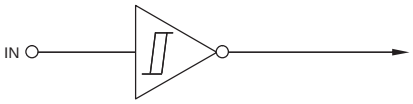
ANALOG3



ANALOG4

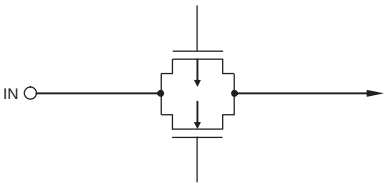


ANALOG5

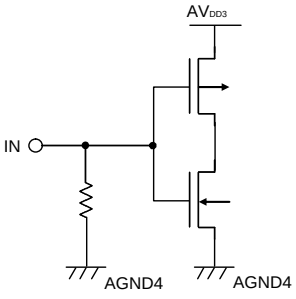


Schmitt-triggered input with hysteresis characteristics

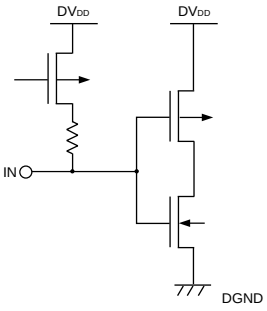
ANALOG6



ANALOG7



ANALOG8



2. 5. 10 AV_{DD}, AV_{SS}, V_{DD}, V_{SS}

(a) AV_{DD}

This is the A/D converter reference voltage input pin and the positive power supply pin of P20 to P24, and A/D converter.

(b) AV_{SS}

This is the A/D converter ground potential pin. Even when the A/D converter is not used, always use this pin with the same potential as the V_{SS} pin.

(c) V_{DD}

This is the positive power supply pin.

(d) V_{SS}

This is the ground potential pin.

Remark Use bypass capacitors (about 0.1 μF) as noise and latch up countermeasures with relatively thick wires at the shortest distance to V_{DD} to V_{SS} line.

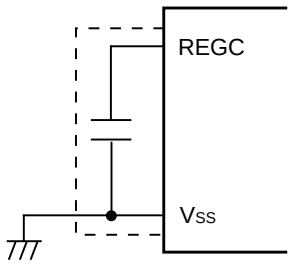
2. 5. 11 $\overline{\text{RESET}}$

This is the active-low system reset input pin for the functions of microcontroller block. When the external reset pin is not used, connect this pin directly or via a resistor to V_{DD}. When the external reset pin is used, design the circuit based on V_{DD}. For details of the functions, see **3. 5. 5 Clock generator operation, 3. 19 Reset Function, 3. 20 Power-On-Reset Circuit**.

2. 5. 12 REGC

This is the pin for connecting regulator output stabilization capacitance for internal operation. Connect this pin to V_{SS} via a capacitor (0.47 to 1 μF).

Also, use a capacitor with good characteristics, since it is used to stabilize internal voltage.



Caution Keep the wiring length as short as possible for the broken-line part in the above figure.

Table 3-3. List of Differences in Expanded Special Function Registers (2nd SFRs) (5/6)

Address	RL78/G1E (64-pin products)			RL78/G1A (64-pin products)		
	2nd SFRs Name	Symbol		2nd SFRs Name	Symbol	
F0180H	Same as RL78/G1A (64-pin products)	TCR00		Timer counter register 00	TCR00	
F0181H						
F0182H	Same as RL78/G1A (64-pin products)	TCR01		Timer counter register 01	TCR01	
F0183H						
F0184H	Same as RL78/G1A (64-pin products)	TCR02		Timer counter register 02	TCR02	
F0185H						
F0186H	Same as RL78/G1A (64-pin products)	TCR03		Timer counter register 03	TCR03	
F0187H						
F0188H	Same as RL78/G1A (64-pin products)	TCR04		Timer counter register 04	TCR04	
F0189H						
F018AH	Same as RL78/G1A (64-pin products)	TCR05		Timer counter register 05	TCR05	
F018BH						
F018CH	Same as RL78/G1A (64-pin products)	TCR06		Timer counter register 06	TCR06	
F018DH						
F018EH	Same as RL78/G1A (64-pin products)	TCR07		Timer counter register 07	TCR07	
F018FH						
F0190H	Same as RL78/G1A (64-pin products)	TMR00		Timer mode register 00	TMR00	
F0191H						
F0192H	Timer mode register 01 Note	TMR01		Timer mode register 01	TMR01	
F0193H						
F0194H	Timer mode register 02 Note	TMR02		Timer mode register 02	TMR02	
F0195H						
F0196H	Timer mode register 03 Note	TMR03		Timer mode register 03	TMR03	
F0197H						
F0198H	Same as RL78/G1A (64-pin products)	TMR04		Timer mode register 04	TMR04	
F0199H						
F019AH	Timer mode register 05 Note	TMR05		Timer mode register 05	TMR05	
F019BH						
F019CH	Timer mode register 06 Note	TMR06		Timer mode register 06	TMR06	
F019DH						
F019EH	Same as RL78/G1A (64-pin products)	TMR07		Timer mode register 07	TMR07	
F019FH						
F01A0H	Same as RL78/G1A (64-pin products)	TSR00L	TSR00	Timer status register 00	TSR00L	TSR00
F01A1H		–			–	
F01A2H	Same as RL78/G1A (64-pin products)	TSR01L	TSR01	Timer status register 01	TSR01L	TSR01
F01A3H		–			–	
F01A4H	Same as RL78/G1A (64-pin products)	TSR02L	TSR02	Timer status register 02	TSR02L	TSR02
F01A5H		–			–	
F01A6H	Same as RL78/G1A (64-pin products)	TSR03L	TSR03	Timer status register 03	TSR03L	TSR03
F01A7H		–			–	
F01A8H	Same as RL78/G1A (64-pin products)	TSR04L	TSR04	Timer status register 04	TSR04L	TSR04
F01A9H		–			–	
F01AAH	Same as RL78/G1A (64-pin products)	TSR05L	TSR05	Timer status register 05	TSR05L	TSR05
F01ABH		–			–	
F01ACH	Same as RL78/G1A (64-pin products)	TSR06L	TSR06	Timer status register 06	TSR06L	TSR06
F01ADH		–			–	
F01AEH	Same as RL78/G1A (64-pin products)	TSR07L	TSR07	Timer status register 07	TSR07L	TSR07
F01AFH		–			–	

Note The bit setting is different from that of RL78/G1A (64-pin products).

3. 4. 3. 3 Pull-up resistor option register (PUxx)

(1) 64-pin products

Symbol	7	6	5	4	3	2	1	0	Address	After Reset	R/W
PU0	0	0	0	0	PU03	PU02	PU01	PU00	F0030H	00H	R/W
PU1	0	0	0	PU14	PU13	PU12	PU11	PU10	F0031H	00H	R/W
PU4	0	0	0	0	0	PU42	PU41	PU40	F0034H	01H	R/W
PU7	0	0	0	0	PU73	PU72	PU71	PU70	F0037H	00H	R/W

Caution Be sure to clear bits 4 to 7 of the PU0 register, bits 5 to 7 of the PU1 register, bits 3 to 7 of the PU4 register, and bits 4 to 7 of the PU7 register to "0".

(2) 80-pin products

Symbol	7	6	5	4	3	2	1	0	Address	After Reset	R/W
PU0	0	0	0	PU04	PU03	PU02	PU01	PU00	F0030H	00H	R/W
PU1	0	0	PU15	PU14	PU13	PU12	PU11	PU10	F0031H	00H	R/W
PU4	0	0	0	0	0	PU42	PU41	PU40	F0034H	01H	R/W
<R> PU5	0	0	0	0	0	0	PU51	PU50	F0035H	00H	R/W
PU7	0	0	0	0	PU73	PU72	PU71	PU70	F0037H	00H	R/W
PU14	0	0	0	0	0	0	0	PU140	F003EH	00H	R/W

<R> **Caution Be sure to clear bits 5 to 7 of the PU0 register, bits 6 and 7of the PU1 register, bits 3 to 7 of the PU4 register, bits 2 to 7 of the PU5 register, bits 4 to 7 of the PU7 register, and bits 1 to 7 of the PU14 register to "0".**

3. 4. 3. 4 Port input mode register (PIMxx)

(1) 64-pin products

Symbol	7	6	5	4	3	2	1	0	Address	After Reset	R/W
PIM0	0	0	0	0	PIM03	0	PIM01	PIM00	F0040H	00H	R/W
PIM1	0	0	0	PIM14	0	0	PIM11	PIM10	F0041H	00H	R/W

<R> **Caution Be sure to clear bits 2 and 4 to 7 of the PIM0 register, and bits 2, 3 and 5 to 7 of the PIM1 register to "0".**

(2) 80-pin products

Symbol	7	6	5	4	3	2	1	0	Address	After Reset	R/W
<R> PIM0	0	0	0	PIM04	PIM03	0	PIM01	PIM00	F0040H	00H	R/W
PIM1	0	0	PIM15	PIM14	0	0	PIM11	PIM10	F0041H	00H	R/W

<R> **Caution Be sure to clear bits 2 and 5 to 7 of the PIM0 register, and bits 2, 3, 6 and 7 of the PIM1 register to "0".**

(1) X1 oscillation: **As of March, 2013(4/4)**

Manufacturer	Resonator	Part Number	SMD/ Lead	Frequency (MHz)	Flash operation mode Note 1	Recommended Circuit Constants Note 2 (reference)			Oscillation Voltage Range (V)	
						C1 (pF)	C2 (pF)	Rd (kΩ)	MIN.	MAX.
Nihon Dempa Kogyo Co., Ltd. Note 3	Crystal resonator	NX8045GB	SMD	8	LS	1	1	0	1.8	5.5
		NX8045GB	SMD	8	HS	1	1	0	2.4	5.5
		NX3225GB	SMD	16		2	2	0	2.4	5.5
		NX2520SA	SMD	20		1	1	0	2.7	5.5

<R> **Notes 1.** Set the flash operation mode by using CMODE1 and CMODE0 bits of the option byte (000C2H).

2. C1, C2 columns indicate a reference value.

3. When using these oscillators, contact Nihon Dempa Kogyo Co., Ltd. (http://www.ndk.com/jp/).

Remark Relationship between operation voltage width, operation frequency of CPU and operation mode is as below.

HS (High speed main) mode: 2.7 V ≤ V_{DD} ≤ 5.5 V@1 MHz to 32 MHz (When X1 oscillation: 1 MHz to 20 MHz)
2.4 V ≤ V_{DD} ≤ 5.5 V@1 MHz to 16 MHz

LS (Low speed main) mode: 1.8 V ≤ V_{DD} ≤ 5.5 V@1 MHz to 8 MHz

LV (Low voltage main) mode: 1.6 V ≤ V_{DD} ≤ 5.5 V@1 MHz to 4 MHz

- Format of Timer Mode Register mn (TMRmn) (3/4)

Address: F0190H, F0191H (TMR00) - F019EH, F019FH (TMR07) After reset: 0000H R/W

Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TMRmn (n = 2, 4, 6)	CKS mn1	CKS mn0	0	CCS mn	MAS TER mn	STS mn2	STS mn1	STS mn0	CIS mn1	CIS mn0	0	0	MD mn3	MD mn2	MD mn1	MD mn0

Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TMRmn (n = 1, 3)	CKS mn1	CKS mn0	0	CCS mn	SPLIT mn	STS mn2	STS mn1	STS mn0	CIS mn1	CIS mn0	0	0	MD mn3	MD mn2	MD mn1	MD mn0

Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TMRmn (n = 0, 5, 7)	CKS mn1	CKS mn0	0	CCS mn	0[Note]	STS mn2	STS mn1	STS mn0	CIS mn1	CIS mn0	0	0	MD mn3	MD mn2	MD mn1	MD mn0

CISmn1	CISmn0	Selection of TImn pin input valid edge
0	0	Falling edge
0	1	Rising edge
1	0	Both edges (when low-level width is measured) Start trigger: Falling edge, Capture trigger: Rising edge
1	1	Both edges (when high-level width is measured) Start trigger: Rising edge, Capture trigger: Falling edge
If both the edges are specified when the value of the STSmn2 to STSmn0 bits is other than 010B, set the CISmn1 to CISmn0 bits to 10B.		

<R> **Note** Bit 11 is fixed at 0 of read only, write is ignored.

Remark m: Unit number (m = 0), n: Channel number (n = 0 to 7 (however, timer input pin (TImn), timer output pin (TOmn): n = 0, 4, 7))

Operation mode (Value set by the MDmn3 to MDmn1 bits (see table above))	MD mn0	Setting of starting counting and interrupt
• Interval timer mode 0, 0, 0)	0	Timer interrupt is not generated when counting is started (timer output does not change, either).
• Capture mode (0, 1, 0)	1	Timer interrupt is generated when counting is started (timer output also changes).
• Event counter mode (0, 1, 1)	0	Timer interrupt is not generated when counting is started (timer output does not change, either).
• One-count mode Note 1 (1, 0, 0)	0	Start trigger is invalid during counting operation. At that time, interrupt is not generated, either.
	1	Start trigger is valid during counting operation Note 2. At that time, interrupt is not generated.
• Capture & one-count mode (1, 1, 0)	0	Timer interrupt is not generated when counting is started (timer output does not change, either). Start trigger is invalid during counting operation. At that time interrupt is not generated, either.
Other than above		Setting prohibited

Notes 1. In one-count mode, interrupt output (INTTMmn) when starting a count operation and TOmn output are not controlled.

2. If the start trigger (TSmn = 1) is issued during operation, the counter is initialized, an interrupt is generated, and recounting is started (does not occur the interrupt request). <R>

Remark m: Unit number (m = 0), n: Channel number (n = 0 to 7 (however, timer input pin (TImn), timer output pin (TOmn): n = 0, 4, 7))

<R> 3. 6. 3. 15 Registers controlling port functions of pins to be used for timer I/O

Using port pins for the timer array unit functions requires setting of the registers that control the port functions multiplexed on the target pins (port mode register (PMxx), port register (Pxx), and port mode control register (PMCxx)). For details, see **3. 4. 3. 1 Port mode registers (PMxx)**, **3. 4. 3. 2 Port registers (Pxx)**, and **3. 4. 3. 6 Port mode control registers (PMCxx)**.

For details of setting example, see **6. 3. 15 Registers controlling port functions of pins to be used for timer I/O** in **RL78/G1A Hardware User's Manual (R01UH0305E)**.

3. 11. 3. 8 Conversion result comparison upper limit setting register (ADUL)

The bit setting is same as that of RL78/G1A (64-pin products). For details, see **11. 3. 8 Conversion result comparison upper limit setting register (ADUL)** in **RL78/G1A Hardware User's Manual (R01UH0305E)**.

3. 11. 3. 9 Conversion result comparison lower limit setting register (ADLL)

The bit setting is same as that of RL78/G1A (64-pin products). For details, see **11. 3. 9 Conversion result comparison lower limit setting register (ADLL)** in **RL78/G1A Hardware User's Manual (R01UH0305E)**.

3. 11. 3. 10 A/D test register (ADTES)

The bit setting is same as that of RL78/G1A (64-pin products). For details, see **11. 3. 10 A/D test register (ADTES)** in **RL78/G1A Hardware User's Manual (R01UH0305E)**.

<R> 3. 11. 3. 11 Registers controlling port function of analog input pins

Set up the registers for controlling the functions of the ports shared with the analog input pins of the A/D converter (port mode registers (PMxx), port mode control registers (PMCxx), and A/D port configuration register (ADPC)).

For details, see as follows.

- **3. 4. 3. 1 Port mode registers (PMxx)**
- **3. 4. 3. 6 Port mode control registers (PMCxx)**
- **3. 4. 3. 7 A/D port configuration register (ADPC)**

For details of setting example, see **11. 3. 11 Registers controlling port function of analog input pins** in **RL78/G1A Hardware User's Manual (R01UH0305E)**.

3. 12. 1 Functions of serial array unit

Each serial interface supported by the RL78/G1E (64-pin products, 80-pin products) has the following features.

3. 12. 1. 1 3-wire serial I/O (CSI00, CSI10, CSI20, CSI21)

Data is transmitted or received in synchronization with the serial clock (SCK) output from the master channel.

3-wire serial communication is clocked communication performed by using three communication lines: one for the serial clock (SCK), one for transmitting serial data (SO), one for receiving serial data (SI).

For details about the settings, see **3. 12. 5 Operation of 3-Wire serial I/O (CSI00, CSI10, CSI20, CSI21) Communication**.

[Data transmission/reception]

- Data length of 7 or 8 bits
- Phase control of transmit/receive data
- MSB/LSB first selectable
- Level setting of transmit/receive data

[Clock control]

- Master/slave selection
- Phase control of I/O clock
- Setting of transfer period by prescaler and internal counter of each channel
- Maximum transfer rate During master communication (CSI00): Max. $f_{CLK}/2$ **Note**
  During master communication (other than CSI00): Max. $f_{CLK}/4$ **Note**
  During slave communication: Max. $f_{MCK}/6$ **Note**

[Interrupt function]

- Transfer end interrupt/buffer empty interrupt

[Error detection flag]

- Overrun error

In addition, CSI00 of following channels supports the SNOOZE mode. When SCK input is detected while in the STOP mode, the SNOOZE mode makes data reception that does not require the CPU possible. Only CSI00 can be specified for asynchronous reception.

Note Use the clocks within a range satisfying the SCK cycle time (t_{KCY}) characteristics (see **CHAPTER 5 ELECTRICAL SPECIFICATIONS**).

CHAPTER 4 ANALOG BLOCK

4. 1 Configurable Amplifier

The RL78/G1E (64-pin products, 80-pin products) has three on-chip configurable amplifier channels.

4. 1. 1 Overview of configurable amplifier features

By specifying settings in the SPI control registers, the configurable amplifiers can be used to realize the following features:

- Single-channel operation
  - Non-inverting amplifier
    - The gain can be specified between 9.5 dB and 40.1 dB in 18 steps
    - Four operating modes are available
    - Includes a power-off function
  - Inverting amplifier
    - The gain can be specified between 6 dB and 40 dB in 18 steps
    - Four operating modes are available
    - Includes a power-off function
  - Differential amplifier
    - The gain can be specified between 6 dB and 40 dB in 18 steps
    - Four operating modes are available
    - Includes a power-off function
  - Transimpedance amplifier
    - The feedback resistance can be specified between 20 kΩ and 640 kΩ in 6 steps
    - Four operating modes are available
    - Includes a power-off function

- Multiple-channel operation
  - Instrumentation amplifier
    - The gain can be specified between 20 dB and 54 dB in 18 steps
    - Four operating modes are available
    - Includes a power-off function

And also, the DACn_OUT output signals can be used as the reference voltage for each configurable amplifier.
If D/A converter is powered off, the external reference voltage is to be input to DACn_OUT/VREFINn pin.
For details about use of D/A converter, see **4. 3 D/A Converter**.

Remark n = 1 to 3

(2) Configuration register 2 (CONFIG2)

This register is used to turn on or off each switch of configurable amplifiers Ch1 to Ch3.

Reset signal input clears this register to 00H.

Address: 01H After reset: 00H R/W

	7	6	5	4	3	2	1	0
CONFIG2	0	SW31	SW32	SW33	0	SW02	SW01	SW00

SW31	Control of SW31
0	Turn off SW31.
1	Turn on SW31.

SW32	Control of SW32
0	Turn off SW32.
1	Turn on SW32.

SW33	Control of SW33
0	Turn off SW33.
1	Turn on SW33.

SW02	Control of SW02
0	Turn off SW02.
1	Turn on SW02.

SW01	Control of SW01
0	Turn off SW01.
1	Turn on SW01.

SW00	Control of SW00
0	Turn off SW00.
1	Turn on SW00.

Remark Bits 7 and 3 can be set to 1, but this has no effect on the function.

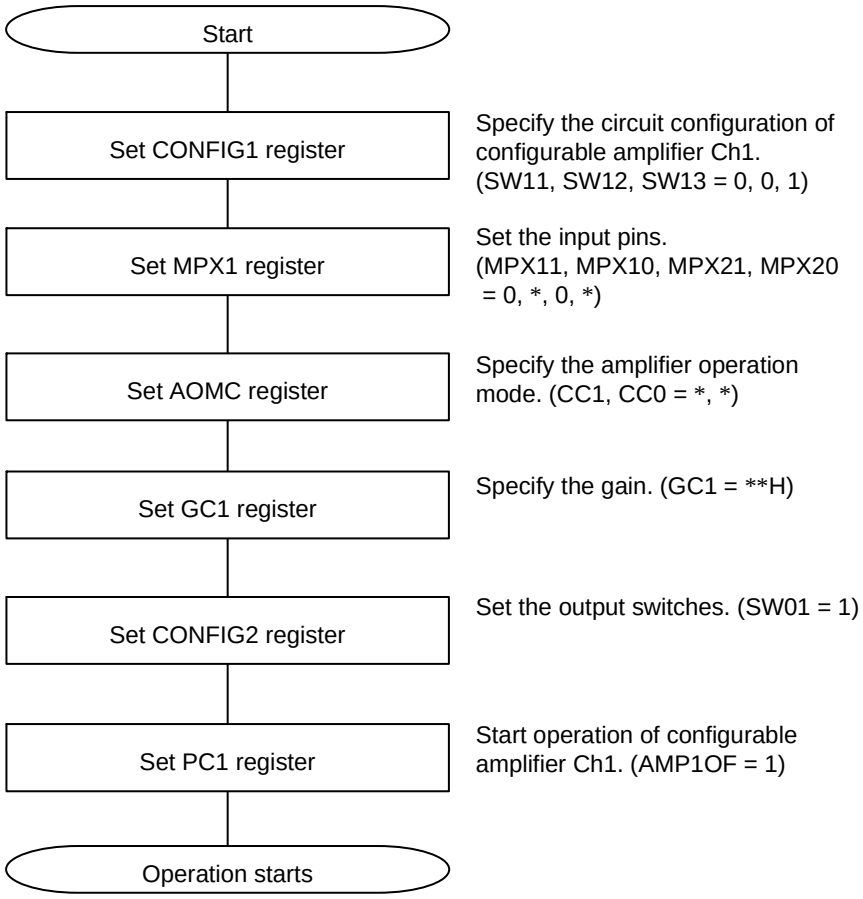
Table 4-9. Feedback Resistance of Configurable Amplifier Ch3 (Transimpedance Amplifier)

AMPG34	AMPG33	AMPG32	AMPG31	AMPG30	Feedback Resistance of Configurable Amplifier Ch3 (Typ.)
0	0	0	0	0	20 kΩ
0	0	0	0	1	
0	0	0	1	0	
0	0	0	1	1	40 kΩ
0	0	1	0	0	
0	0	1	0	1	
0	0	1	1	0	80 kΩ
0	0	1	1	1	
0	1	0	0	0	
0	1	0	0	1	160 kΩ
0	1	0	1	0	
0	1	0	1	1	
0	1	1	0	0	320 kΩ
0	1	1	0	1	
0	1	1	1	0	
0	1	1	1	1	640 kΩ
1	0	0	0	0	
1	0	0	0	1	
Other than above					Setting prohibited

(3) Procedure when using the amplifiers as differential amplifiers

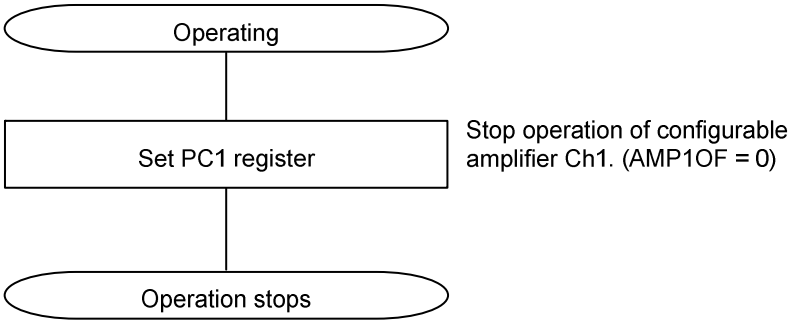
When using the configurable amplifiers together as a differential amplifier, follow the procedures below to start and stop the amplifier.

Example of procedure for starting configurable amplifier Ch1 (differential amplifier)



Remark *: don't care

Example of procedure for stopping configurable amplifier Ch1 (differential amplifier)



<R> **(6) Communication between devices at different potential (1.8 V, 2.5 V or 3 V) (UART mode) (output from dedicated baud rate generator) (2/2)**

(T_A = –40 to +85°C, 1.8 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V) (2/2)

Parameter	Symbol	Conditions		HS Note 1		LS Note 2		LV Note 3		Unit
				MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Transfer rate		Transmission	4.0V ≤ V_{DD} ≤ 5.5V, 2.7V ≤ Vb ≤ 4.0V		**Note 4**		**Note 4**		**Note 4**	bps
			Theoretical value of the maximum transfer rate: Cb = 50 pF, Rb = 1.4 kΩ, Vb = 2.7 V		2.8 Note 5		2.8 Note 5		2.8 Note 5	Mbps
			2.7V ≤ V_{DD} < 4.0V, 2.3V ≤ Vb ≤ 2.7V		**Note 7**		**Note 7**		**Note 7**	bps
			Theoretical value of the maximum transfer rate: Cb = 50 pF, Rb = 2.7 kΩ, Vb = 2.3 V		1.2 Note 8		1.2 Note 8		1.2 Note 8	Mbps
			1.8V ≤ V_{DD} < 3.3V, 1.6V ≤ Vb ≤ 2.0V Note 5		**Note 9**		**Note 9**		**Note 9**	bps
			Theoretical value of the maximum transfer rate: Cb = 50 pF, Rb = 5.5 kΩ, Vb = 1.6 V		0.43 Note 10		0.43 Note 10		0.43 Note 10	Mbps

Notes 1. HS is condition of HS (high-speed main) mode.

2. LS is condition of LS (low-speed main) mode.

3. LV is condition of LV (low-voltage main) mode.

4. The smaller value derived by using f_{MCK}/6 or the following expression is the valid maximum transfer rate.
Expression for calculating the transfer rate when 4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ Vb ≤ 4.0 V

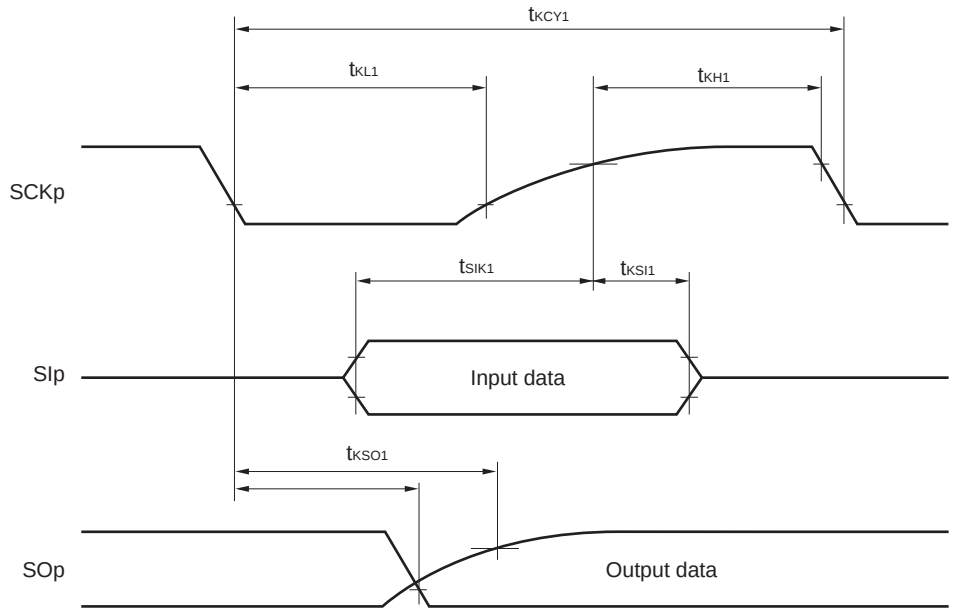
$$\text{Maximum transfer rate} = \frac{1}{\{-Cb \times Rb \times \ln(1 - \frac{2.2}{Vb})\} \times 3} \text{ [bps]}$$

$$\text{Baud rate error (theoretical value)} = \frac{\frac{1}{\text{Transfer rate} \times 2} - \{-Cb \times Rb \times \ln(1 - \frac{2.2}{Vb})\}}{(\frac{1}{\text{Transfer rate}}) \times \text{Number of transferred bits}} \times 100 \text{ [\%]}$$

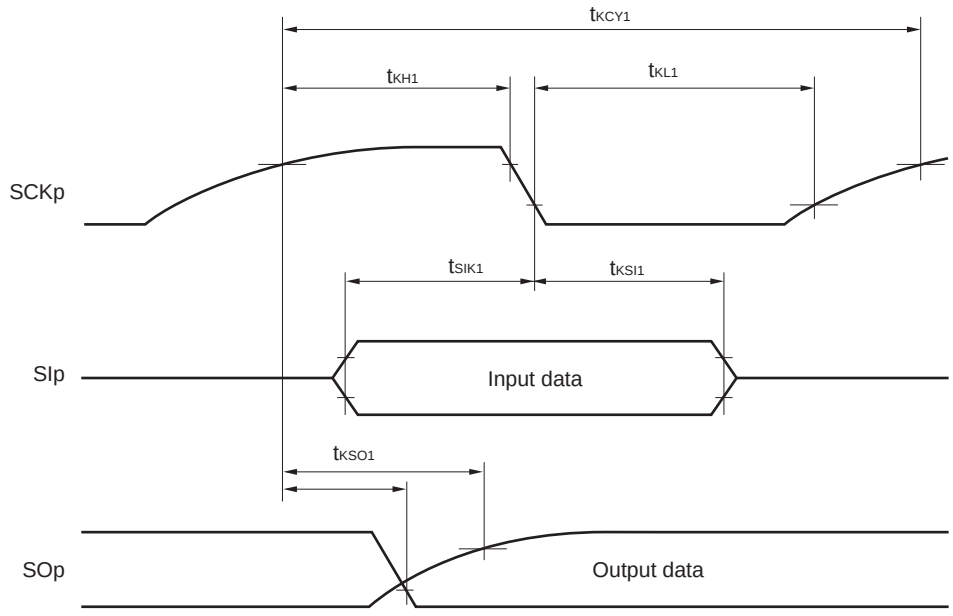
* This value is the theoretical value of the relative difference between the transmission and reception sides.

(Other **Notes** and **Caution** are listed on the next page.)

CSI mode serial transfer timing: master mode (during communication between devices at different potential)
(when DAPmn = 0 and CKPmn = 0 or DAPmn = 1 and CKPmn = 1)



CSI mode serial transfer timing: master mode (during communication between devices at different potential)
(when DAPmn = 0 and CKPmn = 1 or DAPmn = 1 and CKPmn = 0)



Remarks 1. p: CSI number (p = 00, 10, 20), m: Unit number, n: Channel number (mn = 00, 10, 20), g: PIM and POM numbers (g = 0, 1)

2. CSI21 cannot communicate with a device at different potential. Use other CSI channels for communication between devices at different potential.

<R> (3) When reference voltage (+) = AV_{DD} (ADREFP1 = 0, ADREFP0 = 0), reference voltage (–) = AV_{SS} (ADREFM = 0), target for conversion: ANI0 to ANI4 (ANI pins that use AV_{DD} as their power source)

(T_A = –40 to +85°C, 1.6 V ≤ V_{DD} ≤ 5.5 V, 1.6 V ≤ AV_{DD} ≤ 3.6 V, AV_{DD} ≤ V_{DD}, V_{SS} = 0 V, AV_{SS} = 0 V, reference voltage (+) = AV_{DD}, reference voltage (–) = AV_{SS} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Resolution	R_{ES}		2.4 V ≤ AV_{DD} ≤ 3.6 V	8		12	bit
			1.8 V ≤ AV_{DD} ≤ 3.6 V	8		10 Note 1	
			1.6 V ≤ AV_{DD} ≤ 3.6 V	8 Note 2			
Overall error Note 3	AINL	12-bit resolution	2.4 V ≤ AV_{DD} ≤ 3.6 V			±7.5	LSB
		10-bit resolution	1.8 V ≤ AV_{DD} ≤ 3.6 V			±5.5	
		8-bit resolution	1.6 V ≤ AV_{DD} ≤ 3.6 V			±3.0	
Conversion time	t_{CONV}	ADTYP = 0, 12-bit resolution	2.4 V ≤ AV_{DD} ≤ 3.6 V	3.375			μs
		ADTYP = 0, 10-bit resolution Note 1	1.8 V ≤ AV_{DD} ≤ 3.6 V	6.75			
		ADTYP = 0, 8-bit resolution Note 2	1.6 V ≤ AV_{DD} ≤ 3.6 V	13.5			
		ADTYP = 1, 8-bit resolution	2.4 V ≤ AV_{DD} ≤ 3.6 V	2.5625			
			1.8 V ≤ AV_{DD} ≤ 3.6 V	5.125			
			1.6 V ≤ AV_{DD} ≤ 3.6 V	10.25			
Zero-scale error Notes 3	EZS	12-bit resolution	2.4 V ≤ AV_{DD} ≤ 3.6 V			±6.0	LSB
		10-bit resolution	1.8 V ≤ AV_{DD} ≤ 3.6 V			±5.0	
		8-bit resolution	1.6 V ≤ AV_{DD} ≤ 3.6 V			±2.5	
Full-scale error Notes 3	EFS	12-bit resolution	2.4 V ≤ AV_{DD} ≤ 3.6 V			±6.0	LSB
		10-bit resolution	1.8 V ≤ AV_{DD} ≤ 3.6 V			±5.0	
		8-bit resolution	1.6 V ≤ AV_{DD} ≤ 3.6 V			±2.5	
Integral linearity error Note 3	ILE	12-bit resolution	2.4 V ≤ AV_{DD} ≤ 3.6 V			±3.0	LSB
		10-bit resolution	1.8 V ≤ AV_{DD} ≤ 3.6 V			±2.0	
		8-bit resolution	1.6 V ≤ AV_{DD} ≤ 3.6 V			±1.5	
Differential linearity error Note 3	DLE	12-bit resolution	2.4 V ≤ AV_{DD} ≤ 3.6 V			±2.0	LSB
		10-bit resolution	1.8 V ≤ AV_{DD} ≤ 3.6 V			±2.0	
		8-bit resolution	1.6 V ≤ AV_{DD} ≤ 3.6 V			±1.5	
Analog input voltage	V_{AIN}			0		AV_{DD}	V

Notes 1. The lower 2 bits of the ADCR register cannot be used.

2. The lower 4 bits of the ADCR register cannot be used.

3. Excludes quantization error (±1/2 LSB).

B. 2 Revision History of Preceding Editions

Here is the revision history of the preceding editions. Chapter indicates the chapter of each edition.

(1/6)

Edition	Description	Chapter
Rev.1.00	The structure of **CHAPTERS** and **Sessions** are drastically changed.	Whole pages
	Modification of **1. 1 Features**	**CHAPTER 1 OUTLINE**
	Addition of Packaging, modification of Part Numbers and addition of **Cautions** in **1. 2 List of Part Numbers**	
	Modification of **Note 7.** for 64-pin products in **1. 3 Pin Configuration**	
	Modification of **Note 6.** for 80-pin products in **1. 3 Pin Configuration**	
	Addition of Items and **Notes** in **1. 6 Outline of Functions**	
	Error correction of the descriptions in **1. 6 Outline of Functions**	
	Modification of the tables for **Comparison of port functions with RL78/G1A** in **2. 1 Pin Functions in Microcontroller Block**	**CHAPTER 2 PIN FUNCTIONS**
	Error correction of the descriptions in **2. 1. 1 Port functions**	
	Addition of the descriptions in **2. 1. 2 Functions other than port Functions**	
	Error correction of the descriptions in **2. 2 Pin Functions in Analog Block**	
	Addition of **Notes** about the pin of $\overline{\text{ARESET}}$ in **2. 3 Recommended Connection of Unused Pins**	
	Addition of the descriptions for the pin of $\overline{\text{RESET}}$ and the pin of $\overline{\text{ARESET}}$ in **2. 5 Instruction of Pin Functions**	
	Addition of the items listed on the tables in **3. 2 Comparison of Each Function with RL78/G1A (64-pin products)**	**CHAPTER 3 MICROCONTROLLER BLOCK**
	Error correction of the descriptions on the tables in **3. 2 Comparison of Each Function with RL78/G1A (64-pin products)**	
	Modification of the tables for **List of Differences in Special Function Registers (SFRs)** in **3. 3. 2. 4 Special function registers (SFRs)**	
	Modification of the tables for **List of Differences in Expanded Special Function Registers (2nd SFRs)** in **3. 3. 2. 5 Expanded special function registers (2nd SFRs)**	
	Addition of the descriptions for each port in **3. 4. 2 Port configuration**	
	Error correction of the descriptions for each port in **3. 4. 2 Port configuration**	
	Addition of registers listed in **3. 4. 3 Registers controlling port functions**	
	Modification of the frequency for oscillation about the function of high-speed on-chip oscillator and addition of the table about the frequency for oscillation in **3. 5. 1 Functions of clock generator**	
	Addition of the registers listed in **3. 5. 3 Registers controlling clock generator**	
	Error correction of the descriptions about a crystal resonator in **3. 5. 7 Resonator and oscillator constants**	
	Addition of “Port mode control register” to **Table 3-8.**	
	Modification of the figures for Block Diagram on **Figure 3-4.** and **Figure 3-5.** in **3. 6. 2 Configuration of timer array unit**	
	Addition of the registers listed in **3. 6. 3 Registers controlling timer array unit**	
	Addition of the registers listed in **3. 8. 3 Registers controlling 12-bit interval timer**	