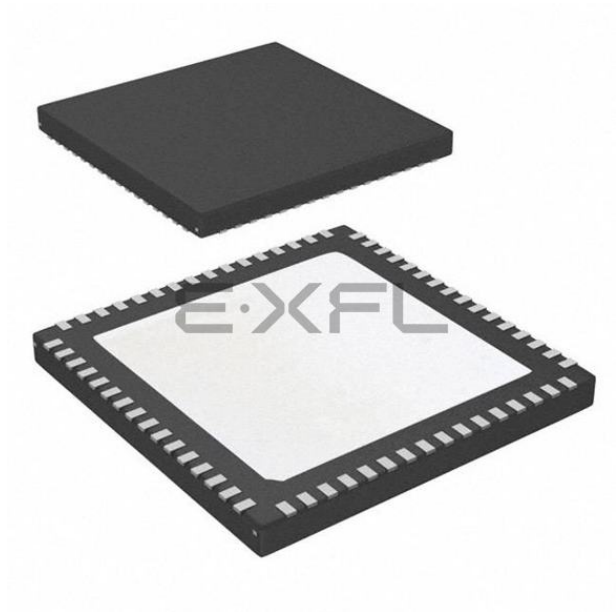
Renesas Electronics America Inc - R5F10FLDDNA#W0 Datasheet



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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	RL78
Core Size	16-Bit
Speed	32MHz
Connectivity	CSI, I²C, LINbus, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	20
Program Memory Size	48KB (48K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	3K x 8
Voltage - Supply (Vcc/Vdd)	1.6V ~ 5.5V
Data Converters	A/D 13x8/12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-WFQFN Exposed Pad
Supplier Device Package	64-WQFN (9x9)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f10flddna-w0

CHAPTER 1 OUTLINE

<R> 1. 1 Features

The RL78/G1E is a multi-chip package (MCP) device that integrates a chip of an analog block and a chip of 16-bit microcontroller block in a single package. The chip of analog block features a range of front-end analog circuits for small sensor signal processing such as a configurable gain amplifier, gain adjustment amplifier, filter circuit, D/A converter, and temperature sensor. The chip of 16-bit microcontroller block corresponds to the RL78/G1A (64-pin products).

1. 1. 1 Microcontroller block

Low power consumption technology by standby function

- HALT mode
- STOP mode
- SNOOZE mode

RL78 CPU core

- CISC architecture with 3-stage pipeline
- Minimum instruction execution time: Can be changed from 0.03125 μs (32 MHz operation with high-speed on-chip oscillator) to 0.05 μs (20 MHz operation with high-speed system clock)
- Address space: 1 MB
- General-purpose registers: (8-bit register × 8) × 4 banks
- On-chip RAM: 2 to 4 KB

Code flash memory

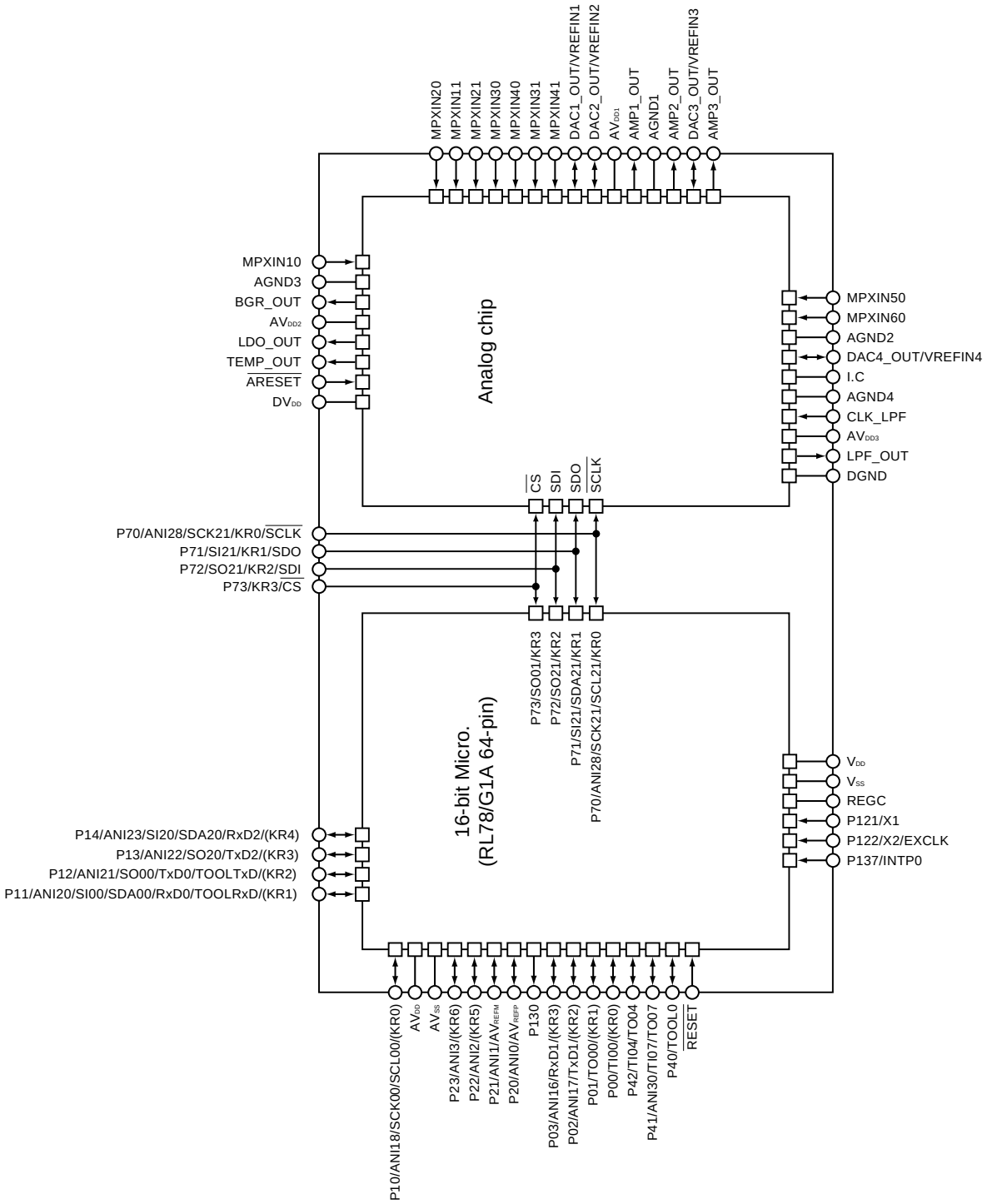
- Code flash memory: 32 to 64 KB
- Block size: 1 KB
- Prohibition of block erase and rewriting (security function)
- On-chip debug function
- Self-programming (with boot swap function/flash shield window function)

Data flash memory

- Data flash memory: 4 KB
- Back ground operation (BGO): Instructions can be executed from the program memory while rewriting the data flash memory.
- Number of rewrites: 1,000,000 times (TYP.)
- Voltage of rewrites: V_{DD} = 1.8 to 5.5 V

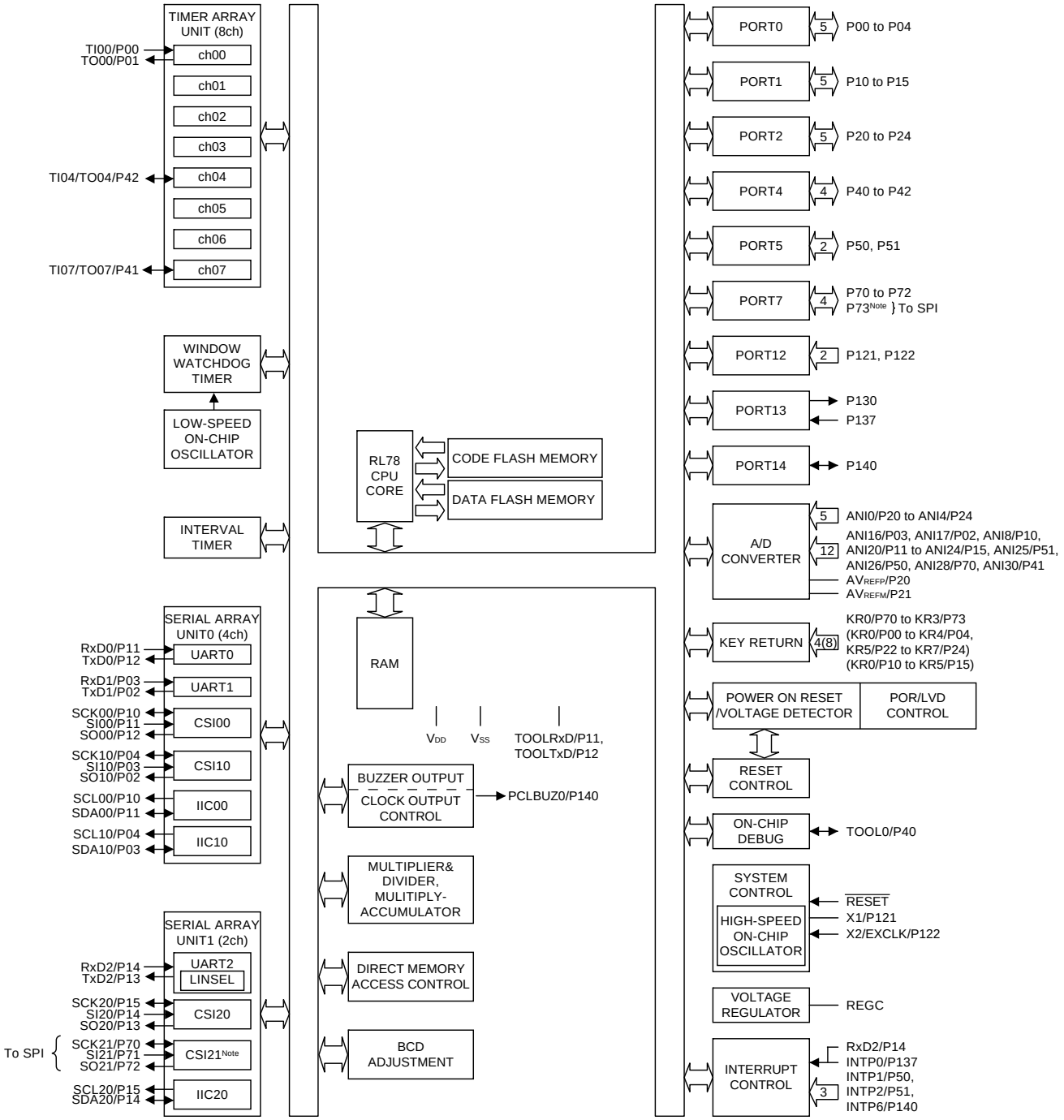
<R> 1. 5 Block Diagram

1. 5. 1 64-pin products



Remark The RL78/G1E (64-pin products) is a multi-chip package (MCP) device that integrates a chip of an analog block and a chip of 16-bit microcontroller block in a single package.

<R> **(1) Block diagram in microcontroller block (80-pin products)**



Note Connected inside the package.

Table 1-1 Outline of Functions (Microcontroller Block) (2/2)

Item		64-pin products	80-pin products
		R5F10FLx	R5F10FMx
Serial interface		• 64-pin products CSI: 1 channel / simplified I^2C: 1 channel / UART: 1 channel UART: 1 channel CSI: 1 channel / UART (LIN-bus supported): 1 channel • 80-pin products CSI: 1 channel / simplified I^2C: 1 channel / UART: 1 channel CSI: 1 channel / simplified I^2C: 1 channel / UART: 1 channel CSI: 2 channels / simplified I^2C: 1 channel / UART (LIN-bus supported): 1 channel	
	I^2C bus	–	
Multiplier and divider / multiply accumulator		Multiplier: 16 bits × 16 bits (Unsigned or signed) Divider: 32 bits ÷ 32 bits (Unsigned) Multiply accumulator: 16 bits × 16 bits + 32 bits (Unsigned or signed)	
DMA controller		2 channels	
Vectored interrupt sources	Internal	25	
	External	2	5
Key interrupt		4 ch (7) Note 1	4 ch (8) Note 1
Reset		• Reset by $\overline{\text{RESET}}$ pin • Internal reset by watchdog timer • Internal reset by power-on-reset • Internal reset by voltage detector • Internal reset by illegal instruction execution Note 2 • Internal reset by RAM parity error • Internal reset by illegal-memory access	
Power-on-reset circuit		• Power-on-reset: 1.51 ±0.03 V • Power-down-reset: 1.50 ±0.03 V	
Voltage detector		Detection level: 3 stages	
On-chip debug function		Provided	

<R>

Notes 1. The number in parentheses is the channels of key interrupt when using the peripheral I/O redirection register (PIOR).

2. The illegal instruction is generated when instruction code FFH is executed. Rest by the illegal instruction execution is not issued by emulation with the in-circuit emulator or on-chip debug emulator.

(2/2)

<R>

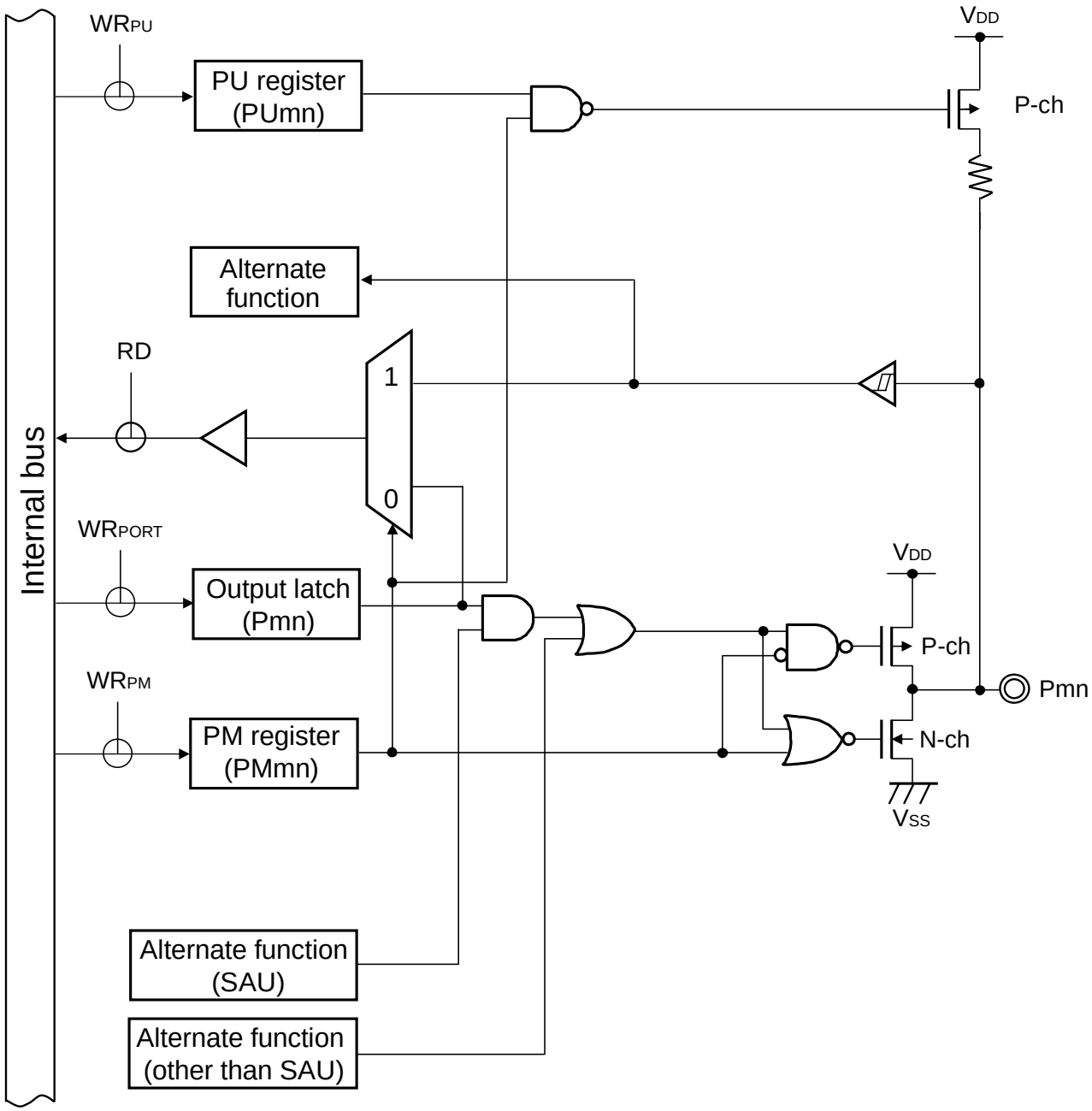
Function Name	Pin Type	I/O	After Reset	Alternate Function	Function
P50	7-3-2	I/O	Analog input port	ANI26/INTP1	Port 5. 2-bit I/O port. Output of P50 can be set to N-ch open-drain output (V_{DD} tolerance). P50 and P51 can be set to analog input. Note 1 Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by software setting at input port.
P51	7-3-1			ANI25/INTP2	
P70	7-3-1	I/O	Analog input port	ANI28/KR0/ SCK21/$\overline{\text{SCLK}}$ Note2	Port 7. 4-bit I/O port. P70 can be set to analog input. Note 1 Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by software setting at input port.
P71	7-1-2		Input port	KR1/SI21/SDO Note2	
P72	7-1-1			KR2/SO21/SDI Note2	
P73				KR3/$\overline{\text{CS}}$ Note2	
P121	2-2-1	Input	Input port	X1	Port 12. 2-bit input port.
P122				X2/EXCLK	
P130	1-1-1	Output	Output port	–	Port 13. 1-bit output port and 1-bit input port.
P137	2-1-2	Input	Input port	INTP0	
P140	7-1-1	I/O	Input port	PCLBUZ0/INTP6	Port 14. 1-bit I/O port. Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting at input port.
RESET	2-1-1	Input	–	–	Input only pin for external reset. When external reset is not used, connect this pin to V_{DD} directly or via a resistor.

<R> **Notes 1.** Digital or analog for each pin can be selected with the port mode control register x (PMCx) (can be set in 1-bit units).

2. $\overline{\text{SCLK}}$, SDO, SDI, $\overline{\text{CS}}$ represent the pin functions of analog block. P70 to P73 which are connected to the pins of the chip of analog block inside the package have some alternate functions for analog block.

<R>

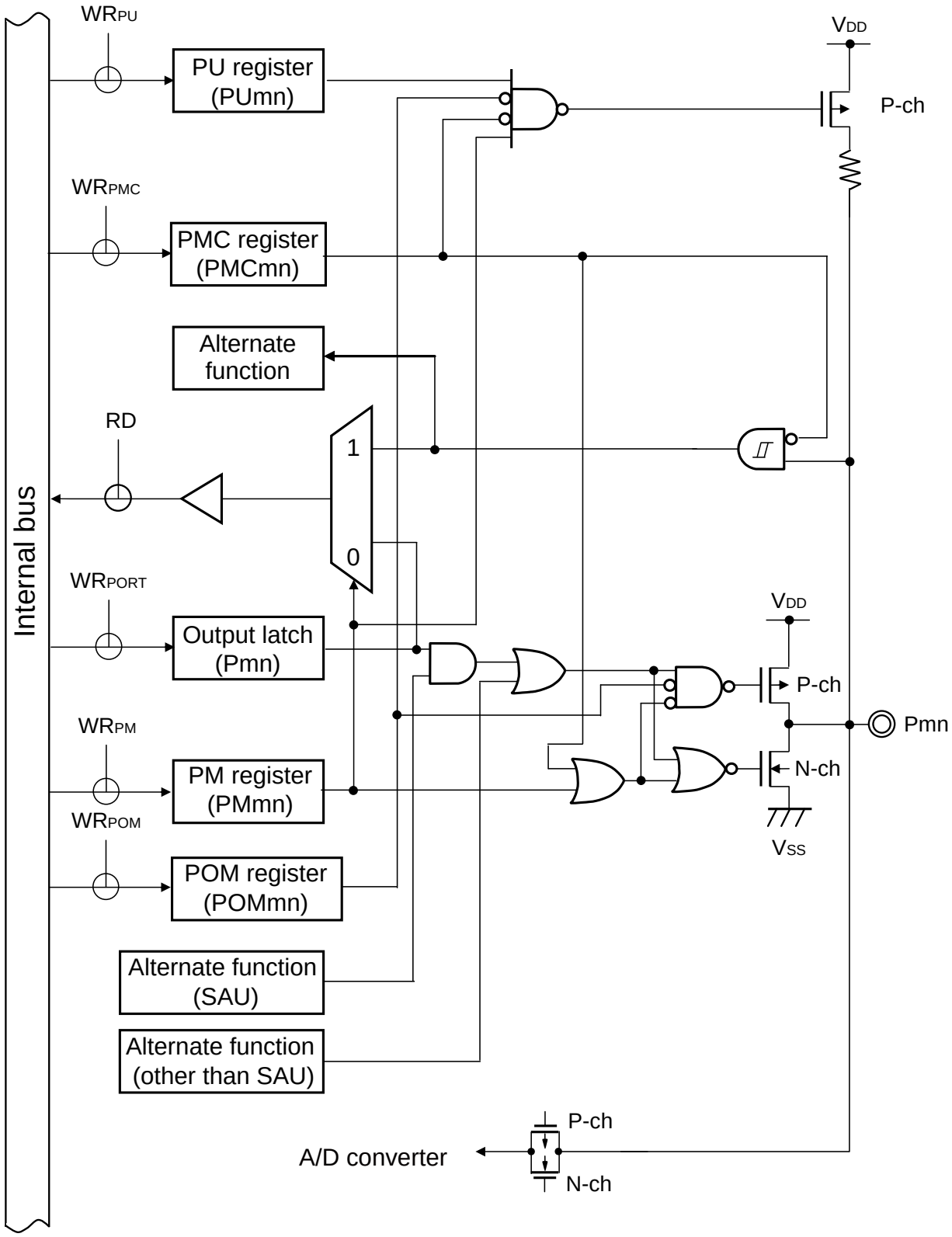
Figure 2-7. Pin Block Diagram for Pin Type 7-1-2



Remarks 1. For alternate functions, see **2. 1. 1 Port functions**.

2. SAU: Serial array unit

<R> **Figure 2-9. Pin Block Diagram for Pin Type 7-3-2**



Remarks 1. For alternate functions, see **2. 1. 1 Port functions**.

2. SAU: Serial array unit

2. 5. 24 AGND1

This is the ground pin for configurable amplifiers Ch1 to Ch3.

2. 5. 25 AV_{DD1}

This is the power supply pin for configurable amplifiers Ch1 to Ch3.

2. 5. 26 AGND3

This is the GND pin for variable output voltage regulator and reference voltage generator.

2. 5. 27 BGR_OUT

This is the output pin for reference voltage generator.

2. 5. 28 AV_{DD2}

This is the power supply pin for variable output voltage regulator and reference voltage generator.

2. 5. 29 LDO_OUT

This is the output pin for variable output voltage regulator.

2. 5. 30 TEMP_OUT

This is the output pin for temperature sensor.

2. 5. 31 $\overline{\text{ARESET}}$

This is the active-low system reset input pin for the function of analog block. After turning on DV_{DD}, it is necessary to input the external reset signal to this pin before starting SPI communication. When controlling the external reset signal by the microcontroller block of this package, it is recommended to directly connect this pin to P130 which is to be a low-level output port on reset. If the resource pin of $\overline{\text{ARESET}}$ is to be Hi-Z at a short moment, this pin must be connected to DGND via a resistor. For details of the functions, see **4. 10 Analog Reset**.

2. 5. 32 DV_{DD}

This is the power supply pin for SPI.

2. 5. 33 $\overline{\text{SCLK}}$

This is the serial clock input pin for SPI.

2. 5. 34 SDO

This is the serial data output pin for SPI.

Table 3-4. List of Differences in Expanded Special Function Registers (2nd SFRs) (3/6)

Address	RL78/G1E (80-pin products)			RL78/G1A (64-pin products)		
	2nd SFRs Name	Symbol		2nd SFRs Name	Symbol	
F0110H	Same as RL78/G1A (64-pin products)	SMR00		Serial mode register 00	SMR00	
F0111H						
F0112H	Serial mode register 01 Note	SMR01		Serial mode register 01	SMR01	
F0113H						
F0114H	Same as RL78/G1A (64-pin products)	SMR02		Serial mode register 02	SMR02	
F0115H						
F0116H	Serial mode register 03 Note	SMR03		Serial mode register 03	SMR03	
F0117H						
F0118H	Same as RL78/G1A (64-pin products)	SCR00		Serial communication operation setting register 00	SCR00	
F0119H						
F011AH	Serial communication operation setting register 01 Note	SCR01		Serial communication operation setting register 01	SCR01	
F011BH						
F011CH	Same as RL78/G1A (64-pin products)	SCR02		Serial communication operation setting register 02	SCR02	
F011DH						
F011EH	Serial communication operation setting register 03 Note	SCR03		Serial communication operation setting register 03	SCR03	
F011FH						
F0120H	Same as RL78/G1A (64-pin products)	SE0L	SE0	Serial channel enable status register 0	SE0L	SE0
F0121H		—			—	
F0122H	Same as RL78/G1A (64-pin products)	SS0L	SS0	Serial channel start register 0	SS0L	SS0
F0123H		—			—	
F0124H	Same as RL78/G1A (64-pin products)	ST0L	ST0	Serial channel stop register 0	ST0L	ST0
F0125H		—			—	
F0126H	Same as RL78/G1A (64-pin products)	SPS0L	SPS0	Serial clock select register 0	SPS0L	SPS0
F0127H		—			—	
F0128H	Same as RL78/G1A (64-pin products)	SO0		Serial output register 0	SO0	
F0129H						
F012AH	Same as RL78/G1A (64-pin products)	SOE0L	SOE0	Serial output enable register 0	SOE0L	SOE0
F012BH		—			—	
F0134H	Same as RL78/G1A (64-pin products)	SOL0L	SOL0	Serial output level register 0	SOL0L	SOL0
F0135H		—			—	
F0138H	Same as RL78/G1A (64-pin products)	SSC0L	SSC0	Serial standby control register 0	SSC0L	SSC0
		—			—	
F0140H	Same as RL78/G1A (64-pin products)	SSR10L	SSR10	Serial status register 10	SSR10L	SSR10
F0141H		—			—	
F0142H	Same as RL78/G1A (64-pin products)	SSR11L	SSR11	Serial status register 11	SSR11L	SSR11
F0143H		—			—	

Note The bit setting is different from that of RL78/G1A (64-pin products).

3. 6. 2 Configuration of timer array unit

Timer array unit includes the following hardware.

Table 3-8. Configuration of Timer Array Unit

Item	Configuration
Timer/counter	Timer count register mn (TCRmn)
Register	Timer data register mn (TDRmn)
Timer input	TI00, TI04, TI07, RxD2 pin (for LIN-bus)
Timer output	TO00, TO04, TO07, output controller
Control registers	<Registers of unit setting block> • Peripheral enable register 0 (PER0) • Timer clock select register m (TPSm) • Timer channel enable status register m (TEm) • Timer channel start register m (TSm) • Timer channel stop register m (TTm) • Timer input select register 0 (TIS0) • Timer output enable register m (TOEm) • Timer output register m (TOm) • Timer output level register m (TOLm) • Timer output mode register m (TOMm)
	<Registers of each channel> • Timer mode register mn (TMRmn) • Timer status register mn (TSRmn) • Input switch control register (ISC) • Noise filter enable register 1 (NFEN1) • Port mode control register (PMCxx) • Port mode register (PMxx) • Port register (Pxx)

Remark m: Unit number (m = 0), n: Channel number (n = 0 to 7)

<R> **Notes 1.** The SCR00, SCR02, and SCR10 registers only. Others are fixed to 0.

2. The SCR00 and SCR01 registers only. Others are fixed to 1.

3. When using CSImn not with EOCmn = 0, error interrupt INTSRE0 may be generated.

Caution Be sure to clear bits 3, 6, and 11 to "0". Be sure to set bit 2 to "1".

Remark m: Unit number (m = 0, 1)

n: Channel number (n = 0 to 3)

p: CSI number (80-pin products: p = 00, 10, 20, 21 64-pin products: p = 00, 21)

3. 17. 3. 5 Peripheral I/O redirection register (PIOR)

Address: F0077H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
PIOR	0	0	0	0	0	0	PIOR1	PIOR0

Function	64-pin products				80-pin products			
	Setting value of PIOR1, PIOR0				Setting value of PIOR1, PIOR0			
	0, 0	0, 1	1, 0	1, 1	0, 0	0, 1	1, 0	1, 1
KR0	P70	Setting prohibited	P00	P10	P70	Setting prohibited	P00	P10
KR1	P71		P01	P11	P71		P01	P11
KR2	P72		P02	P12	P72		P02	P12
KR3	P73		P03	P13	P73		P03	P13
KR4	–		–	P14	–		P04	P14
KR5	–		P22	–	–		P22	P15
KR6	–		P23	–	–		P23	–
KR7	–		–	–	–		P24	–

3. 17. 4 Key interrupt operation

See **17. 4 Key Interrupt Operation** in **RL78/G1A Hardware User's Manual (R01UH0305E)**.

3. 21 Voltage Detector

<R> **3. 21. 1 Functions of voltage detector**

The operation mode and detection voltages (V_{LVDH}, V_{LVDL}, V_{LVD}) for the voltage detector is set by using the option byte (000C1H).

The voltage detector (LVD) has the following functions.

- The LVD circuit compares the supply voltage (V_{DD}) with the detection voltage (V_{LVDH}, V_{LVDL}, V_{LVD}), and generates an internal reset or interrupt request signal.
- The detection level for the power supply detection voltage (V_{LVDH}, V_{LVDL}, V_{LVD}) can be selected by using the option byte as one of 3 levels (For details, see **3. 24 Option Byte**).
- Operable in STOP mode.
- After power is supplied, the reset state must be retained until the operating voltage becomes in the range defined in **5. 2. 3 AC characteristics**. This is done by utilizing the voltage detector or controlling the externally input reset signal. After the power supply is turned off, this LSI should be placed in the STOP mode, or placed in the reset state by utilizing the voltage detector or controlling the externally input reset signal before the voltage falls below the operating range. The range of operating voltage varies with the setting of the user option byte (000C2H or 010C2H).

(a) Interrupt & reset mode (option byte LVIMDS1, LVIMDS0 = 1, 0)

The two detection voltages (V_{LVDH}, V_{LVDL}) are selected by the option byte 000C1H. The high-voltage detection level (V_{LVDH}) is used for releasing resets and generating interrupts. The low-voltage detection level (V_{LVDL}) is used for generating resets.

(b) Reset mode (option byte LVIMDS1, LVIMDS0 = 1, 1)

The detection voltage (V_{LVD}) selected by the option byte 000C1H is used for generating/releasing resets.

(c) Interrupt mode (option byte LVIMDS1, LVIMDS0 = 0, 1)

The detection voltage (V_{LVD}) selected by the option byte 000C1H is used for releasing resets/generating interrupts.

3. 26. 2 On-chip debug security ID

See **26. 2 On-Chip Debug Security ID** in **RL78/G1A Hardware User's Manual (R01UH0305E)**.

3. 26. 3 Securing of user resources

See **26. 3 Securing of User Resources** in **RL78/G1A Hardware User's Manual (R01UH0305E)**.

4. 1. 3 Registers controlling the configurable amplifiers

The configurable amplifiers are controlled by the following 9 registers:

- Configuration register 1 (CONFIG1)
- Configuration register 2 (CONFIG2)
- MPX setting register 1 (MPX1)
- MPX setting register 2 (MPX2)
- Gain control register 1 (GC1)
- Gain control register 2 (GC2)
- Gain control register 3 (GC3)
- AMP operation mode control register (AOMC)
- Power control register 1 (PC1)

(2) Power control register 2 (PC2)

This register is used to enable or disable operation of the gain adjustment amplifier, the low-pass filter, the high-pass filter, the variable output voltage regulator, the reference voltage generator, and the temperature sensor. Use this register to stop unused functions to reduce power consumption and noise.

When using the high-pass filter, be sure to set bit 2 to 1.

Reset signal input clears this register to 00H.

- 80-pin products

Address: 12H After reset: 00H R/W

	7	6	5	4	3	2	1	0
PC2	0	0	0	GAINOF	LPFOF	HPFOF	LDOOF	TEMPOF

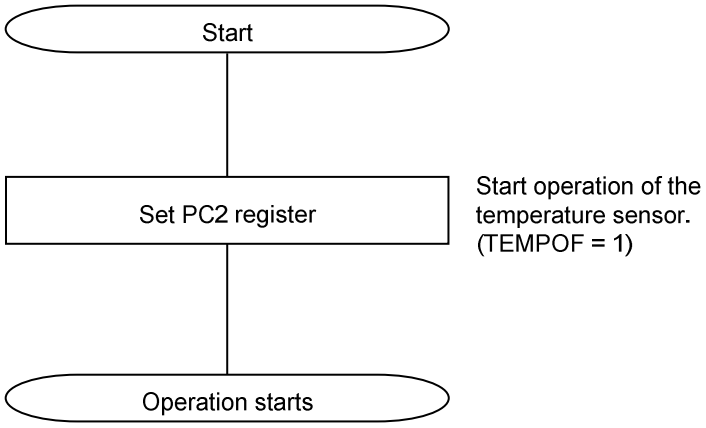
HPFOF	Operation of high-pass filter
0	Stop operation of the high-pass filter.
1	Enable operation of the high-pass filter.

Remark Bits 7 to 5 can be set to 1, but this has no effect on the function.

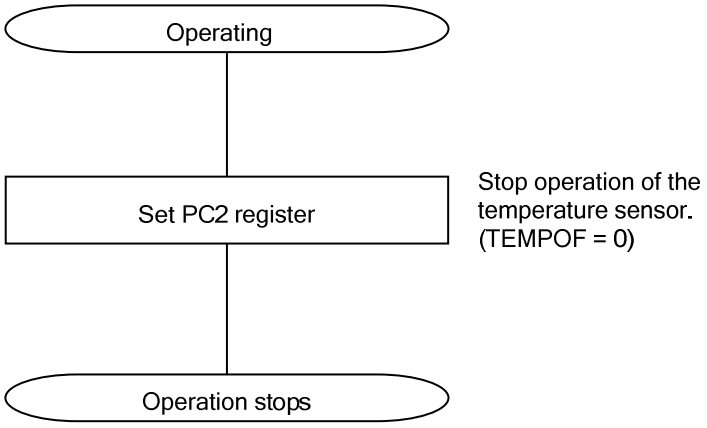
4. 6. 4 Procedure for operating the temperature sensor

Follow the procedures below to start and stop the temperature sensor.

Example of procedure for starting the temperature sensor

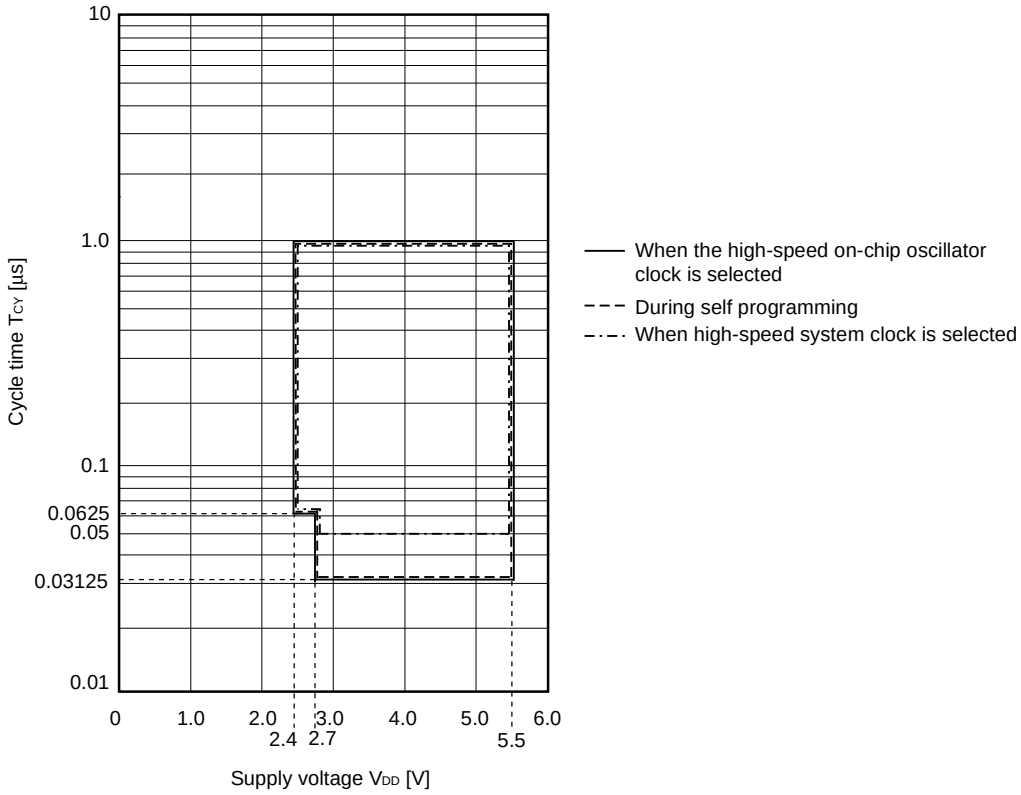


Example of procedure for stopping the temperature sensor



<R> **Minimum Instruction Execution Time during Main System Clock Operation**

T_{CY} vs V_{DD} (HS (high-speed main) mode)



<R> **(4) Communication between devices at same potential (CSI mode)**
(slave mode, SCKp ... External clock input) (1/2)

(T_A = –40 to +85°C, 1.6 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V) (1/2)

Parameter	Symbol	Conditions		HS Note 1		LS Note 2		LV Note 3		Unit
				MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
SCKp cycle time Note 4	t_{KCY2}	4.0V ≤ V_{DD} ≤ 5.5V	20MHz < f_{MCK}	8/f_{MCK}		–		–		ns
			f_{MCK} ≤ 20MHz	6/f_{MCK}		6/f_{MCK}		6/f_{MCK}		ns
		2.7V ≤ V_{DD} ≤ 5.5V	16MHz < f_{MCK}	8/f_{MCK}		–		–		ns
			f_{MCK} ≤ 16MHz	6/f_{MCK}		6/f_{MCK}		6/f_{MCK}		ns
		2.4 V ≤ V_{DD} ≤ 5.5 V		6/f_{MCK} and 500ns		6/f_{MCK} and 500ns		6/f_{MCK} and 500ns		ns
		1.8 V ≤ V_{DD} ≤ 5.5 V		6/f_{MCK} and 750ns		6/f_{MCK} and 750ns		6/f_{MCK} and 750ns		ns
		1.7 V ≤ V_{DD} ≤ 5.5 V		6/f_{MCK} and 1500ns		6/f_{MCK} and 1500ns		6/f_{MCK} and 1500ns		ns
		1.6 V ≤ V_{DD} ≤ 5.5 V		–		6/f_{MCK} and 1500ns		6/f_{MCK} and 1500ns		ns
SCKp high-level width low-level width	t_{KH2}, t_{KL2}	4.0 V ≤ V_{DD} ≤ 5.5 V		t_{KCY2}/2 -7		t_{KCY2}/2 -7		t_{KCY2}/2 -7		ns
		2.7 V ≤ V_{DD} ≤ 5.5 V		t_{KCY2}/2 -8		t_{KCY2}/2 -8		t_{KCY2}/2 -8		ns
		1.8 V ≤ V_{DD} ≤ 5.5 V		t_{KCY2}/2 -18		t_{KCY2}/2 -18		t_{KCY2}/2 -18		ns
		1.7 V ≤ V_{DD} ≤ 5.5 V		t_{KCY2}/2 -66		t_{KCY2}/2 -66		t_{KCY2}/2 -66		ns
		1.6 V ≤ V_{DD} ≤ 5.5 V		–		t_{KCY2}/2 -66		t_{KCY2}/2 -66		ns

Notes 1. HS is condition of HS (high-speed main) mode.

2. LS is condition of LS (low-speed main) mode.

3. LV is condition of LV (low-voltage main) mode.

4. Transfer rate in the SNOOZE mode: MAX. 1 Mbps

Caution Select the normal input buffer for the SIp pin and SCKp pin and the normal output mode for the SOp pin by using port input mode register g (PIMg) and port output mode register g (POMg).

Remarks 1. p: CSI number (p = 00, 10, 20, 21), m: Unit number (m = 0, 1), n: Channel number (n = 0 to 2), g: PIM and POM numbers (g = 0, 1)

2. f_{MCK}: Serial array unit operating clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn).
m: Unit number, n: Channel number (mn = 00 to 03, 10, 11))

<R> **(8) Communication between devices at different potential (1.8 V, 2.5 V or 3 V) (CSI mode) (master mode, SCKp ... internal clock output) (1/2)**

(T_A = –40 to +85°C, 1.8 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V) (1/2)

Parameter	Symbol	Conditions	HS Note 1		LS Note 2		LV Note 3		Unit
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
SCKp cycle time	t_{KCY1}	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ Vb ≤ 4.0 V, Cb = 30 pF, Rb = 1.4 kΩ, t_{KCY1} ≥ 4/f_{CLK}	300		1150		1150		ns
		2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ Vb ≤ 2.7 V, Cb = 30 pF, Rb = 2.7 kΩ, t_{KCY1} ≥ 4/f_{CLK}	500		1150		1150		
		1.8 V ≤ V_{DD} < 3.3 V, 1.6 V ≤ Vb ≤ 2.0 V, Note 4 Cb = 30 pF, Rb = 5.5 kΩ, t_{KCY1} ≥ 4/f_{CLK}	1150		1150		1150		
SCKp high level width	t_{KH1}	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ Vb ≤ 4.0 V, Cb = 30 pF, Rb = 1.4 kΩ	t_{KCY1}/2 -75		t_{KCY1}/2 -75		t_{KCY1}/2 -75		ns
		2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ Vb ≤ 2.7 V, Cb = 30 pF, Rb = 2.7 kΩ	t_{KCY1}/2 -170		t_{KCY1}/2 -170		t_{KCY1}/2 -170		
		1.8 V ≤ V_{DD} < 3.3 V, 1.6 V ≤ Vb ≤ 2.0 V, Note 4 Cb = 30 pF, Rb = 5.5 kΩ	t_{KCY1}/2 -458		t_{KCY1}/2 -458		t_{KCY1}/2 -458		
SCKp low level width	t_{KL1}	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ Vb ≤ 4.0 V, Cb = 30 pF, Rb = 1.4 kΩ	t_{KCY1}/2 -12		t_{KCY1}/2 -50		t_{KCY1}/2 -50		ns
		2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ Vb ≤ 2.7 V, Cb = 30 pF, Rb = 2.7 kΩ	t_{KCY1}/2 -18		t_{KCY1}/2 -50		t_{KCY1}/2 -50		
		1.8 V ≤ V_{DD} < 3.3 V, 1.6 V ≤ Vb ≤ 2.0 V, Note 4 Cb = 30 pF, Rb = 5.5 kΩ	t_{KCY1}/2 -50		t_{KCY1}/2 -50		t_{KCY1}/2 -50		

(**Notes**, **Caution** and **Remarks** are listed on the next page.)