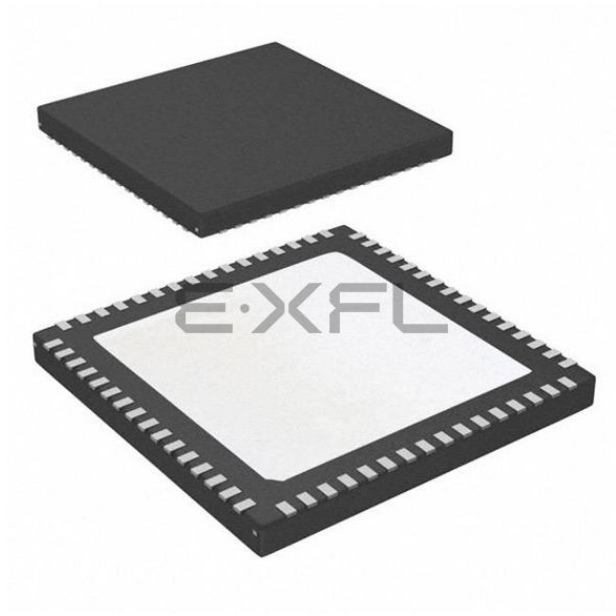
Renesas Electronics America Inc - R5F10FLEANA#U0 Datasheet



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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	RL78
Core Size	16-Bit
Speed	32MHz
Connectivity	CSI, I²C, LINbus, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	20
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	1.6V ~ 5.5V
Data Converters	A/D 13x8/12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-WFQFN Exposed Pad
Supplier Device Package	64-HWQFN (9x9)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f10fleana-u0

How to Read This Manual

It is assumed that the readers of this manual have general knowledge of electrical engineering, logic circuits, and microcontrollers.

- To gain a general understanding of functions:
  → Read this manual in the order of the **CONTENTS**. The mark "<R>" shows major revised points. The revised points can be easily searched by copying an "<R>" in the PDF file and specifying it in the "Find what:" field.

- How to interpret the register format:
  → For a bit number enclosed in angle brackets, the bit name is defined as a reserved word in the assembler, and is defined as an sfr variable using the #pragma sfr directive in the compiler.

- To know details of the microcontroller block:
  →Refer to the separate document **RL78/G1A Hardware User's Manual (R01UH0305E)**.

- To know details of the RL78 microcontroller instructions:
  → Refer to the separate document **RL78 family User's Manual Software (R01US0015E)**.

Conventions

Data significance:	Higher digits on the left and lower digits on the right	
Active low representations:	$\overline{\times\times\times}$ (overscore over pin and signal name)	
Note:	Footnote for item marked with **Note** in the text	
Caution:	Information requiring particular attention	
Remark:	Supplementary information	
Numerical representations:	Binary	···×××× or ××××B
	Decimal	···××××
	Hexadecimal	···××××H

CHAPTER 2 PIN FUNCTIONS

2. 1 Pin Functions in Microcontroller Block

The microcontroller block in the RL78/G1E is the RL78/G1A (64-pin products), but a part of pin functions of them are different from each other. The microcontroller function pins in the RL78/G1E (64-pin and 80-pin products) that differ from those in the RL78/G1A (64-pin products) are shown in the table below.

<R> **(1) Comparison of port functions (64-pin products)**

(1/2)

RL78/G1E (64-pin products)		RL78/G1A (64-pin products)	
Function Name	Alternate Function	Function Name	Alternate Function
P00	Same as RL78/G1A (64-pin products)	P00	TI00/(KR0)
P01	Same as RL78/G1A (64-pin products)	P01	TO00/(KR1)
P02	ANI17/TxD1/(KR2)	P02	ANI17/SO10/TxD1/(KR2)
P03	P03/ANI6/RxD1/(KR3)	P03	ANI16/SI10/SDA10/RxD1/(KR3)
		P04	SCK10/SCL10/(KR4)
		P05	TI05/TO05/KR8
		P06	TI06/TO06/KR9
P10	Same as RL78/G1A (64-pin products)	P10	ANI18/SCK00/SCL00/(KR0)
P11	Same as RL78/G1A (64-pin products)	P11	ANI20/SI00/RxD0/TOOLRxD/SDA00/(KR1)
P12	Same as RL78/G1A (64-pin products)	P12	ANI21/SO00/TxD0/TOOLTxD/(KR2)
P13	ANI22/TxD2/(KR3)	P13	ANI22/SO20/TxD2/(KR3)
P14	ANI23/RxD2/(KR4)	P14	ANI23/SI20/SDA20/RxD2/(KR4)
		P15	ANI24/SCK20/SCL20/(KR5)
		P16	TI01/TO01/INTP5
P20	Same as RL78/G1A (64-pin products)	P20	ANI0/AV_{REFP}
P21	Same as RL78/G1A (64-pin products)	P21	ANI1/AV_{REFM}
P22	Same as RL78/G1A (64-pin products)	P22	ANI2/(KR5)
P23	Same as RL78/G1A (64-pin products)	P23	ANI3/(KR6)
		P24	ANI4/(KR7)
		P25	ANI5/(KR8)
		P26	ANI6/(KR9)
		P27	ANI7
		P30	ANI27/SCK11/SCL11/INTP3/RTC1HZ
		P31	ANI29/TI03/TO03/INTP4
P40	Same as RL78/G1A (64-pin products)	P40	TOOL0
P41	Same as RL78/G1A (64-pin products)	P41	ANI30/TI07/TO07
P42	Same as RL78/G1A (64-pin products)	P42	TI04/TO04
		P43	–
		P50	ANI26/SI11/SDA11/INTP1
		P51	ANI25/SO11/INTP2
		P60	SCLA0
		P61	SDAA0
		P62	–
		P63	–

Remark Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR). About format, see Figure in **3. 4. 3. 8 Peripheral I/O redirection register (PIOR)**.

(2/2)

<R>

RL78/G1E (80-pin products)		RL78/G1A (64-pin products)	
Function Name	Alternate Function	Function Name	Alternate Function
P70	ANI28/SCK21/KR0/$\overline{\text{SCLK}}$ Note	P70	ANI28/SCK21/SCL21/KR0
P71	SI21/KR1/SDO Note	P71	SI21/SDA21/KR1
P72	SO21/KR2/SDI Note	P72	SO21/KR2
P73	KR3/$\overline{\text{CS}}$ Note	P73	SO01/KR3
		P74	SI01/SDA01/INTP8/KR4
		P75	SCK01/SCL01/INTP9/KR5
		P76	INTP10/KR6
		P77	INTP11/KR7
		P120	ANI19
P121	Same as RL78/G1A (64-pin products)	P121	X1
P122	Same as RL78/G1A (64-pin products)	P122	X2/EXCLK
		P123	XT1
		P124	XT2/EXCLKS
P130	Same as RL78/G1A (64-pin products)	P130	–
P137	Same as RL78/G1A (64-pin products)	P137	INTP0
P140	Same as RL78/G1A (64-pin products)	P140	PCLBUZ0/INTP6
		P141	PCLBUZ1/INTP7
		P150	ANI8
		P151	ANI9/(KR6)
		P152	ANI10/(KR7)
		P153	ANI11/(KR8)
		P154	ANI12/(KR9)

Note $\overline{\text{SCLK}}$, SDO, SDI, $\overline{\text{CS}}$ represent the pin functions of analog block. P70 to P73 which are connected to the pins of the chip of analog block inside the package have some alternate functions for analog block.

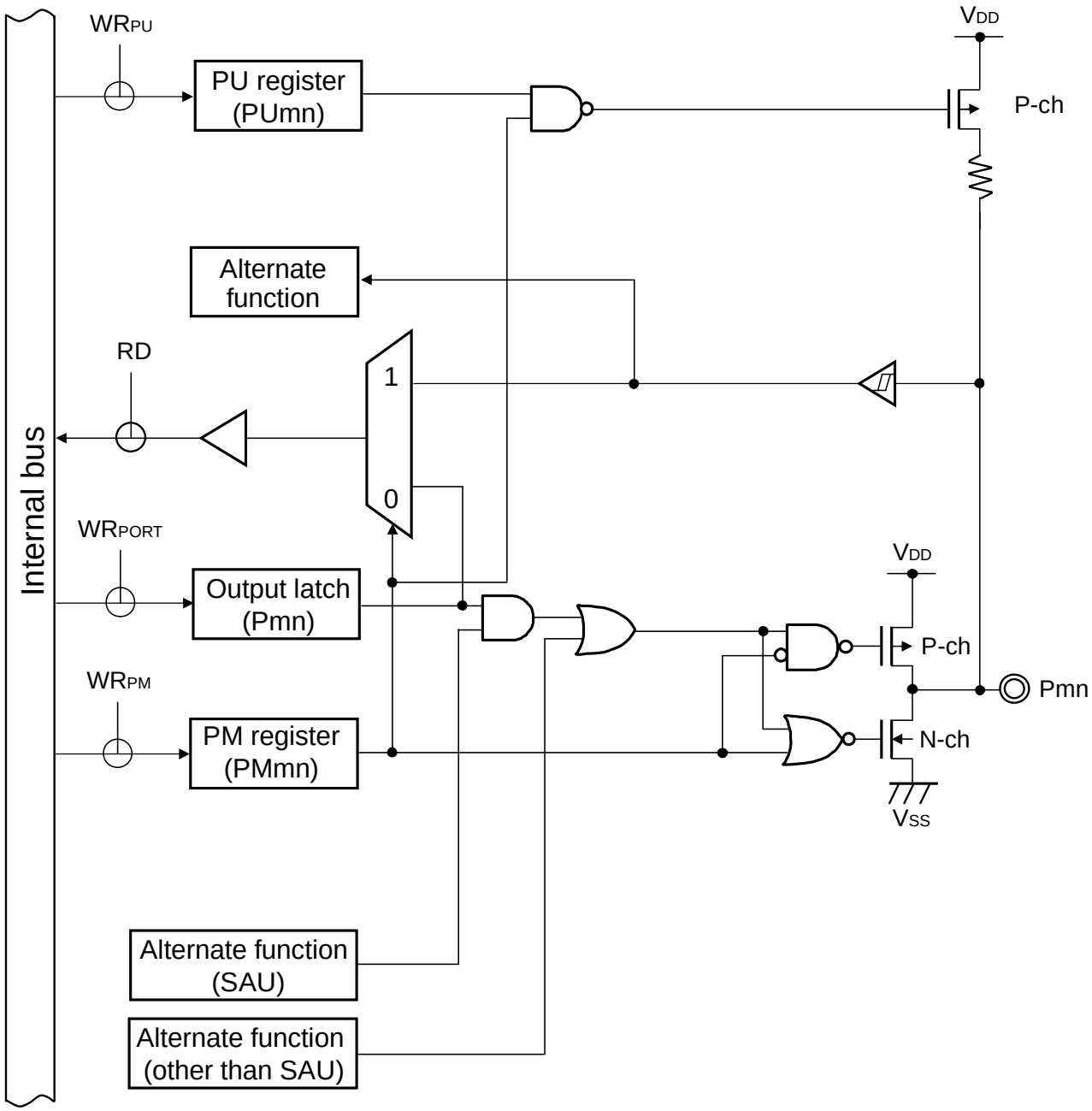
<R> **Remark** Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR). About format, see Figure in **3. 4. 3. 8 Peripheral I/O redirection register (PIOR)**.

(3) Comparison of functions other than port functions (60-pin products and 80-pin products)

About the comparison of functions other than port pins, See **2. 1. 2. 1 Functions available for each product**.

<R>

Figure 2-7. Pin Block Diagram for Pin Type 7-1-2



Remarks 1. For alternate functions, see **2. 1. 1 Port functions**.

2. SAU: Serial array unit

3. 3 CPU Architecture

In this section, the differences of the functions and registers from RL78/G1A (64-pin products) are described. For details, see **CHAPTER 3 CPU ARCHITECURE** in **RL78/G1A Hardware User's Manual (R01UH0305E)**.

3. 3. 1 Memory space

See **3. 1 Memory Space** in **RL78/G1A Hardware User's Manual (R01UH0305E)**.

3. 3. 2 Processor registers

3. 3. 2. 1 Control registers

See **3. 2. 1 Control registers** in **RL78/G1A Hardware User's Manual (R01UH0305E)**.

3. 3. 2. 2 General-purpose registers

See **3. 2. 2 General-purpose registers** in **RL78/G1A Hardware User's Manual (R01UH0305E)**.

3. 3. 2. 3 ES and CS registers

See **3. 2. 3 ES and CS registers** in **RL78/G1A Hardware User's Manual (R01UH0305E)**.

3. 4. 3. 3 Pull-up resistor option register (PUxx)

(1) 64-pin products

Symbol	7	6	5	4	3	2	1	0	Address	After Reset	R/W
PU0	0	0	0	0	PU03	PU02	PU01	PU00	F0030H	00H	R/W
PU1	0	0	0	PU14	PU13	PU12	PU11	PU10	F0031H	00H	R/W
PU4	0	0	0	0	0	PU42	PU41	PU40	F0034H	01H	R/W
PU7	0	0	0	0	PU73	PU72	PU71	PU70	F0037H	00H	R/W

Caution Be sure to clear bits 4 to 7 of the PU0 register, bits 5 to 7 of the PU1 register, bits 3 to 7 of the PU4 register, and bits 4 to 7 of the PU7 register to "0".

(2) 80-pin products

Symbol	7	6	5	4	3	2	1	0	Address	After Reset	R/W
PU0	0	0	0	PU04	PU03	PU02	PU01	PU00	F0030H	00H	R/W
PU1	0	0	PU15	PU14	PU13	PU12	PU11	PU10	F0031H	00H	R/W
PU4	0	0	0	0	0	PU42	PU41	PU40	F0034H	01H	R/W
<R> PU5	0	0	0	0	0	0	PU51	PU50	F0035H	00H	R/W
PU7	0	0	0	0	PU73	PU72	PU71	PU70	F0037H	00H	R/W
PU14	0	0	0	0	0	0	0	PU140	F003EH	00H	R/W

<R> **Caution Be sure to clear bits 5 to 7 of the PU0 register, bits 6 and 7of the PU1 register, bits 3 to 7 of the PU4 register, bits 2 to 7 of the PU5 register, bits 4 to 7 of the PU7 register, and bits 1 to 7 of the PU14 register to "0".**

3. 4. 3. 4 Port input mode register (PIMxx)

(1) 64-pin products

Symbol	7	6	5	4	3	2	1	0	Address	After Reset	R/W
PIM0	0	0	0	0	PIM03	0	PIM01	PIM00	F0040H	00H	R/W
PIM1	0	0	0	PIM14	0	0	PIM11	PIM10	F0041H	00H	R/W

<R> **Caution Be sure to clear bits 2 and 4 to 7 of the PIM0 register, and bits 2, 3 and 5 to 7 of the PIM1 register to "0".**

(2) 80-pin products

Symbol	7	6	5	4	3	2	1	0	Address	After Reset	R/W
<R> PIM0	0	0	0	PIM04	PIM03	0	PIM01	PIM00	F0040H	00H	R/W
PIM1	0	0	PIM15	PIM14	0	0	PIM11	PIM10	F0041H	00H	R/W

<R> **Caution Be sure to clear bits 2 and 5 to 7 of the PIM0 register, and bits 2, 3, 6 and 7 of the PIM1 register to "0".**

<R> **(2) Low-speed on-chip oscillator clock (Low-speed on-chip oscillator)**

This circuit oscillates a clock of f_{IL} = 15 kHz (TYP.).

The low-speed on-chip oscillator clock cannot be used as the CPU clock.

Only the following peripheral hardware runs on the low-speed on-chip oscillator clock.

- Watchdog timer
- 12-bit Interval timer

<R> This clock operates when bit 4 (WDTON) of the option byte (000C0H), bit 4 (WUTMMCK0) of the subsystem clock supply mode control register (OSMC), or both are set to 1.

However, when WDTON = 1, WUTMMCK0 = 0, and bit 0 (WDSTBYON) of the option byte (000C0H) is 0, oscillation of the low-speed on-chip oscillator stops if the HALT or STOP instruction is executed.

Remark f_X: X1 clock oscillation frequency

f_{IH}: High-speed on-chip oscillator clock frequency

f_{EX}: External main system clock frequency

f_{IL}: Low-speed on-chip oscillator clock frequency

3. 5. 7 Resonator and oscillator constants

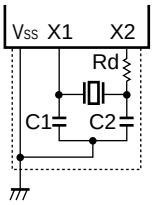
The resonators for which the operation is verified and their oscillator constants are shown below.

Cautions 1. The oscillator constants shown above are reference values based on evaluation in a specific environment by the resonator manufacturer. Be sure to apply to the resonator manufacturer for evaluation on the actual circuit before using these constants for your application.
Also apply to the resonator manufacturer for re-evaluation on the actual circuit if you have changed the make of the microcontroller or the board.

2. The oscillation voltage and oscillation frequency only indicate the oscillator characteristic. Use the RL78/G1E so that the internal operation conditions are within the specifications of the DC and AC characteristics.

<R> **Figure 3-2. External Oscillation Circuit Example**

(a) X1 oscillation



(1) X1 oscillation: **As of March, 2013 (1/4)**

Manufacturer	Resonator	Part Number	SMD/ Lead	Frequency (MHz)	Flash operation mode Note 1	Recommended Circuit Constants Note 2 (reference)			Oscillation Voltage Range (V)	
						C1 (pF)	C2 (pF)	Rd (kΩ)	MIN.	MAX.
KYOCERA rystal Device Corporation Note 3	Crystal resonator	CX8045GB04000D0HEQZ1	SMD	4.0	LV	12	12	0	1.6	5.5
		CX8045GB04000D0HEQZ1	SMD	4.0	LS	12	12	0	1.8	5.5
		CX8045GB04000D0HEQZ1	SMD	4.0	HS	12	12	0	2.4	5.5
		CX8045GB08000D0HEQZ1	SMD	8.0	LS	12	12	0	1.8	5.5
		CX8045GB08000D0HEQZ1	SMD	8.0	HS	12	12	0	2.4	5.5
		CX8045GB12000D0HEQZ1	SMD	12.0	HS	10	10	0	2.4	5.5
		CX3225GB16000D0HEQZ1	SMD	16.0	HS	10	10	0	2.4	5.5
		CX3225GB20000D0HEQZ1	SMD	20.0	HS	8	8	0	2.7	5.5

<R> **Notes 1.** Set the flash operation mode by using CMODE1 and CMODE0 bits of the option byte (000C2H).

2. C1, C2 columns indicate a reference value.

3. When using these oscillators, contact KYOCERA Crystal Device Corporation (http://www.kyocera-crystal.jp/).

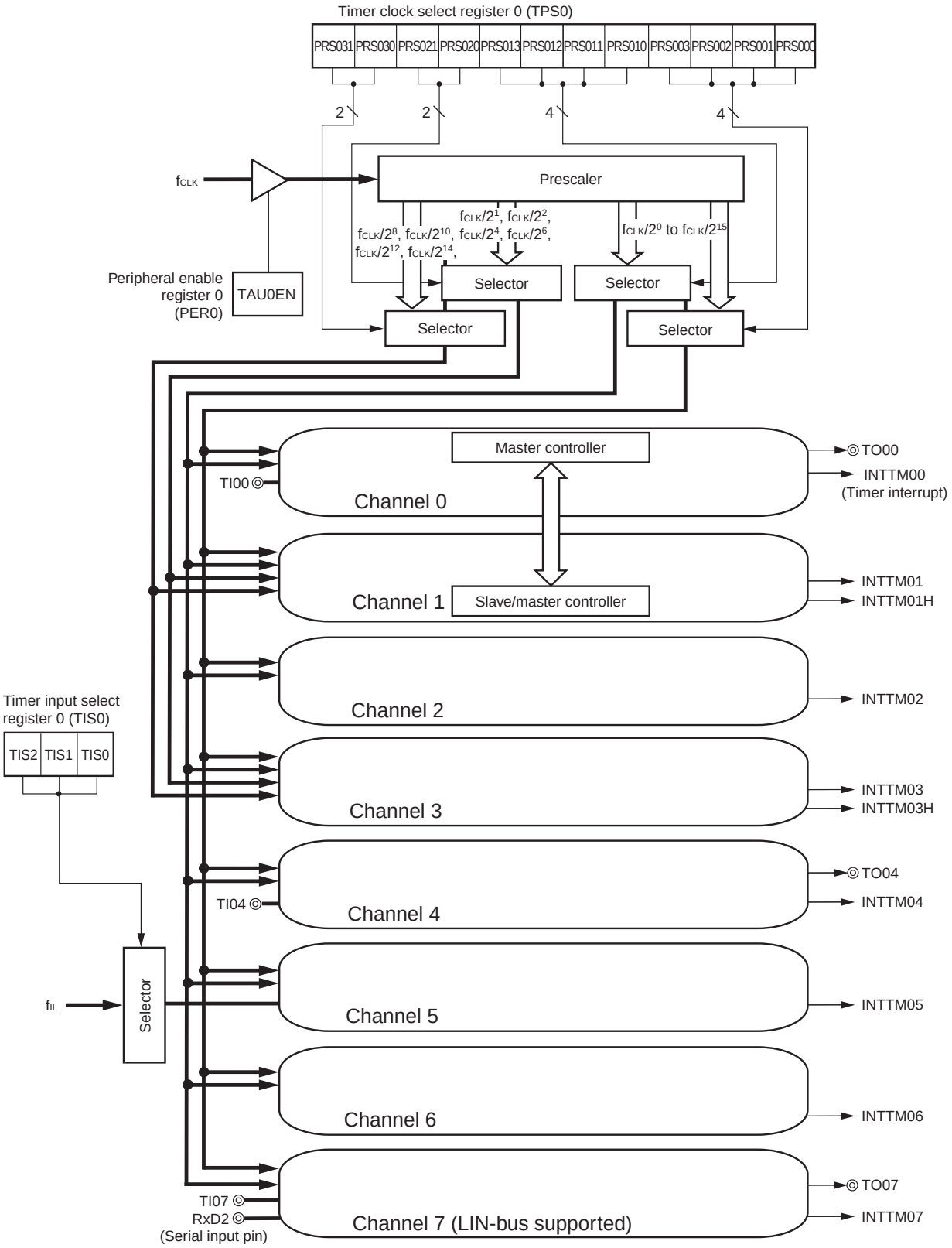
Remark Relationship between operation voltage width, operation frequency of CPU and operation mode is as below.

HS (High speed main) mode: $2.7\ V \le V_{DD} \le 5.5\ V$@1 MHz to 32 MHz (When X1 oscillation: 1 MHz to 20 MHz)
$2.4\ V \le V_{DD} \le 5.5\ V$@1 MHz to 16 MHz

LS (Low speed main) mode: $1.8\ V \le V_{DD} \le 5.5\ V$@1 MHz to 8 MHz

LV (Low voltage main) mode: $1.6\ V \le V_{DD} \le 5.5\ V$@1 MHz to 4 MHz

Figure 3-3. Entire Configuration of Timer Array Unit 0 (Example: 80-pin products)



Remark f_{IL}: ow-speed on-chip oscillator clock frequency

3. 6. 3 Registers controlling timer array unit

The bit settings which are different from that of RL78/G1A (64-pin products) are shown below. For details of each register, see **6. 3 Registers Controlling Timer Array Unit** in **RL78/G1A Hardware User's Manual (R01UH0305E)**.

<R> 3. 6. 3. 1 Peripheral enable register 0 (PER0)

Address: F00F0H After reset: 00H R/W

Symbol	<7>	6	<5>	4	<3>	<2>	1	<0>
PER0	RTCEN	0	ADCEN	0	SAU1EN	SAU0EN	0	TAU0EN

TAU0EN	Control of timer array 0 unit input clock
0	Stops input clock supply. • SFR used by timer array unit 0 cannot be written. • Timer array unit 0 is in the reset status.
1	Enables input clock supply. • SFR used by timer array unit 0 can be read/written.

Cautions 1. When setting the timer array unit, be sure to set the TAUmEN bit to 1 first. If TAUmEN = 0, writing to a control register of timer array unit is ignored, and all read values are default values (except for the timer input select register 0 (TIS0), input switch control register (ISC), noise filter enable register 1 (NFEN1), port mode control registers 0, 1, 4 (PMC0, PMC1, PMC4), port mode registers 0, 1, 4 (PM0, PM1, PM4), and port registers 0, 1, 4 (P0, P1, P4)).

- **Timer clock select register m (TPSm)**
- **Timer mode register mn (TMRmn)**
- **Timer status register mn (TSRmn)**
- **Timer channel enable status register m (TEm)**
- **Timer channel start register m (TSm)**
- **Timer channel stop register m (TTm)**
- **Timer output enable register m (TOEm)**
- **Timer output register m (TOm)**
- **Timer output level register m (TOLm)**
- **Timer output mode register m (TOMm)**

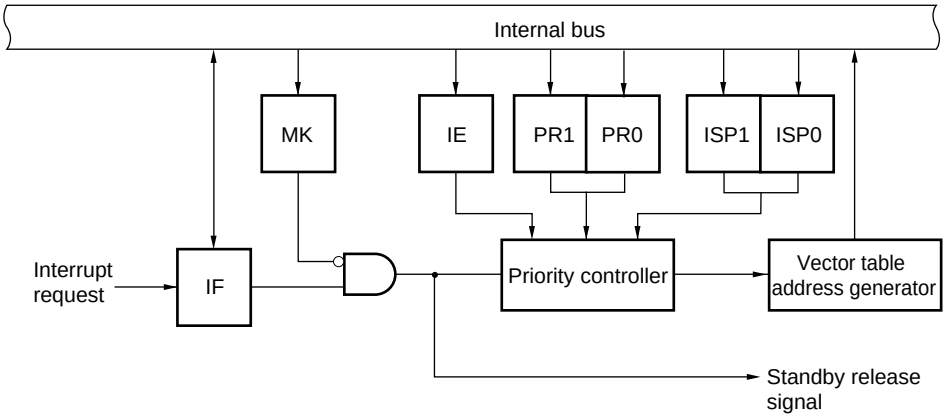
2. Be sure to clear bits 1, 4, and 6 to "0".

3. 6. 3. 2 Timer clock select register m (TPSm)

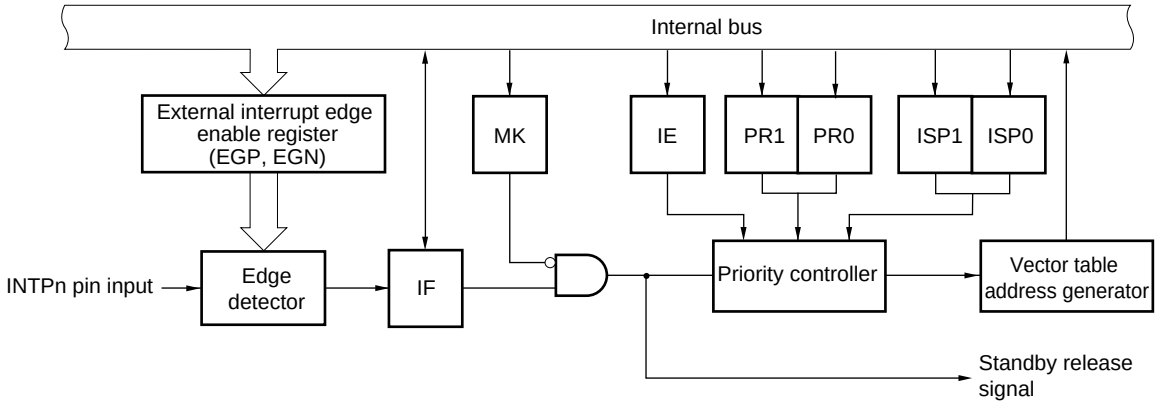
The bit setting is same as that of RL78/G1A (64-pin products). For details, see **6. 3. 2 Timer clock select register m (TPSm)** in **RL78/G1A Hardware User's Manual (R01UH0305E)**.

Figure 3-13. Basic Configuration of Interrupt Function (1/2)

(a) Internal maskable interrupt



(b) External maskable interrupt (INTPn)



IF: Interrupt request flag
IE: Interrupt enable flag
ISP0: In-service priority flag 0
ISP1: In-service priority flag 1
MK: Interrupt mask flag
PR0: Priority specification flag 0
PR1: Priority specification flag 1

Remark 64-pin products: n = 0
80-pin products: n = 0 to 3, 6

3. 20 Power-On-Reset Circuit

See **CHAPTER 20 POWER-ON-RESET CIRCUIT** in **RL78/G1A Hardware User's Manual (R01UH0305E)**.

Format of user option byte (000C2H/010C2H)

Address: 000C2H/010C2H [Note]

7	6	5	4	3	2	1	0
CMODE1	CMODE0	1	0	FRQSEL3	FRQSEL2	FRQSEL1	FRQSEL0

CMODE1	CMODE0	Setting of flash operation mode		
			Operating Frequency Range	Operating Voltage Range
0	0	LV (low voltage main) mode	1 to 4 MHz	1.6 to 5.5 V
1	0	LS (low speed main) mode	1 to 8 MHz	1.8 to 5.5 V
1	1	HS (high speed main) mode	1 to 16 MHz	2.4 to 5.5 V
			1 to 32 MHz	2.7 to 5.5 V
Other than above		Setting prohibited		

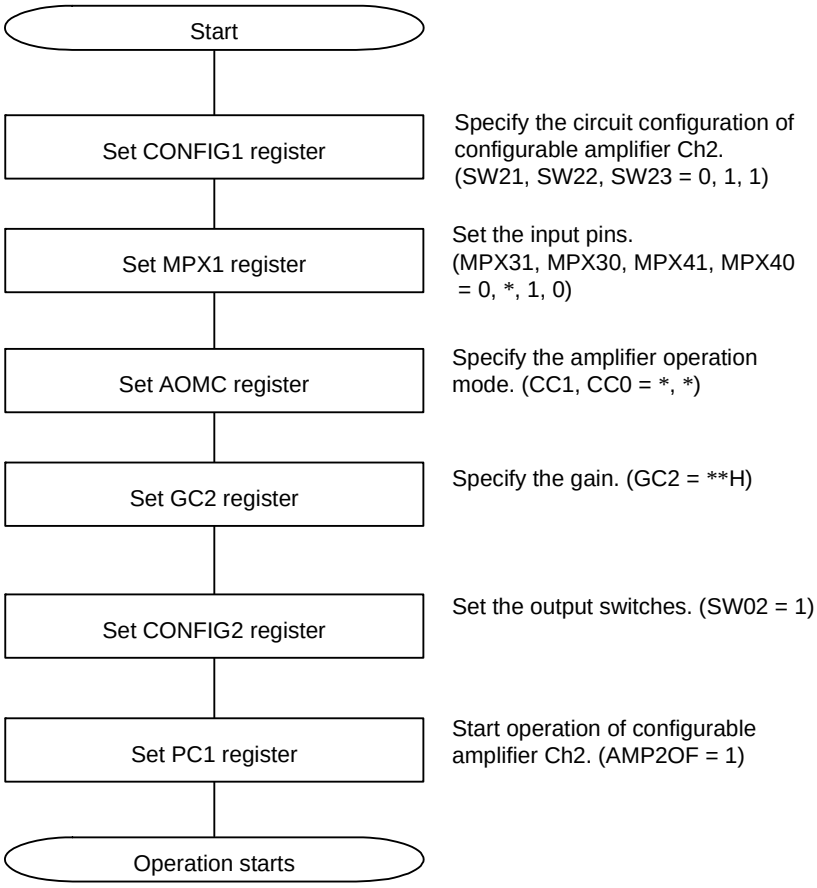
FRQSEL3	FRQSEL2	FRQSEL1	FRQSEL0	Frequency of the high-speed on-chip oscillator
1	0	0	0	32 MHz
0	0	0	0	24 MHz
1	0	0	1	16 MHz
0	0	0	1	12 MHz
1	0	1	0	8 MHz
0	0	1	0	6 MHz
1	0	1	1	4 MHz
0	0	1	1	3 MHz
1	1	0	0	2 MHz
1	1	0	1	1 MHz
Other than above				Setting prohibited

Note Set the same value as 000C2H to 010C2H when the boot swap operation is used because 000C2H is replaced by 010C2H.

<R> **Cautions 1. Be sure to set bits 5, 4 to “10B”.**

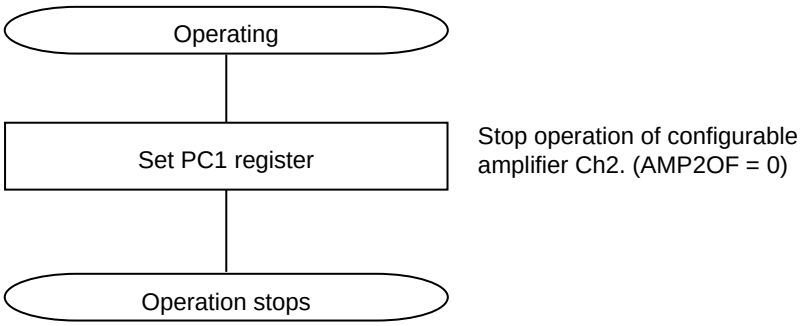
2. The ranges of operation frequency and operation voltage vary depending on the flash operation mode. For details, see 5. 2. 3 AC characteristics.

Example of procedure for starting configurable amplifier Ch2 (inverting amplifier)



Remark *: don't care

Example of procedure for stopping configurable amplifier Ch2 (inverting amplifier)



4. 2. 3 Registers controlling the gain adjustment amplifier

The gain adjustment amplifier is controlled by the following 3 registers:

- MPX setting register 3 (MPX3)
- Gain control register 4 (GC4)
- Power control register 2 (PC2)

(1) MPX setting register 3 (MPX3)

This register is used to control MPX7, MPX9, MPX10, and MPX11.

When selecting the signal to be input to the gain adjustment amplifier, use bits 2 to 0.

Reset signal input clears this register to 00H.

- **64-pin products**

Address: 05H After reset: 00H R/W

	7	6	5	4	3	2	1	0
MPX3	0	0	SCF2	SCF1	0	MPX72	MPX71	MPX70

MPX72	MPX71	MPX70	Source of gain adjustment amplifier input
0	0	0	–
0	0	1	Configurable amplifier Ch1 output signal
0	1	0	Configurable amplifier Ch2 output signal
0	1	1	Configurable amplifier Ch3 output signal
1	0	0	D/A converter Ch4 output signal or VREFIN4 pin
Other than above			Setting prohibited

Caution Be sure to clear bit 3 to "0".

<R> **Remark** Bits 7 and 6 are fixed at 0 of read only.

- **80-pin products**

Address: 05H After reset: 00H R/W

	7	6	5	4	3	2	1	0
MPX3	0	0	SCF2	SCF1	SCF0	MPX72	MPX71	MPX70

MPX72	MPX71	MPX70	Source of gain adjustment amplifier input
0	0	0	GAINAMP_IN pin
0	0	1	Configurable amplifier Ch1 output signal
0	1	0	Configurable amplifier Ch2 output signal
0	1	1	Configurable amplifier Ch3 output signal
1	0	0	D/A converter Ch4 output signal or VREFIN4 pin
Other than above			Setting prohibited

<R> **Remark** Bits 7 and 6 are fixed at 0 of read only.

4. 7 Variable Output Voltage Regulator

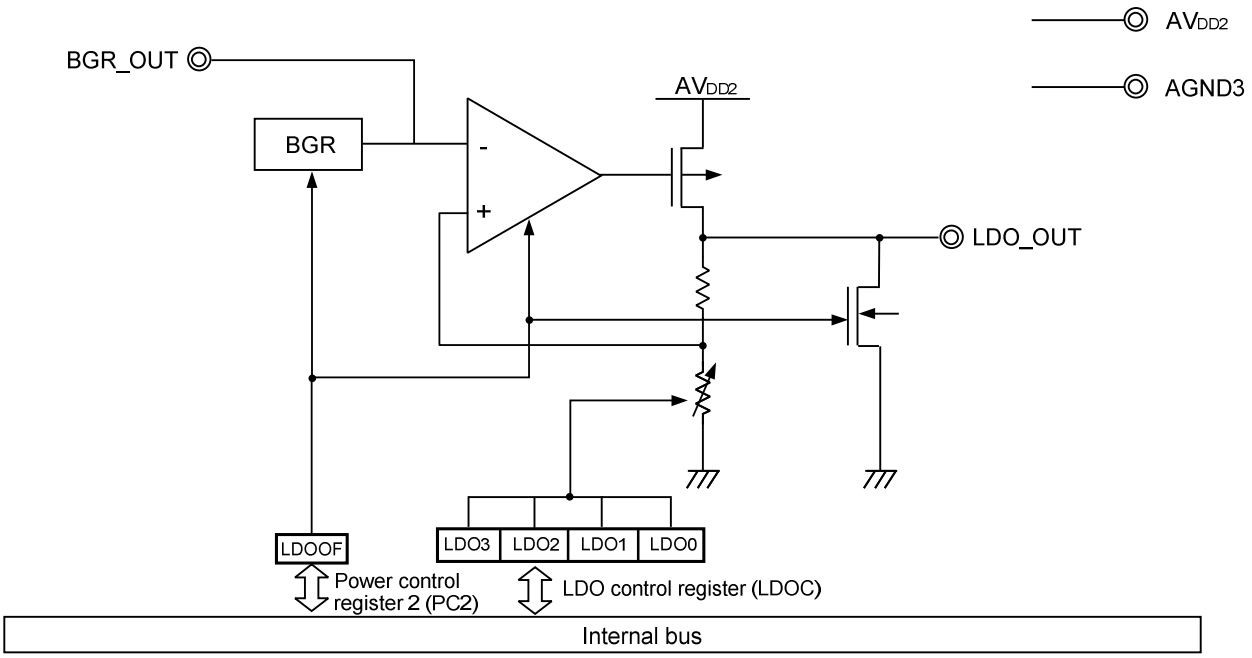
The RL78/G1E (64-pin products, 80-pin products) has one on-chip variable output voltage regulator channel. This is a series regulator that generates a voltage of 3.3 V (default) from a supplied voltage of 5 V.

4. 7. 1 Overview of variable output voltage regulator features

The features of variable output voltage regulator are described below.

- Output voltage range: 2.0 to 3.3 V (Typ.)
- Output current: 15 mA (Max.)
- Includes a power-off function.

4. 7. 2 Block diagram



<R> **(6) Communication between devices at different potential (1.8 V, 2.5 V or 3 V) (UART mode) (output from dedicated baud rate generator) (1/2)**

(T_A = –40 to +85°C, 1.8 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V) (1/2)

Parameter	Symbol	Conditions		HS Note 1		LS Note 2		LV Note 3		Unit
				MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Transfer rate Note 4		Reception	4.0V ≤ V_{DD} ≤ 5.5V, 2.7V ≤ Vb ≤ 4.0V		f_{MCK}/6		f_{MCK}/6		f_{MCK}/6	bps
			Theoretical value of the maximum transfer rate: f_{MCK} = f_{CLK} Note 7		5.3		1.3		0.6	Mbps
			2.7V ≤ V_{DD} < 4.0V, 2.3V ≤ Vb ≤ 2.7V		f_{MCK}/6		f_{MCK}/6		f_{MCK}/6	bps
			Theoretical value of the maximum transfer rate: f_{MCK} = f_{CLK} Note 7		5.3		1.3		0.6	Mbps
			1.8V ≤ V_{DD} < 3.3V, 1.6V ≤ Vb ≤ 2.0V Note 5		f_{MCK}/6		f_{MCK}/6		f_{MCK}/6	bps
			Theoretical value of the maximum transfer rate: f_{MCK} = f_{CLK} Note 7		5.3 Note 6		1.3		0.6	Mbps

Notes 1. HS is condition of HS (high-speed main) mode.

2. LS is condition of LS (low-speed main) mode.

3. LV is condition of LV (low-voltage main) mode.

4. Transfer rate in the SNOOZE mode is 4,800 bps.

5. Specify a value so as to satisfy V_{DD} ≥ Vb.

6. The following conditions are also required for low voltage interface.
2.4 V ≤ V_{DD} < 2.7 V: MAX. 2.6 Mbps
1.8 V ≤ V_{DD} < 2.4 V: MAX. 1.3 Mbps

7. f_{CLK} in each operating mode is as below.
HS (high-speed main) mode: f_{CLK} = 32 MHz
LS (low-speed main) mode: f_{CLK} = 8 MHz
LV (low-voltage main) mode: f_{CLK} = 4 MHz

(**Caution** and **Remarks** are listed on the next page.)

(-40°C ≤ T_A ≤ 85°C, AV_{DD1} = AV_{DD2} = AV_{DD3} = DV_{DD} = 5.0 V, VREFIN1 = VREFIN2 = VREFIN3 = 1.7 V, AMP1OF = AMP2OF = AMP3OF = 1, DAC1OF = DAC2OF = DAC3OF = 0, GC1 = GC2 = 03H, instrumentation amplifier) (2/2)

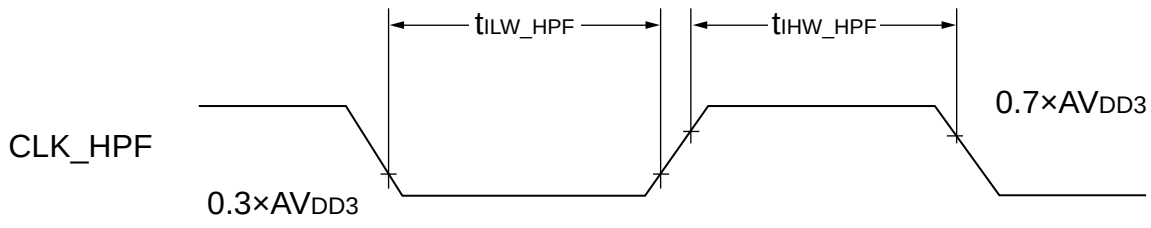
Parameter	Symbol	Conditions	Ratings			Unit
			MIN	TYP	MAX	
Input conversion offset voltage	VOFF00	CC1, CC0 = 0, 0, T_A = 25°C, GC3 = 00H (20 dB)	-7	–	7	mV
	VOFF01	CC1, CC0 = 0, 1, T_A = 25°C, GC3 = 00H (20 dB)	-10	–	10	mV
	VOFF10	CC1, CC0 = 1, 0, T_A = 25°C, GC3 = 00H (20 dB)	-10	–	10	mV
	VOFF11	CC1, CC0 = 1, 1, T_A = 25°C, GC3 = 00H (20 dB)	-12	–	12	mV
Input conversion offset voltage temperature coefficient	VOTC		–	±6.0	–	μV/°C
Slew rate	SR00	CC1, CC0 = 0, 0, CL = 30 pF, GC3 = 00H (20 dB)	–	0.68	–	V/μs
	SR01	CC1, CC0 = 0, 1, CL = 30 pF, GC3 = 00H (20 dB)	–	0.35	–	V/μs
	SR10	CC1, CC0 = 1, 0, CL = 30 pF, GC3 = 00H (20 dB)	–	0.25	–	V/μs
	SR11	CC1, CC0 = 1, 1, CL = 30 pF, GC3 = 00H (20 dB)	–	0.09	–	V/μs
Common mode rejection ratio	CMRR00	CC1, CC0 = 0, 0 GC3 = 11H (54 dB) f = 1 kHz	–	86	–	dB
	CMRR01	CC1, CC0 = 0, 1 GC3 = 11H (54 dB) f = 1 kHz	–	84	–	dB
	CMRR10	CC1, CC0 = 1, 0 GC3 = 11H (54 dB) f = 1 kHz	–	82	–	dB
<R>	CMRR11	CC1, CC0 = 1, 1 GC3 = 11H (54 dB) f = 1 kHz	–	76	–	dB
Power supply rejection ratio	PSRR00	CC1, CC0 = 0, 0 GC3 = 00H (20 dB) f = 1 kHz	–	70	–	dB
	PSRR01	CC1, CC0 = 0, 1 GC3 = 00H (20 dB) f = 1 kHz	–	68	–	dB
	PSRR10	CC1, CC0 = 1, 0 GC3 = 00H (20 dB) f = 1 kHz	–	62	–	dB
<R>	PSRR11	CC1, CC0 = 1, 1 GC3 = 00H (20 dB) f = 1 kHz	–	50	–	dB
Gain setting error	GAIN_Accu1	T_A = 25°C	-0.6	–	0.6	dB
	GAIN_Accu2	T_A = –40 to 85°C	-1.0	–	1.0	dB

5. 3. 3. 5 High-pass filter characteristics

($-40°C \le T_A \le 85°C$, $AV_{DD1} = AV_{DD2} = AV_{DD3} = AV_{DD4} = DV_{DD} = 5.0$ V, HPFOF = 1)

Parameter	Symbol	Conditions	Ratings			Unit
			MIN.	TYP.	MAX.	
Current consumption	IccA		–	800	1800	μA
Input voltage	V_{ILHPF}		AGND4 +0.2	–	–	V
	V_{IHHPF}		–	–	AV_{DD3} - 1.5	V
<R> Output voltage	V_{OLHPF}	IOL = –200 μA	–	AGND4 +0.22	AGND4 +0.25	V
	V_{OHHPF}	IOH = 200 μA	AV_{DD3} -1.55	AV_{DD3} -1.52	–	V
Cutoff frequency	fc1	f_{CLK_HPF} = 2 kHz	–	8	–	Hz
	fc2	f_{CLK_HPF} = 200 kHz	–	800	–	Hz
CLK_HPF low-level input voltage	V_{ILCLK_HPF}				$0.3 \times AV_{DD3}$	V
CLK_HPF high-level input voltage	V_{IHCLK_HPF}		$0.7 \times AV_{DD3}$			V
CLK_HPF Input frequency	f_{CLK_HPF}		2	–	200	kHz
CLK_HPF Input low-level-width Input high-level-width	t_{ILW_HPF} t_{IHW_HPF}		200	–	–	ns

Clock Timing



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