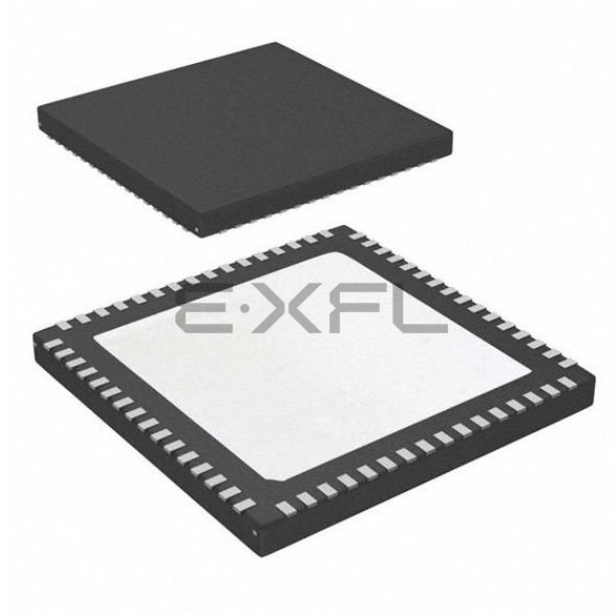
Renesas Electronics America Inc - R5F10FLEANA#YB1 Datasheet



Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	RL78
Core Size	16-Bit
Speed	32MHz
Connectivity	CSI, I²C, LINbus, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	20
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	1.6V ~ 5.5V
Data Converters	A/D 13x8/12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-WFQFN Exposed Pad
Supplier Device Package	64-WQFN (9x9)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f10fleana-yb1

2. 1. 2 Functions other than port functions

2. 1. 2. 1 Functions available for each product

(1/3)

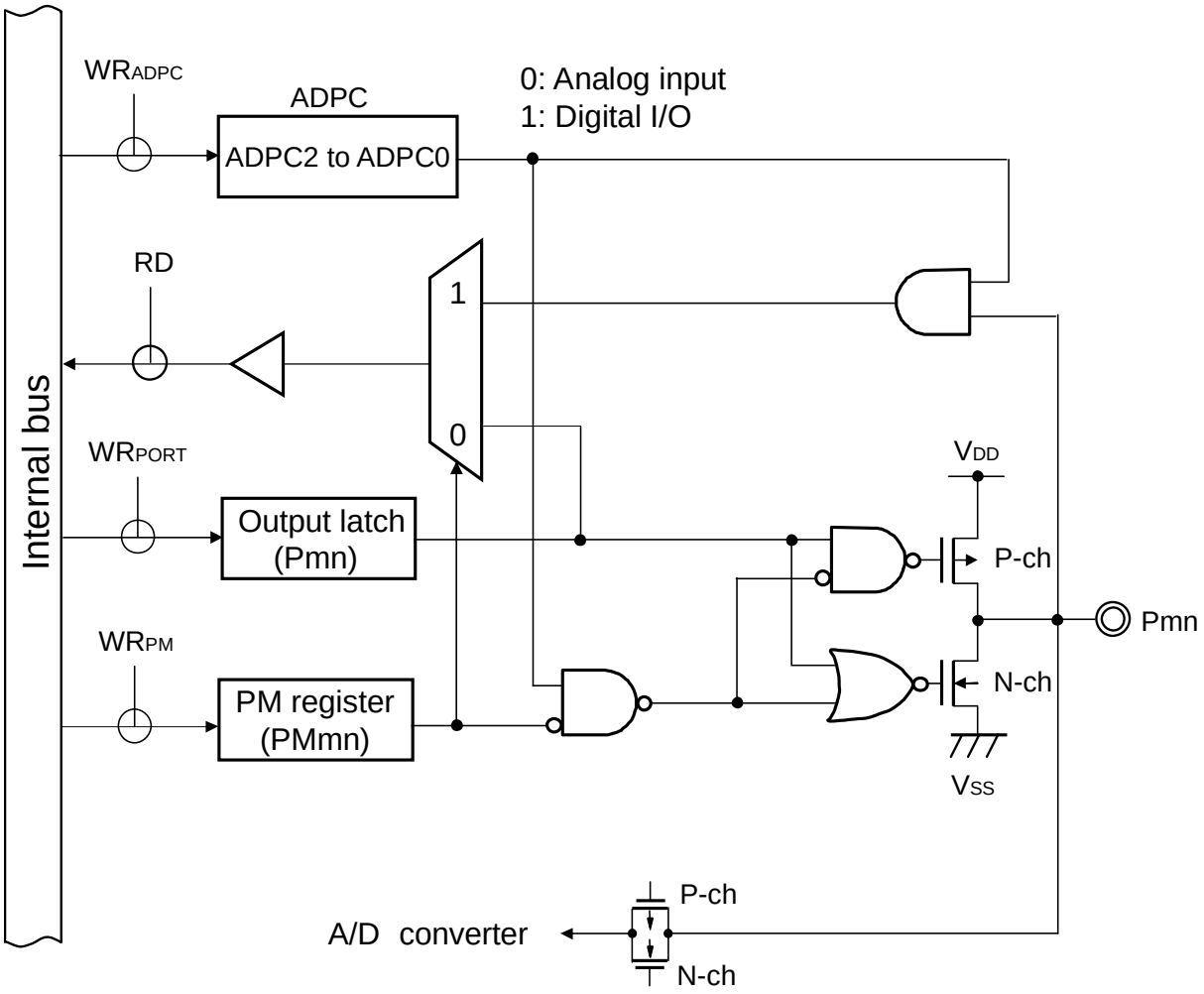
Function Name	RL78/G1E (64-pin)	RL78/G1E (80-pin)	RL78/G1A (64-pin)
ANI0	√	√	√
ANI1	√	√	√
ANI2	√	√	√
ANI3	√	√	√
ANI4	–	√	√
ANI5	–	–	√
ANI6	–	–	√
ANI7	–	–	√
ANI8	–	–	√
ANI9	–	–	√
ANI10	–	–	√
ANI11	–	–	√
ANI12	–	–	√
ANI16	√	√	√
ANI17	√	√	√
ANI18	√	√	√
ANI19	–	–	√
ANI20	√	√	√
ANI21	√	√	√
ANI22	√	√	√
ANI23	√	√	√
ANI24	–	√	√
ANI25	–	√	√
ANI26	–	√	√
ANI27	–	–	√
ANI28	√	√	√
ANI29	–	–	√
ANI30	√	√	√
INTP0	√	√	√
INTP1	–	√	√
INTP2	–	√	√
INTP3	–	–	√
INTP4	–	–	√
INTP5	–	–	√
INTP6	–	√	√
INTP7	–	–	√
INTP8	–	–	√
INTP9	–	–	√
INTP10	–	–	√
INTP11	–	–	√

<R> 2. 2. 2 80-pin products

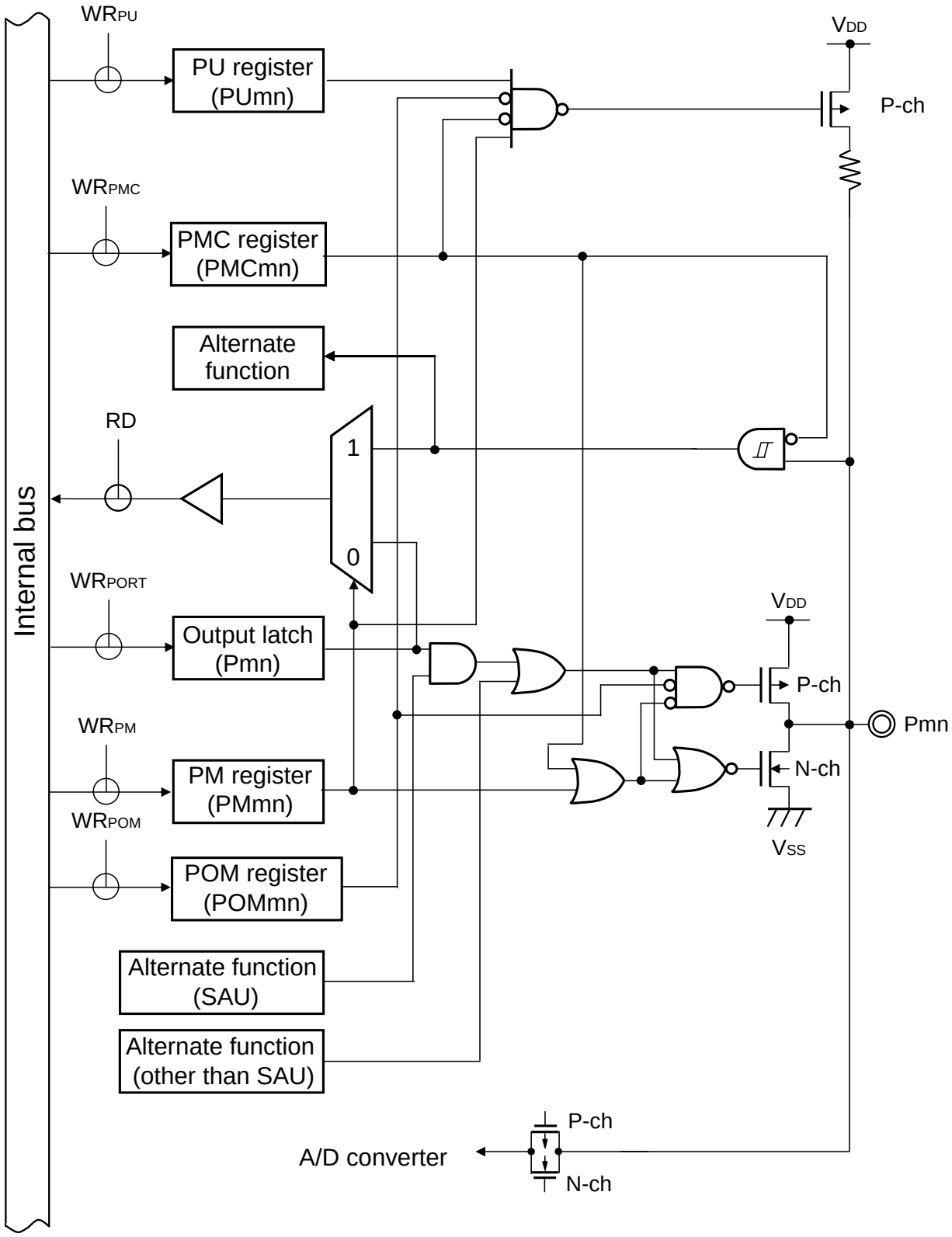
Function Name	I/O Circuit Type	I/O	Function
AV_{DD3}	–	–	Power supply pin for filter
SC_IN	ANALOG6	Input	Input pin for filter signal processing
CLK_SYNCH	ANALOG7	Input	Pin for inputting synchronous detector control clock
SYNCH_OUT	ANALOG11	Output	Synchronous detector output pin
AGND2	–	–	GND pin for gain adjustment amplifier
GAINAMP_OUT	ANALOG10	Output	Output pin for gain adjustment amplifier
GAINAMP_IN	ANALOG6	Input	Input pin for gain adjustment amplifier
MPXIN61	ANALOG6	Input	Multiplexer 6 input pin 1 (Configurable amplifier Ch3 input pin 1 (+))
MPXIN51	ANALOG6		Multiplexer 5 input pin 1 (Configurable amplifier Ch3 input pin 1 (-))
MPXIN60	ANALOG6		Multiplexer 6 input pin 0 (Configurable amplifier Ch3 input pin 0 (+))
MPXIN50	ANALOG6		Multiplexer 5 input pin 0 (Configurable amplifier Ch3 input pin 0 (-))
AMP3_OUT	ANALOG10	Output	Configurable amplifier Ch3 output pin
DAC3_OUT/ VREFIN3	ANALOG2	I/O	D/A converter Ch3 output pin/configurable amplifier Ch3 reference voltage input pin
AMP2_OUT	ANALOG11	Output	Configurable amplifier Ch2 output pin
AGND1	–	–	GND pin for configurable amplifiers Ch1 to Ch3
AMP1_OUT	ANALOG11	Output	Configurable amplifier Ch1 output pin
AV_{DD1}	–	–	Power supply pin for configurable amplifiers Ch1 to Ch3
DAC2_OUT/ VREFIN2	ANALOG2	I/O	D/A converter Ch2 output pin/configurable amplifier Ch2 reference voltage input pin
DAC1_OUT/ VREFIN1	ANALOG2		D/A converter Ch1 output pin/configurable amplifier Ch1 reference voltage input pin
MPXIN41	ANALOG6	Input	Multiplexer 4 input pin 1 (Configurable amplifier Ch2 input pin 1 (+))
MPXIN31	ANALOG6		Multiplexer 3 input pin 1 (Configurable amplifier Ch2 input pin 1 (-))
MPXIN40	ANALOG6		Multiplexer 4 input pin 0 (Configurable amplifier Ch2 input pin 0 (+))
MPXIN30	ANALOG6		Multiplexer 3 input pin 0 (Configurable amplifier Ch2 input pin 0 (-))
MPXIN21	ANALOG6		Multiplexer 2 input pin 1 (Configurable amplifier Ch1 input pin 1 (+))
MPXIN11	ANALOG6		Multiplexer 1 input pin 1 (Configurable amplifier Ch1 input pin 1 (-))
MPXIN20	ANALOG6		Multiplexer 2 input pin 0 (Configurable amplifier Ch1 input pin 0 (+))
MPXIN10	ANALOG6		Multiplexer 1 input pin 0 (Configurable amplifier Ch1 input pin 0 (-))
AGND3	–	–	GND pin for variable output voltage regulator and reference voltage generator
BGR_OUT	ANALOG9	Output	Reference voltage generator output pin
AV_{DD2}	–	–	Power supply pin for variable output voltage regulator and reference voltage generator
LDO_OUT	ANALOG3	Output	Variable output voltage regulator output pin
TEMP_OUT	ANALOG4	Output	Temperature sensor output pin
$\overline{\text{ARESET}}$	ANALOG5	Input	External reset signal input for the functions of analog block
DV_{DD}	–	–	Power supply pin for SPI
$\overline{\text{SCLK}}$	ANALOG8	Input	Serial clock input pin for SPI
SDO	ANALOG12	Output	Serial data output pin for SPI
SDI	ANALOG8	Input	Serial data input pin for SPI
$\overline{\text{CS}}$	ANALOG8	Input	Chip select input pin for SPI
DGND	–	–	GND pin for SPI
DAC4_OUT/ VREFIN4	ANALOG13	I/O	D/A converter Ch4 output pin/gain adjustment amplifier, filter reference voltage input pin
HPF_OUT	ANALOG1	Output	High-pass filter output pin
CLK_HPF	ANALOG7	Input	Pin for inputting high-pass filter control clock
CLK_LPF	ANALOG7	Input	Pin for inputting low-pass filter control clock
AGND4	–	–	GND pin for filter
LPF_OUT	ANALOG1	Output	Low-pass filter output pin

<R>

Figure 2-5. Pin Block Diagram for Pin Type 4-3-1



<R> **Figure 2-9. Pin Block Diagram for Pin Type 7-3-2**



Remarks 1. For alternate functions, see **2. 1. 1 Port functions**.

2. SAU: Serial array unit

3. 4. 3. 1 Port mode register (PMxx)

(1) 64-pin products

Symbol	7	6	5	4	3	2	1	0	Address	After Reset	R/W
PM0	1	PM06	PM05	PM04	PM03	PM02	PM01	PM00	FFF20H	FFH	R/W
PM1	1	PM16	1	PM14	PM13	PM12	PM11	PM10	FFF21H	FFH	R/W
PM2	PM27	PM26	PM25	PM24	PM23	PM22	PM21	PM20	FFF22H	FFH	R/W
PM4	1	1	1	1	PM43	PM42	PM41	PM40	FFF24H	FFH	R/W
PM6	1	1	1	1	PM63	PM62	PM61	PM60	FFF26H	FFH	R/W
PM7	PM77	PM76	PM75	PM74	PM73	PM72	PM71	PM70	FFF27H	FFH	R/W
PM14	1	1	1	1	1	1	PM141	PM140	FFF2EH	FFH	R/W
PM15	1	1	1	PM154	PM153	PM152	PM151	PM150	FFF2FH	FFH	R/W

Cautions 1. Be sure to clear bits 4 to 6 of the PM0 register, bit 6 of the PM1 register, bits 4 to 7 of the PM2 register, bit 3 of the PM4 register, bits 0 to 3 of the PM6 register, bits 4 to 7 of the PM7 register, bits 0 and 1 of the PM14 register, and bits 0 to 4 of the PM15 register to “0”.

2. Be sure to set bit 7 of the PM0 register, bits 5 and 7 of the PM1 register, bits 4 to 7 of the PM4 register, bits 4 to 7 of the PM6 register, bits 2 to 7 of the PM14 register, and bits 5 to 7 of the PM15 register to “1”.

(2) 80-pin products

Symbol	7	6	5	4	3	2	1	0	Address	After Reset	R/W
PM0	1	PM06	PM05	PM04	PM03	PM02	PM01	PM00	FFF20H	FFH	R/W
PM1	1	PM16	PM15	PM14	PM13	PM12	PM11	PM10	FFF21H	FFH	R/W
PM2	PM27	PM26	PM25	PM24	PM23	PM22	PM21	PM20	FFF22H	FFH	R/W
PM4	1	1	1	1	PM43	PM42	PM41	PM40	FFF24H	FFH	R/W
<R> PM5	1	1	1	1	1	1	PM51	PM50	FFF25H	FFH	R/W
PM6	1	1	1	1	PM63	PM62	PM61	PM60	FFF26H	FFH	R/W
PM7	PM77	PM76	PM75	PM74	PM73	PM72	PM71	PM70	FFF27H	FFH	R/W
PM14	1	1	1	1	1	1	PM141	PM140	FFF2EH	FFH	R/W
PM15	1	1	1	PM154	PM153	PM152	PM151	PM150	FFF2FH	FFH	R/W

Cautions 1. Be sure to clear bits 5 and 6 of the PM0 register, bit 6 of the PM1 register, bits 5 to 7 of the PM2 register, bit 3 of the PM4 register, bits 0 to 3 of the PM6 register, bits 4 to 7 of the PM7 register, bit 1 of the PM14 register, and bits 0 to 4 of the PM15 register to “0”.

2. Be sure to set bit 7 of the PM0 register, bit 7 of the PM1 register, bits 4 to 7 of the PM4 register,
<R> **bits 2 to 7 of the PM5 register, bits 4 to 7 of the PM6 register, bits 2 to 7 of the PM14 register, and bits 5 to 7 of the PM15 register to “1”.**

- Format of Timer Mode Register mn (TMRmn) (2/4)

Address: F0190H, F0191H (TMR00) - F019EH, F019FH (TMR07) After reset: 0000H R/W

Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TMRmn (n = 2, 4, 6)	CKS mn1	CKS mn0	0	CCS mn	MASTER mn	STS mn2	STS mn1	STS mn0	CIS mn1	CIS mn0	0	0	MD mn3	MD mn2	MD mn1	MD mn0

Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TMRmn (n = 1, 3)	CKS mn1	CKS mn0	0	CCS mn	SPLIT mn	STS mn2	STS mn1	STS mn0	CIS mn1	CIS mn0	0	0	MD mn3	MD mn2	MD mn1	MD mn0

Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TMRmn (n = 0, 5, 7)	CKS mn1	CKS mn0	0	CCS mn	0[Note]	STS mn2	STS mn1	STS mn0	CIS mn1	CIS mn0	0	0	MD mn3	MD mn2	MD mn1	MD mn0

Bit 11 of TMRmn (n = 2, 4, 6)

MASTER mn	Selection between using channel n independently or simultaneously with another channel (as a slave or master)
0	Operates in independent channel operation function or as slave channel in simultaneous channel operation function.
1	Operates as master channel in simultaneous channel operation function.
Only the channel 2, 4, 6 can be set as a master channel (MASTERmn = 1). Be sure to use channel 0, 5, 7 are fixed to 0 (Regardless of the bit setting, channel 0 operates as master, because it is the highest channel). Clear the MASTERmn bit to 0 for a channel that is used with the independent channel operation function.	

Bit 11 of TMRmn (n = 1, 3)

SPLITmn	Selection of 8 or 16-bit timer operation for channels 1 and 3
0	Operates as 16-bit timer. (Operates in independent channel operation function or as slave channel in simultaneous channel operation function.)
1	Operates as 8-bit timer.

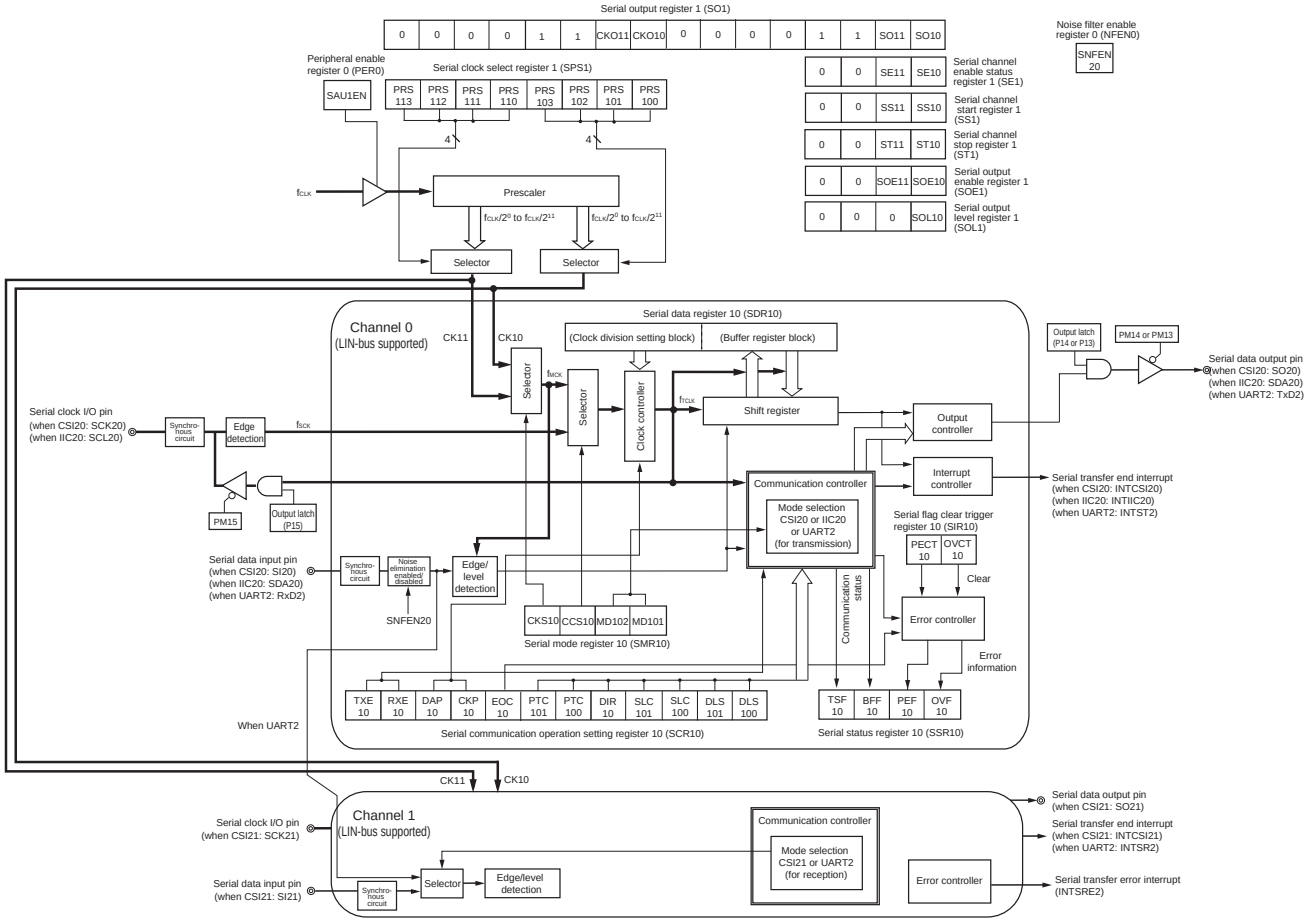
STS mn2	STS mn1	STS mn0	Setting of start trigger or capture trigger of channel n
0	0	0	Only software trigger start is valid (other trigger sources are unselected).
0	0	1	Valid edge of the TImn pin input is used as both the start trigger and capture trigger.
0	1	0	Both the edges of the TImn pin input are used as a start trigger and a capture trigger.
1	0	0	Interrupt signal of the master channel is used (when the channel is used as a slave channel with the simultaneous channel operation function).
Other than above			Setting prohibited

<R> **Note** Bit 11 is fixed at 0 of read only, write is ignored.

Remark m: Unit number (m = 0), n: Channel number (n = 0 to 7 (however, timer input pin (TImn), timer output pin (TOmn): n = 0, 4, 7))

<R> Figure 3-10 shows the block diagram of the serial array unit 1.

Figure 3-10. Block Diagram of Serial Array Unit 1



3. 17. 3 Register controlling key interrupt

The bit settings which are different from that of RL78/G1A (64-pin products) are shown below. For details of each register, see **17. 3 Register Controlling Key Interrupt** in **RL78/G1A Hardware User's Manual (R01UH0305E)**.

3. 17. 3. 1 Key return control register (KRCTL)

The bit setting is same as that of RL78/G1A (64-pin products). For details, see **17. 3. 1 Key return control register (KRCTL)** in **RL78/G1A Hardware User's Manual (R01UH0305E)**.

3. 17. 3. 2 Key return mode register 0 (KRM0)

(1) 64-pin products

Address: FFF37H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
KRM0	0	KRM06	KRM05	KRM04	KRM03	KRM02	KRM01	KRM00

Caution Be sure to clear bit 7 of the KRM0 register to "0".

<R> (2) 80-pin products

Address: FFF37H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
KRM0	KRM07	KRM06	KRM05	KRM04	KRM03	KRM02	KRM01	KRM00

3. 17. 3. 3 Key return flag register (KRF)

The bit setting is same as that of RL78/G1A (64-pin products). For details, see **17. 3. 3 Key return flag register (KRF)** in **RL78/G1A Hardware User's Manual (R01UH0305E)**.

3. 21. 4 Operation of voltage detector

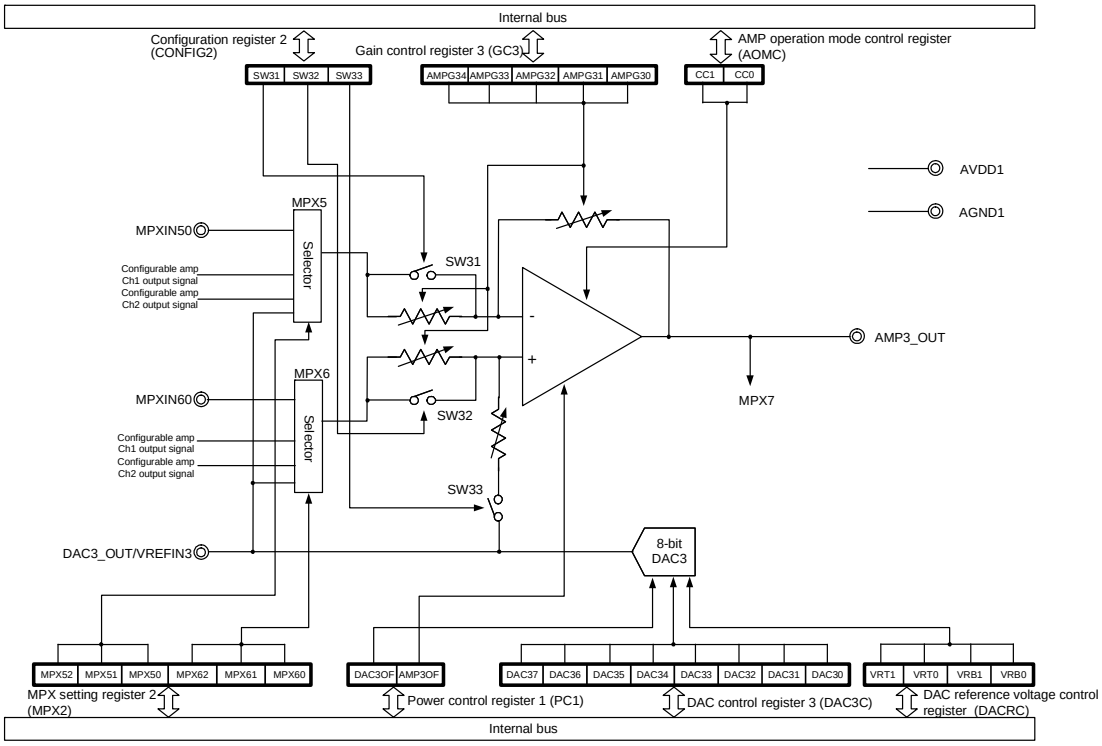
See **21. 4 Operation of Voltage Detector** in **RL78/G1A Hardware User's Manual (R01UH0305E)**.

3. 21. 5 Cautions for voltage detector

See **21. 5 Cautions for Voltage Detector** in **RL78/G1A Hardware User's Manual (R01UH0305E)**.

Figure 4-3. Block Diagram of Configurable Amplifier Ch3

- **64-pin products**



- **80-pin products**

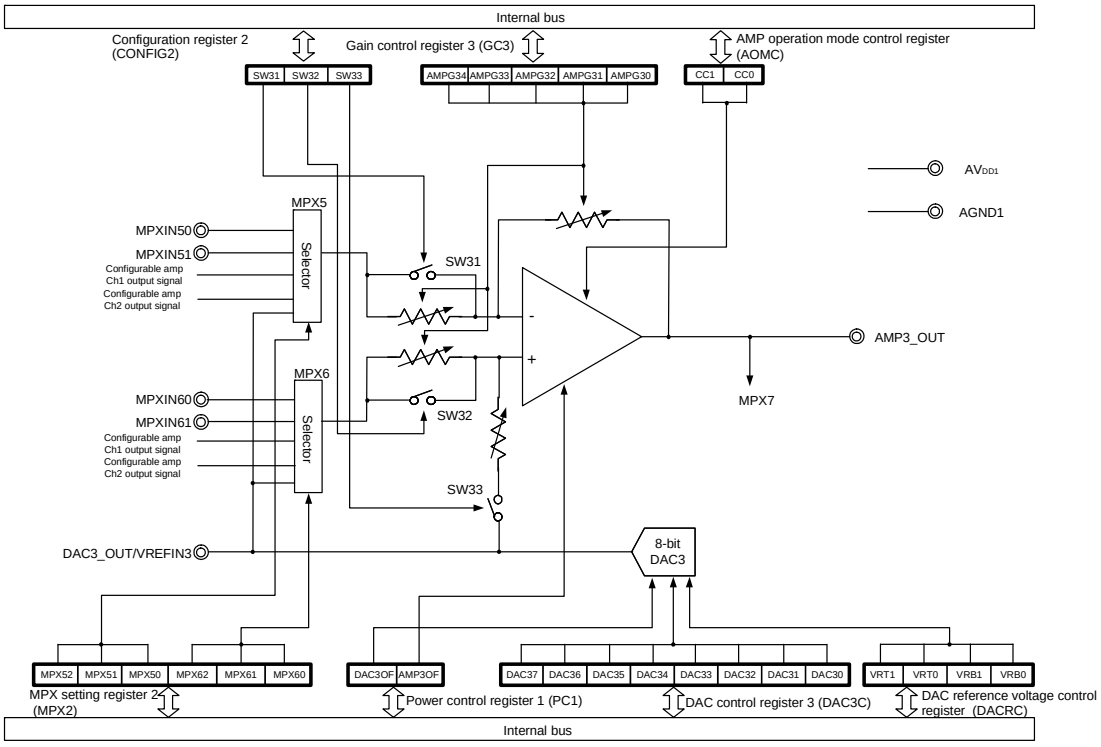
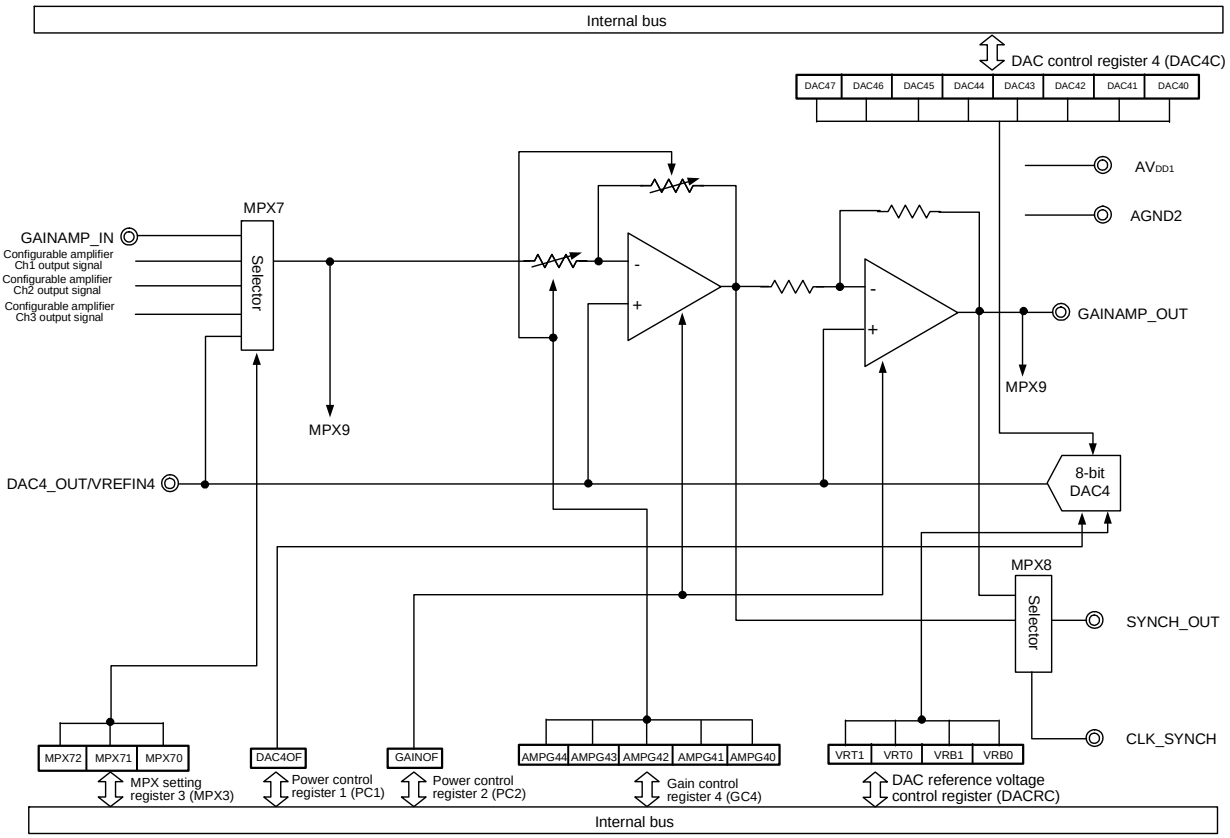


Table 4-3. Feedback Resistance of Configurable Amplifier Ch1 (Transimpedance Amplifier)

AMPG14	AMPG13	AMPG12	AMPG11	AMPG10	Feedback Resistance of Configurable Amplifier Ch1 (Typ.)
0	0	0	0	0	20 kΩ
0	0	0	0	1	
0	0	0	1	0	
0	0	0	1	1	40 kΩ
0	0	1	0	0	
0	0	1	0	1	
0	0	1	1	0	80 kΩ
0	0	1	1	1	
0	1	0	0	0	
0	1	0	0	1	160 kΩ
0	1	0	1	0	
0	1	0	1	1	
0	1	1	0	0	320 kΩ
0	1	1	0	1	
0	1	1	1	0	
0	1	1	1	1	640 kΩ
1	0	0	0	0	
1	0	0	0	1	
Other than above					Setting prohibited

- **80-pin products**



4. 2. 3 Registers controlling the gain adjustment amplifier

The gain adjustment amplifier is controlled by the following 3 registers:

- MPX setting register 3 (MPX3)
- Gain control register 4 (GC4)
- Power control register 2 (PC2)

(1) MPX setting register 3 (MPX3)

This register is used to control MPX7, MPX9, MPX10, and MPX11.

When selecting the signal to be input to the gain adjustment amplifier, use bits 2 to 0.

Reset signal input clears this register to 00H.

- **64-pin products**

Address: 05H After reset: 00H R/W

	7	6	5	4	3	2	1	0
MPX3	0	0	SCF2	SCF1	0	MPX72	MPX71	MPX70

MPX72	MPX71	MPX70	Source of gain adjustment amplifier input
0	0	0	–
0	0	1	Configurable amplifier Ch1 output signal
0	1	0	Configurable amplifier Ch2 output signal
0	1	1	Configurable amplifier Ch3 output signal
1	0	0	D/A converter Ch4 output signal or VREFIN4 pin
Other than above			Setting prohibited

Caution Be sure to clear bit 3 to "0".

<R> **Remark** Bits 7 and 6 are fixed at 0 of read only.

- **80-pin products**

Address: 05H After reset: 00H R/W

	7	6	5	4	3	2	1	0
MPX3	0	0	SCF2	SCF1	SCF0	MPX72	MPX71	MPX70

MPX72	MPX71	MPX70	Source of gain adjustment amplifier input
0	0	0	GAINAMP_IN pin
0	0	1	Configurable amplifier Ch1 output signal
0	1	0	Configurable amplifier Ch2 output signal
0	1	1	Configurable amplifier Ch3 output signal
1	0	0	D/A converter Ch4 output signal or VREFIN4 pin
Other than above			Setting prohibited

<R> **Remark** Bits 7 and 6 are fixed at 0 of read only.

(2) Gain control register 4 (GC4)

This register is used to specify the gain of the gain adjustment amplifier.

Reset signal input clears this register to 00H.

Address: 0AH After reset: 00H R/W

	7	6	5	4	3	2	1	0
GC4	0	0	0	AMP44	AMP43	AMP42	AMP41	AMP40

AMP44	AMP43	AMP42	AMP41	AMP40	Gain
0	0	0	0	0	6 dB
0	0	0	0	1	8 dB
0	0	0	1	0	10 dB
0	0	0	1	1	12 dB
0	0	1	0	0	14 dB
0	0	1	0	1	16 dB
0	0	1	1	0	18 dB
0	0	1	1	1	20 dB
0	1	0	0	0	22 dB
0	1	0	0	1	24 dB
0	1	0	1	0	26 dB
0	1	0	1	1	28 dB
0	1	1	0	0	30 dB
0	1	1	0	1	32 dB
0	1	1	1	0	34 dB
0	1	1	1	1	36 dB
1	0	0	0	0	38 dB
1	0	0	0	1	40 dB
Other than above					Setting prohibited

<R> **Remark** Bits 7 to 5 are fixed at 0 of read only.

Table 4-12. Statuses during Analog Reset

Function Block	External Reset from $\overline{\text{ARESET}}$ Pin	Internal Reset by Reset Control Register (RC)
Configurable amplifier	Operation stops.	
Gain adjustment amplifier	Operation stops.	
D/A converter	Operation stops.	
Low-pass filter	Operation stops.	
High-pass filter Note	Operation stops.	
Temperature sensor	Operation stops.	
Variable output voltage regulator	Operation stops.	
Reference voltage generator	Operation stops.	
SPI	Operation stops.	Operation enabled.

Note 80-pin products only.

Table 4-13. Statuses of SPI Control Registers after Analog Reset Is Acknowledged

Address	SPI Control Register	Status After a Reset Is Acknowledged	
		External Reset	Internal Reset
00H	Configuration register 1 (CONFIG1)	00H	00H
01H	Configuration register 2 (CONFIG2)	00H	00H
03H	MPX setting register 1 (MPX1)	00H	00H
04H	MPX setting register 2 (MPX2)	00H	00H
05H	MPX setting register 3 (MPX3)	00H	00H
06H	Gain control register 1 (GC1)	00H	00H
07H	Gain control register 2 (GC2)	00H	00H
08H	Gain control register 3 (GC3)	00H	00H
09H	AMP operation mode control register (AOMC)	00H	00H
0AH	Gain control register 4 (GC4)	00H	00H
0BH	LDO control register (LDOC)	0DH	0DH
0CH	DAC reference voltage control register (DACRC)	00H	00H
0DH	DAC control register 1 (DAC1C)	80H	80H
0EH	DAC control register 2 (DAC2C)	80H	80H
0FH	DAC control register 3 (DAC3C)	80H	80H
10H	DAC control register 4 (DAC4C)	80H	80H
11H	Power control register 1 (PC1)	00H	00H
12H	Power control register 2 (PC2)	00H	00H
13H	Reset control register (RC)	00H	01H Note

<R> **Note** The reset control register is not initialized by generating internal reset of the reset control register, but it can be done to 00H by generating external reset from $\overline{\text{ARESET}}$ pin or writing 0 to the RESET bit of the reset control register (RC)..

5. 2. 5. 2 Temperature sensor, internal reference voltage output characteristics

(T_A = –40 to +85°C, 2.4 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V, HS (high-speed main) mode)

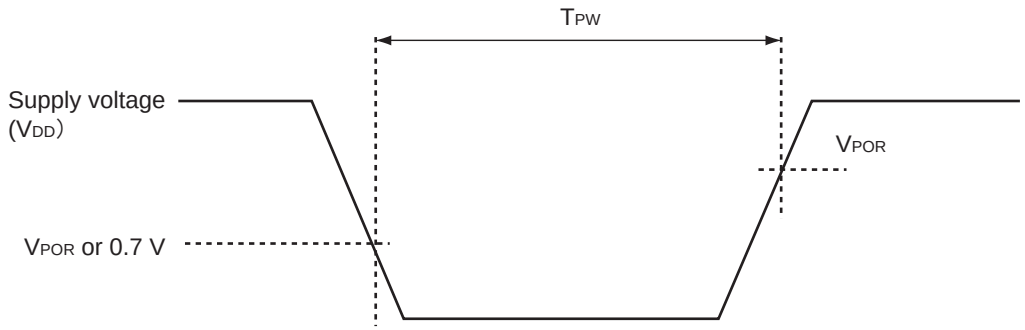
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Temperature sensor output voltage	V_{TMPS25}	ADS register = 80H, T_A = +25°C		1.05		V
Internal reference voltage	V_{BGR}	ADS register = 81H	1.38	1.45	1.5	V
Temperature coefficient	F_{VTMPS}	Temperature sensor output voltage that depends on the temperature		–3.6		mV/°C
Operation stabilization wait time	t_{AMP}		10			μs

5. 2. 5. 3 POR circuit characteristics

(T_A = –40 to +85°C, V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Detection voltage	V_{POR}	When power supply voltage is rising	1.47	1.51	1.55	V
	V_{PDR}	When power supply voltage is falling	1.46	1.50	1.54	V
Minimum pulse width[Note]	T_{PW}		300			μs

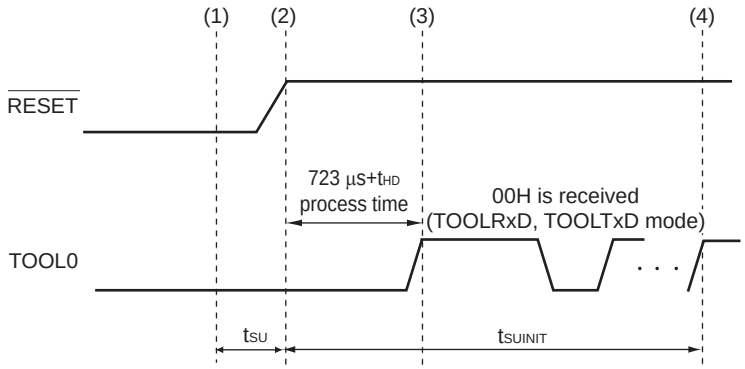
Note This is the time required for the POR circuit to execute a reset when V_{DD} falls below V_{PDR}. When the microcontroller enters STOP mode or if the main system clock (f_{MAIN}) has been stopped by setting bit 0 (HIOSTOP) and bit 7 (MSTOP) of the clock operation status control register (CSC), this is the time required for the POR circuit to execute a reset before V_{DD} rises to V_{POR} after having fallen below 0.7 V.



<R> **5. 2. 9 Timing specs for switching flash memory programming modes**

(T_A = –40 to +85°C, 1.8 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
How long from when a external reset ends until the initial communication settings are specified	t_{SUINIT}	POR and LVD resets must end before the external reset ends.			100	ms
How long from when the TOOL0 pin is placed at the low level until a external reset ends	t_{SU}	POR and LVD resets must end before the external reset ends.	10			μs
How long the TOOL0 pin must be kept at the low level after a reset ends (except flash firmware processing time)	t_{HD}	POR and LVD resets must end before the external reset ends.	1			ms



<1> The low level is input to the TOOL0 pin.

<2> The external reset ends (POR and LVD resets must end before the external reset ends.).

<3> The TOOL0 pin is set to the high level.

<4> The flash memory programming mode is set by UART reception and the baud rate setting completes.

Remark t_{SUINIT}: The segment shows that it is necessary to finish specifying the initial communication settings within 100 ms from when the resets end.

t_{SU}: How long from when the TOOL0 pin is placed at the low level until a external reset ends.

t_{HD}: How long to keep the TOOL0 pin at the low level from when the external or internal resets end (except flash firmware processing time).

5. 3. 3. 2 Gain adjustment amplifier characteristics

(1) 64-pin products

(–40°C ≤ T_A ≤ 85°C, AV_{DD1} = AV_{DD2} = AV_{DD3} = DV_{DD} = 5.0 V, VREFIN4 = 1.7 V, GAINOF = 1, DAC4OF = 0)

Parameter	Symbol	Conditions	Ratings			Unit
			MIN	TYP	MAX	
Current consumption	IccA		–	530	1,300	μA
Input voltage	VINL		AGND2 - 0.1	–	–	V
	VINH		–	–	AV_{DD1} - 0.05	V
Output voltage	VOUTL1	IOL = -100 μA	–	AGND2 + 0.02	AGND2 + 0.05	V
	VOUTH1	IOH = 100 μA	AV_{DD1} - 0.05	AV_{DD1} - 0.02	–	V
Gain bandwidth	GBW2	CL = 30 pF, GC4 = 11H (40 dB)	–	0.86	–	MHz
Input conversion offset voltage	VOFF	GC4 = 00H (6 dB), T_A = 25°C, GAINAMP_IN = 2.5 V	-30	–	30	mV
Input conversion offset voltage temperature coefficient	VOTC2	CLK_SYNCH = L, GAINAMP_OUT pin	–	±18	–	μV/°C
Slew rate	SR	CL = 30 pF	–	0.9	–	V/μs
Equivalent input noise	En_Gain	f = 1 kHz, GC4 = 11H (40 dB)	–	700	–	nV/√ Hz
Power supply rejection ratio	PSRR2	f = 1 kHz, GC4 = 00H (6 dB)	–	45	–	dB
Gain setting error	GAIN_Accu1	T_A = 25°C	-0.6	–	0.6	dB
	GAIN_Accu2	T_A = –40 to 85°C	-1.0	–	1.0	dB

(2/6)

Edition	Description	Chapter
Rev.1.00	Addition of the registers listed in **3. 9. 3 Registers controlling clock output/buzzer output controller**	**CHAPTER 3 MICROCONTROLLER BLOCK**
	Addition of the registers listed in **3. 11. 3 Registers used in A/D converters**	
	Addition and Modification of **Cautions** in **3. 11. 3. 7 Analog input channel specification register (ADS)**	
	Addition of the registers listed in **3. 12. 3 Registers controlling serial array unit**	
	Error correction of the number of maskable interrupts (internal) in **3. 16 Interrupt Functions**	
	Addition of the registers listed in **3. 16. 3 Registers controlling interrupt functions**	
	Error correction of the number of key interrupt input channels for 64-pin products in **3. 17 Key Interrupt Function**	
	Addition of the registers listed in **3. 17. 3 Registers controlling key interrupt**	
	Addition of **Caution** in **3. 17. 3. 2 Key return mode registers 0 (KRM0)**	
	Error correction of the descriptions in **3. 21. Voltage Detector**	
	Addition of the registers listed in **3. 21. 3 Registers controlling voltage detector**	
	Error correction of the descriptions about user option byte (000C1H/010C1H) in **3. 21. 3 Registers controlling voltage detector**	
	Addition of the registers listed in **3. 22. 3 Operation of safety functions**	
	Error correction of the descriptions about user option byte (000C1H/010C1H) in **3. 24. 2 Format of user option byte**	
	Addition of **3. 25 Flash Memory**	
	Addition of **3. 26. 1 Connecting E1 on-chip debugging emulator to RL78/G1E**	
	Addition of the descriptions about the reference voltage in **4. 1. 1 Overview of configurable amplifier features**	**CHAPTER 4 ANALOG BLOCK**
	Modification of the registers listed in **4. 1. 3 Registers controlling the configurable amplifiers**	
	Addition of the descriptions about the reference voltage in **4. 2. 1 Overview of gain adjustment amplifier features**	
	Modification of the registers listed in **4. 2. 3 Registers controlling the gain adjustment amplifier**	
	Modification of the equation for calculation of analog output voltage in **4. 3. 1 Overview of D/A converter features**	
	Addition of the descriptions about the reference voltage in **4. 4. 1 Overview of low-pass filter features**	
	Modification of the registers listed in **4. 4. 3 Registers controlling the low-pass filter**	
	Addition of the descriptions about the reference voltage in **4. 5. 1 Overview of high-pass filter features**	
	Modification of the registers listed in **4. 5. 3 Registers controlling the high-pass filter**	
	Modification of the description in **4. 8. 3 Registers controlling the reference voltage generator**	
	Modification of **Caution** in **4. 9. 1 Overview of SPI features**	
	Addition of **Note** to **Table 4-11.**	