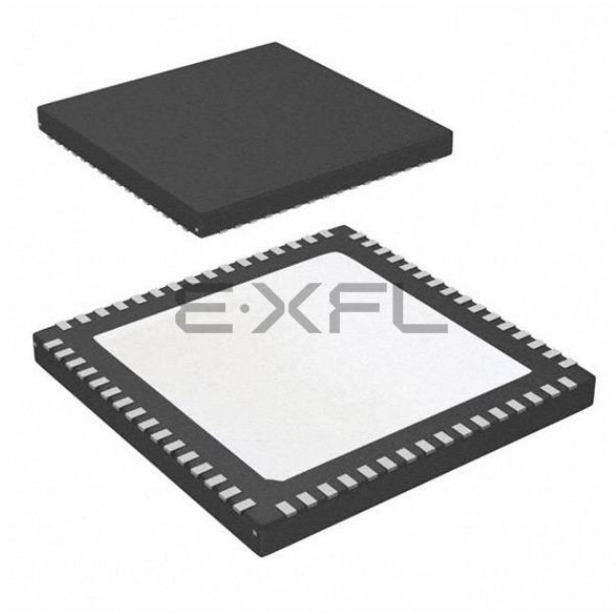
Renesas Electronics America Inc - R5F10FLEANA#YK1 Datasheet



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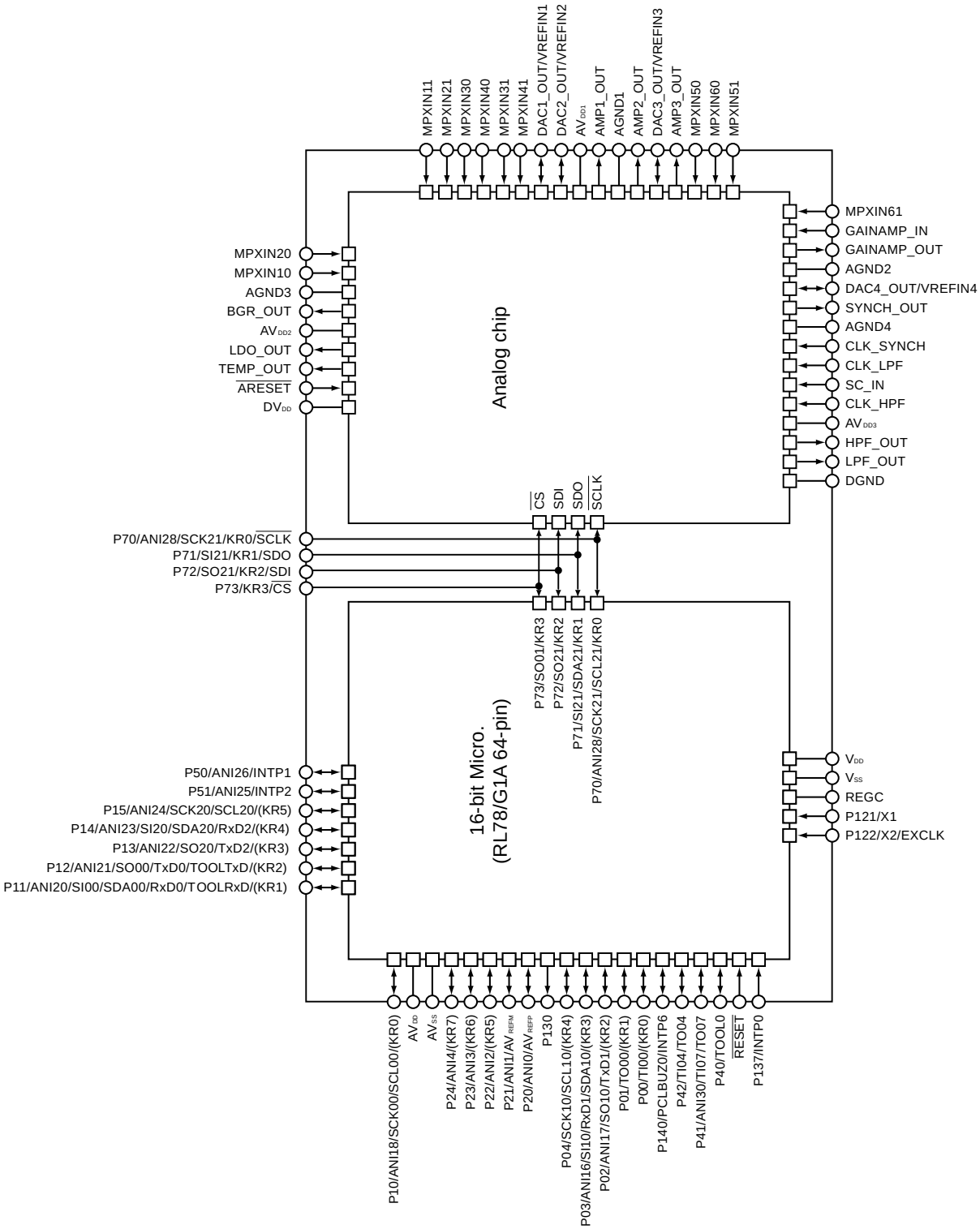
Applications of "Embedded - Microcontrollers"

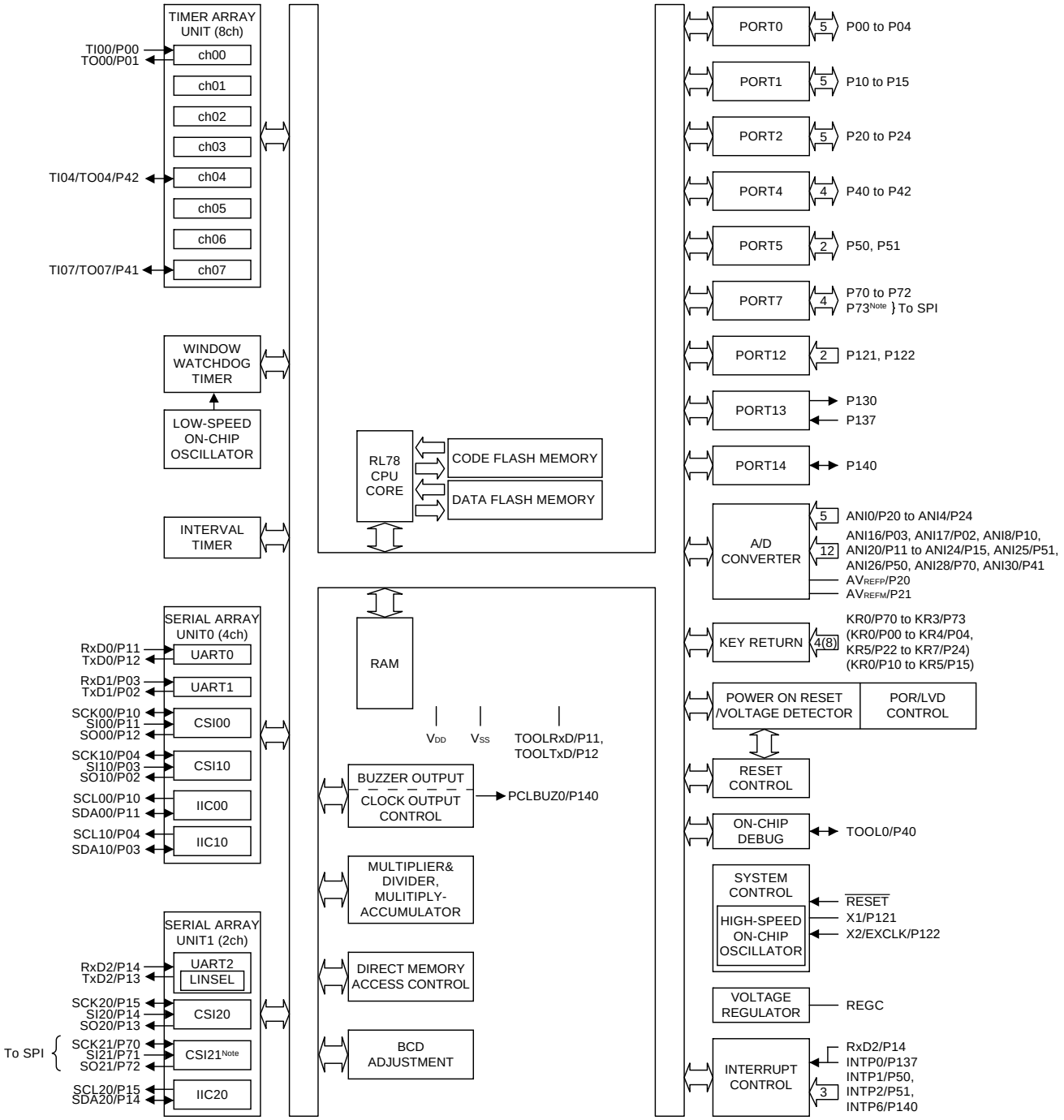
Details	
Product Status	Obsolete
Core Processor	RL78
Core Size	16-Bit
Speed	32MHz
Connectivity	CSI, I²C, LINbus, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	20
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	1.6V ~ 5.5V
Data Converters	A/D 13x8/12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-WFQFN Exposed Pad
Supplier Device Package	64-WQFN (9x9)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f10fleana-yk1

<R> **1. 5. 2 80-pin products**



Remark The RL78/G1E (80-pin products) is a multi-chip package (MCP) device that integrates a chip of an analog block and a chip of 16-bit microcontroller block in a single package.

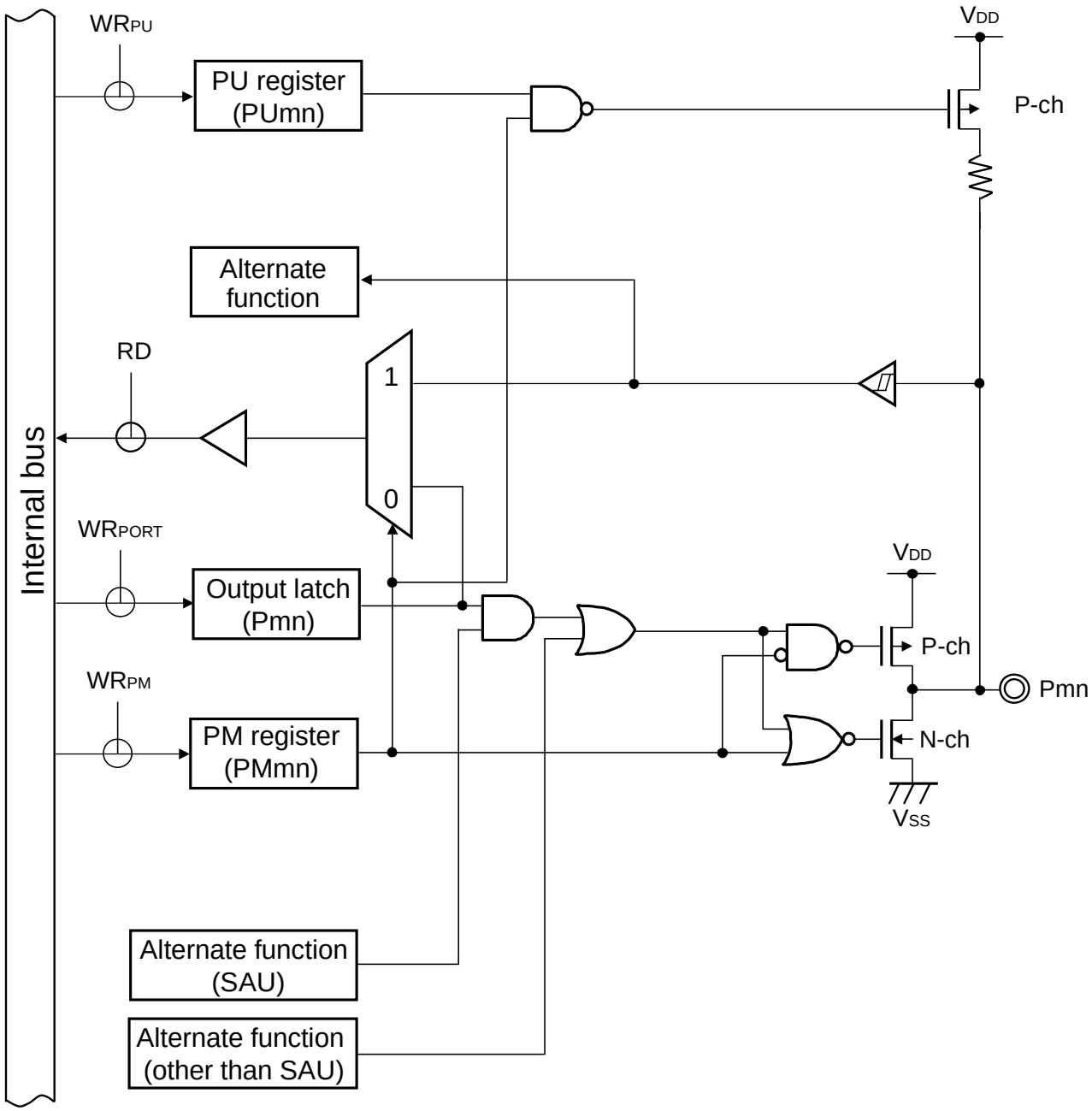
<R> **(1) Block diagram in microcontroller block (80-pin products)**



Note Connected inside the package.

<R>

Figure 2-7. Pin Block Diagram for Pin Type 7-1-2



Remarks 1. For alternate functions, see **2. 1. 1 Port functions**.

2. SAU: Serial array unit

3. 4. 2. 4 Port 3

Port 3 is not available for RL78/G1E.

3. 4. 2. 5 Port 4

Port 4 is an I/O port with an output latch. Port 4 can be set to the input mode or output mode in 1-bit units using port mode register 4 (PM4). When the P40 to P42 pins are used as an input port, use of an on-chip pull-up resistor can be
<R> specified in 1-bit units by pull-up resistor option register 4 (PU4). The P41 pin can be specified as digital input/output or analog input, using port mode control register 4 (PMC4). This port can be also used for A/D converter analog input, data I/O for a flash memory programmer/debugger, and timer I/O. Be sure to connect an external pull-up resistor to the P40 pins when on-chip debugging is enabled to P40 (by using an option byte).

When reset signal is generated, the P40 to P42 pins will be set to input mode.

3. 4. 2. 6 Port 5

Port 5 is an I/O port with an output latch. Port 5 can be set to the input mode or output mode in 1-bit units using port mode register 5 (PM5). When the P50 and P51 pins are used as an input port, use of an on-chip pull-up resistor can be
<R> specified in 1-bit units by pull-up resistor option register 5 (PU5). Output from the P50 pins can be specified as normal CMOS output or N-ch open-drain output (V_{DD} tolerance) in 1-bit units using port output mode register 5 (POM5). The P50 and P51 pins can be specified as digital input/output or analog input in 1-bit units, using port mode control register 5 (PMC5). This port can be also used for A/D converter analog input, and external interrupt request input.

When reset signal is generated, the P50 and P51 pins will be set to input mode.

3. 4. 2. 7 Port 6

Port 6 is not available for RL78/G1E.

3. 4. 2. 8 Port 7

Port 7 is an I/O port with an output latch. Port 7 can be set to the input mode or output mode in 1-bit units using port mode register 7 (PM7). When the P70 to P73 pins are used as an input port, use of an on-chip pull-up resistor can be
<R> specified in 1-bit units by pull-up resistor option register 7 (PU7). The P70 pin can be specified as digital input/output or analog input, using port mode control register 7 (PMC7). This port can be also used for A/D converter analog input, serial interface data I/O, and clock I/O.

When reset signal is generated, the P70 to P73 pins will be set to input mode.

(2) 80-pin products

Address: F0076H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
ADPC	0	0	0	0	0	ADPC2	ADPC1	ADPC0

ADPC2	ADPC1	ADPC0	Analog input (A)/digital I/O (D) switching				
			ANI4/P24	ANI3/P23	ANI2/P22	ANI1/P21	ANI0/P20
0	0	0	A	A	A	A	A
0	0	1	D	D	D	D	D
0	1	0	D	D	D	D	A
0	1	1	D	D	D	A	A
1	0	0	D	D	A	A	A
1	0	1	D	A	A	A	A
Other than above			Setting prohibited				

Cautions 1. Be sure to clear bits 3 to 7 to "0".

2. Set the channel used for A/D conversion to the input mode by using port mode register 2 (PM2).

3. Do not set the pin set by the ADPC register as digital I/O by the analog input channel specification register (ADS).

4. When using AV_{REFP} and AV_{REFM}, specify ANI0 and ANI1 as the analog input channels and specify input mode by using the port mode register.

3. 7 Real-Time Clock

Real-time clock is not provided in RL78/G1E (64-pin products, 80-pin products).

<R> 3. 12. 2. 1 Shift register

This is a 9-bit register that converts parallel data into serial data or vice versa.

In case of the UART communication of nine bits of data, nine bits (bits 0 to 8) are used[Note 1].

The shift register cannot be directly manipulated by program.

During reception, it converts data input to the serial pin into parallel data, and stores to the lower 8/9 bits of the SDRmn register.

When data is transmitted, the value transferred from the lower 8/9 bits of the SDRmn register to this register is output as serial data from the serial output pin.

For details, see **3. 12. 2. 2 Lower 8/9 bits of the serial data register mn (SDRmn)**.

	8	7	6	5	4	3	2	1	0
Shift register									

<R> 3. 12. 2. 2 Lower 8/9 bits of the serial data register mn (SDRmn)

The SDRmn register is the transmit/receive data register (16 bits) of channel n. Bits 8 to 0 of SDR00, SDR01 (lower 9 bits) or bits 7 to 0 of SDR02, SDR03, SDR10Note 1, and SDR11Note 1 (lower 8 bits) function as a transmit/receive buffer register, and bits 15 to 9 (higher 7 bits) are used as a register that sets the division ratio of the operation clock (f_{MCK}).

Remark For the function of the higher 7 bits of the SDRmn register, see **12. 3. 5 Higher 7 bits of the serial data register mn (SDRmn)** in **RL78/G1A Hardware User's Manual (R01UH0305E)**.

When data is received, parallel data converted by the shift register is stored in the lower 8/9 bits. When data is to be transmitted, set transmit to be transferred to the shift register to the lower 8/9 bits.

The data stored in the lower 8/9 bits of this register is as follows, depending on the setting of bits 0 and 1 (DLSmn0, DLSmn1) of serial communication operation setting register mn (SCRmn), regardless of the output sequence of the data.

- 7-bit data length (stored in bits 0 to 6 of SDRmn register)
- 8-bit data length (stored in bits 0 to 7 of SDRmn register)
- 9-bit data length (stored in bits 0 to 8 of SDRmn register)[Note 1]

The SDRmn register can be read or written in 16-bit units.

The lower 8/9 bits of the SDRmn register can be read or written[Note 2] as the following SFR, depending on the communication mode.

- CSIp communication … SIOp (CSIp data register)
- UARTq reception … RXDq (UARTq receive data register)
- UARTq transmission … TXDq (UARTq transmit data register)
- IICr communication … SIOr (IICr data register)

The SDRmn register can be read or written in 16-bit units.

Reset signal generation clears the SDRmn register to 0000H.

Notes 1. Only following UART0 can be specified for the 9-bit data length.

2. Writing in 8-bit units is prohibited when the operation is stopped (SEmn = 0).

Remarks 1. After data is received, "0" is stored in bits 0 to 8 in bit portions that exceed the data length.

2. m: Unit number (m = 0, 1)
n: Channel number (n = 0 to 3)
p: CSI number (80-pin products: p = 00, 10, 20, 21 64-pin products: p = 00, 21)
q: UART number (q = 0 to 2)
r: IIC number (80-pin products: r = 00, 10, 20 64-pin products: r = 00)

3. 16. 3 Registers controlling interrupt functions

The following 6 types of registers are used to control the interrupt functions.

- Interrupt request flag register (IF0L, IF0H, IF1L, IF1H, IF2L, IF2H)
- Interrupt mask flag register (MK0L, MK0H, MK1L, MK1H, MK2L, MK2H)
- Priority specification flag registers (PR00L, PR00H, PR01L, PR01H, PR02L, PR02H, PR10L, PR10H, PR11L, PR11H, PR12L, PR12H)
- External interrupt rising edge enable register (EGP0)
- External interrupt falling edge enable register (EGN0)
- Program status word (PSW)

Table 3-14 shows a list of interrupt request flags, interrupt mask flags, and priority specification flags corresponding to interrupt request sources.

Table 3-14. Flags Corresponding to Interrupt Request Sources (1/4)

Interrupt Source	Interrupt Request Flag		Interrupt Mask Flag		Priority Specification Flag		RL78/G1E	
		Register		Register		Register	64-pin	80-pin
INTWDTI	WDTIIF	IF0L	WDTIMK	MK0L	WDTIPR0, WDTIPR1	PR00L, PR10L	√	√
INTLVI	LVIIF		LVIMK		LVIPR0, LVIPR1		√	√
INTP0	PIF0		PMK0		PPR00, PPR10		√	√
INTP1	PIF1		PMK1		PPR01, PPR11		–	√
INTP2	PIF2		PMK2		PPR02, PPR12		–	√
INTP3	PIF3		PMK3		PPR03, PPR13		–	–
INTP4	PIF4		PMK4		PPR04, PPR14		–	–
INTP5	PIF5		PMK5		PPR05, PPR15		–	–
INTST2[Note 1]	STIF2[Note 1]	IF0H	STMK2[Note 1]	MK0H	STPR02, STPR12[Note 1]	PR00H, PR10H	√	√
INTCSI20[Note 1]	CSIIF20[Note 1]		CSIMK20[Note 1]		CSIPR020, CSIPR120[Note 1]		–	√
INTIIC20[Note 1]	IICIF20[Note 1]		IICMK20[Note 1]		IICPR020, IICPR120[Note 1]		–	√
INTSR2[Note 2]	SRIF2[Note 2]		SRMK2[Note 2]		SRPR02, SRPR12[Note 2]		–	√
INTCSI21[Note 2]	CSIIF21[Note 2]		CSIMK21[Note 2]		CSIPR021, CSIPR121[Note 2]		√	√
INTIIC21[Note 2]	IICIF21[Note 2]		IICMK21[Note 2]		IICPR021, IICPR121[Note 2]		–	–

Notes 1. If one of the interrupt sources INTST2, INTCSI20, and INTIIC20 is generated, bit 0 of the IF0H register is set to 1. Bit 0 of the MK0H, PR00H, and PR10H registers can be used for all three of these interrupt sources.

2. If one of the interrupt sources INTSR2, INTCSI21, and INTIIC21 is generated, bit 1 of the IF0H register is set to 1. Bit 1 of the MK0H, PR00H, and PR10H registers can be used for all three of these interrupt sources.

Notes 1. If one of the interrupt sources INTST1, INTCSI10, and INTIIC10 is generated, bit 0 of the IF1L register is set to 1. Bit 0 of the MK1L, PR01L, and PR11L registers can be used for all three of these interrupt sources.

2. If one of the interrupt sources INTSR1, INTCSI11, and INTIIC11 is generated, bit 1 of the IF1L register is set to 1. Bit 1 of the MK1L, PR01L, and PR11L registers can be used for all three of these interrupt sources.

<R> **3.** Do not use the error interrupt of UART1 reception and the interrupt of channel 3 of TAU0 (while the higher 8 bits are operating at a timer) at the same time because they share flags for the interrupt request sources. If the error interrupt of UART1 reception is not used (EOC03 = 0), UART1 and channel 3 of TAU0 (while the higher 8 bits are operating at a timer) can be used at the same time. If the interrupt source INTSRE1 or INTTM03H is generated, bit 2 of the IF1L register is set to 1. Bit 2 of the MK1L, PR01L, and PR11L registers can be used for both these interrupt sources.

3. 17 Key Interrupt Function

The number of key interrupt input channels differs, depending on the product.

	64-pin products	80-pin products
Key interrupt input channels	4 ch (7 ch)	4 ch (8 ch)

Remarks 1. Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR).

2. Most of the following descriptions in this section use the case of 80-pin products as an example.

3. 17. 1 Functions of key interrupt

A key interrupt (INTKR) can be generated by inputting a rising/falling edge to the key interrupt input pins (KR0 to KR7).

There are two ways to identify the channel(s) to which a valid edge has been input:

- Identify the channel(s) (KR0 to KR7) by using the port input level.
- Identify the channel(s) (KR0 to KR5) by using the key interrupt flag.

Table 3-16. Assignment of Key Interrupt Detection Pins

Key Interrupt Pins	Key return mode register (KRM0)	Key return flag register (KRF)
KR0	KRM00	KRF0
KR1	KRM01	KRF1
KR2	KRM02	KRF2
KR3	KRM03	KRF3
KR4	KRM04	KRF4
KR5	KRM05	KRF5
KR6	KRM06	–
KR7	KRM07	–

Remark KR0 to KR3 (KR0 to KR6): 64-pin products
KR0 to KR3 (KR0 to KR7): 80-pin products
Functions in parentheses can be assigned via settings in the peripheral I/O redirection register (PIOR)

3. 21. 4 Operation of voltage detector

See **21. 4 Operation of Voltage Detector** in **RL78/G1A Hardware User's Manual (R01UH0305E)**.

3. 21. 5 Cautions for voltage detector

See **21. 5 Cautions for Voltage Detector** in **RL78/G1A Hardware User's Manual (R01UH0305E)**.

3. 22. 2 Registers used by safety functions

See **22. 2 Registers Used by Safety Functions** in **RL78/G1A Hardware User's Manual (R01UH0305E)**.

3. 22. 3 Operation of safety functions

3. 22. 3. 1 Flash memory CRC operation function (high-speed CRC)

See **22. 3. 1 Flash memory CRC operation function (high-speed CRC)** in **RL78/G1A Hardware User's Manual (R01UH0305E)**.

3. 22. 3. 2 CRC operation function (general-purpose CRC)

See **22. 3. 2 CRC operation function (general-purpose CRC)** in **RL78/G1A Hardware User's Manual (R01UH0305E)**.

3. 22. 3. 3 RAM parity error detection function

See **22. 3. 3 RAM parity error detection function** in **RL78/G1A Hardware User's Manual (R01UH0305E)**.

3. 22. 3. 4 RAM guard function

See **22. 3. 4 RAM guard function** in **RL78/G1A Hardware User's Manual (R01UH0305E)**.

3. 22. 3. 5 SFR guard function

See **22. 3. 5 SFR guard function** in **RL78/G1A Hardware User's Manual (R01UH0305E)**.

3. 22. 3. 6 Invalid memory access detection function

See **22. 3. 6 Invalid memory access detection function** in **RL78/G1A Hardware User's Manual (R01UH0305E)**.

Format of user option byte (000C2H/010C2H)

Address: 000C2H/010C2H [Note]

7	6	5	4	3	2	1	0
CMODE1	CMODE0	1	0	FRQSEL3	FRQSEL2	FRQSEL1	FRQSEL0

CMODE1	CMODE0	Setting of flash operation mode		
			Operating Frequency Range	Operating Voltage Range
0	0	LV (low voltage main) mode	1 to 4 MHz	1.6 to 5.5 V
1	0	LS (low speed main) mode	1 to 8 MHz	1.8 to 5.5 V
1	1	HS (high speed main) mode	1 to 16 MHz	2.4 to 5.5 V
			1 to 32 MHz	2.7 to 5.5 V
Other than above		Setting prohibited		

FRQSEL3	FRQSEL2	FRQSEL1	FRQSEL0	Frequency of the high-speed on-chip oscillator
1	0	0	0	32 MHz
0	0	0	0	24 MHz
1	0	0	1	16 MHz
0	0	0	1	12 MHz
1	0	1	0	8 MHz
0	0	1	0	6 MHz
1	0	1	1	4 MHz
0	0	1	1	3 MHz
1	1	0	0	2 MHz
1	1	0	1	1 MHz
Other than above				Setting prohibited

Note Set the same value as 000C2H to 010C2H when the boot swap operation is used because 000C2H is replaced by 010C2H.

<R> **Cautions 1. Be sure to set bits 5, 4 to “10B”.**

2. The ranges of operation frequency and operation voltage vary depending on the flash operation mode. For details, see 5. 2. 3 AC characteristics.

3. 27 BCD Correction Circuit

See **CHAPTER 27 BCD CORRECTION CIRCUIT** in **RL78/G1A Hardware User's Manual (R01UH0305E)**.

(3) MPX setting register 1 (MPX1)

This register is used to control MPX1, MPX2, MPX3, and MPX4.

This register is used to select the signal input to configurable amplifiers Ch1 and Ch2.

Reset signal input clears this register to 00H.

Address: 03H After reset: 00H R/W

	7	6	5	4	3	2	1	0
MPX1	MPX11	MPX10	MPX21	MPX20	MPX31	MPX30	MPX41	MPX40

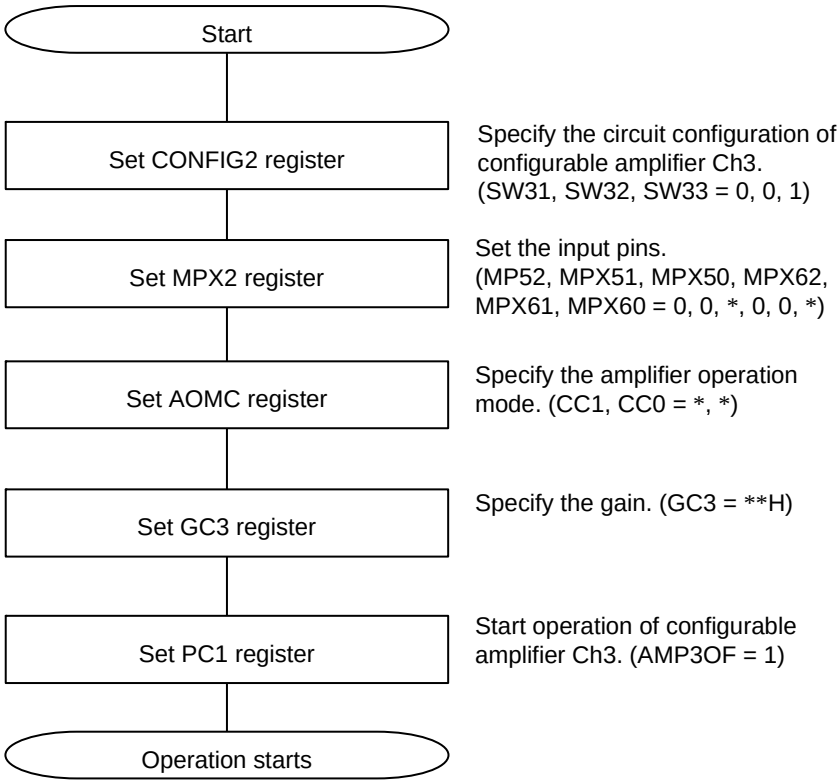
MPX11	MPX10	Source of configurable amplifier Ch1 inverse input
0	0	MPXIN10 pin
0	1	MPXIN11 pin
1	0	D/A converter Ch1 output signal or VREFIN1 pin
1	1	Open pin

MPX21	MPX20	Source of configurable amplifier Ch1 non-inverted input
0	0	MPXIN20 pin
0	1	MPXIN21 pin
1	0	D/A converter Ch1 output signal or VREFIN1 pin
1	1	Open pin

MPX31	MPX30	Source of configurable amplifier Ch2 inverse input
0	0	MPXIN30 pin
0	1	MPXIN31 pin
1	0	D/A converter Ch2 output signal or VREFIN2 pin
1	1	Open pin

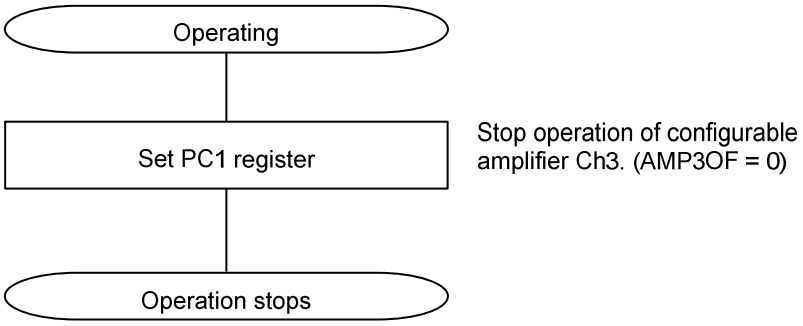
MPX41	MPX40	Source of configurable amplifier Ch2 non-inverted input
0	0	MPXIN40 pin
0	1	MPXIN41 pin
1	0	D/A converter Ch2 output signal or VREFIN2 pin
1	1	Open pin

Example of procedure for starting configurable amplifier Ch3 (differential amplifier)



Remark *: don't care

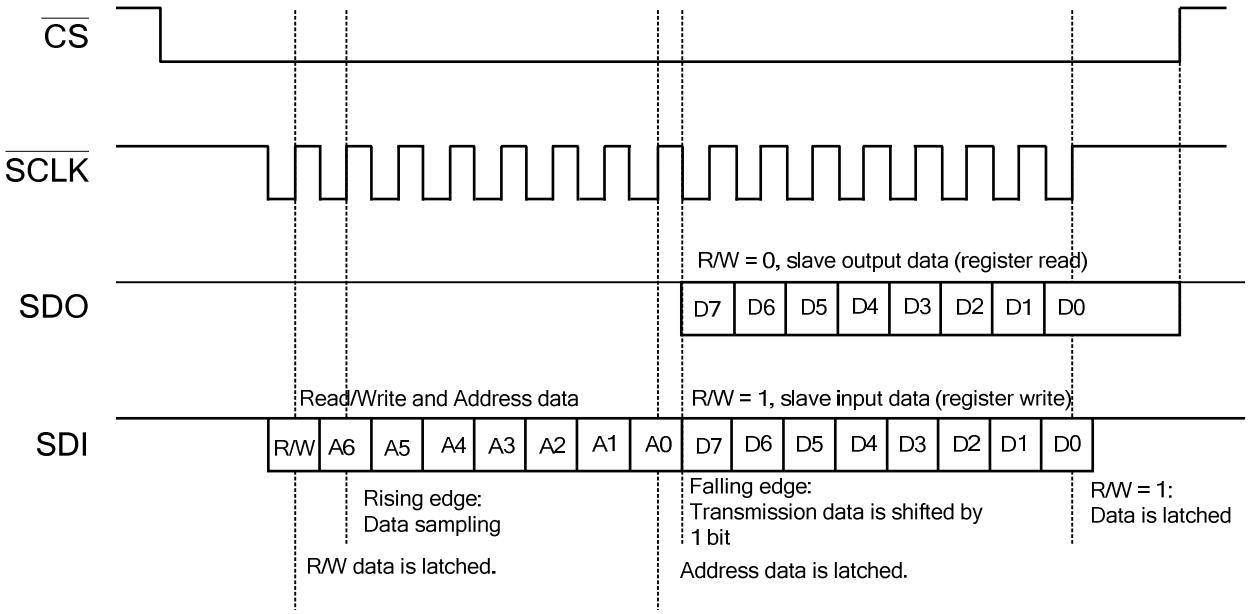
Example of procedure for stopping configurable amplifier Ch3 (differential amplifier)



4. 9. 2 SPI communication

The SPI transmits and receives data in 16-bit units. Data can be transmitted and received when $\overline{CS}$ is low. Data is transmitted one bit at a time in synchronization with the falling edge of the serial clock, and is received one bit at a time in synchronization with the rising edge of the serial clock. When the R/W bit is 1, data is written to the SPI control register in accordance with the address/data setting after the 16th rising edge of $\overline{SCLK}$ has been detected following the fall of $\overline{CS}$, and the operation specified by the data is executed. When the R/W bit is 0, the data is output from the register in accordance with the address/data setting in synchronization with the 9th and later falling edges of $\overline{SCLK}$ following the fall of $\overline{CS}$.

Figure 4-5. SPI Communication Timing



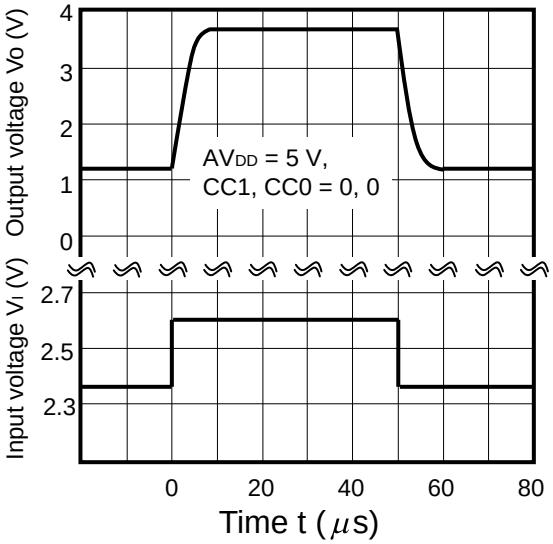
<R> **(8) Communication between devices at different potential (1.8 V, 2.5 V or 3 V) (CSI mode) (master mode, SCKp ... internal clock output) (2/2)**

(T_A = –40 to +85°C, 1.8 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V) (2/2)

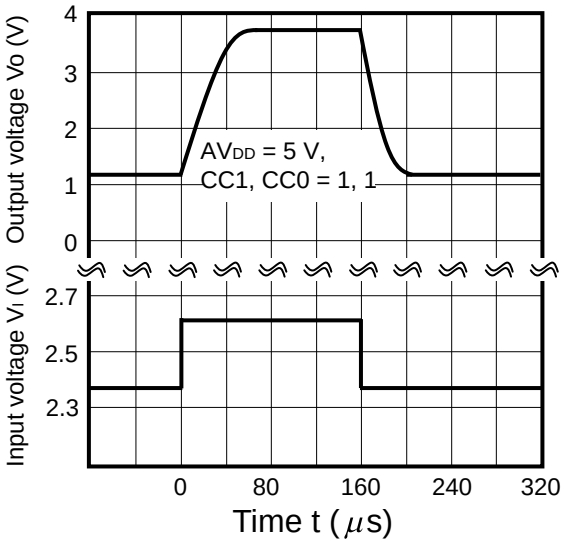
Parameter	Symbol	Conditions	HS Note 1		LS Note 2		LV Note 3		Unit
			MIN	MAX	MIN	MAX	MIN	MAX	
SIp setup time (to SCKp↑) Note 4	t_{SIK1}	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ Vb ≤ 4.0 V, Cb = 30 pF, Rb = 1.4 kΩ	81		479		479		ns
		2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ Vb ≤ 2.7 V, Cb = 30 pF, Rb = 2.7 kΩ	177		479		479		ns
		1.8 V ≤ V_{DD} < 3.3 V, 1.6 V ≤ Vb ≤ 2.0 V, Note 6 Cb = 30 pF, Rb = 5.5 kΩ	479		479		479		ns
SIp hold time (from SCKp↑) Note 4	t_{KSI1}	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ Vb ≤ 4.0 V, Cb = 30 pF, Rb = 1.4 kΩ	19		19		19		ns
		2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ Vb ≤ 2.7 V, Cb = 30 pF, Rb = 2.7 kΩ	19		19		19		ns
		1.8 V ≤ V_{DD} < 3.3 V, 1.6 V ≤ Vb ≤ 2.0 V, Note 6 Cb = 30 pF, Rb = 5.5 kΩ	19		19		19		ns
Delay time from SCKp↓ to SOp output Note 4	t_{KSO1}	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ Vb ≤ 4.0 V, Cb = 30 pF, Rb = 1.4 kΩ		100		100		100	ns
		2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ Vb ≤ 2.7 V, Cb = 30 pF, Rb = 2.7 kΩ		195		195		195	ns
		1.8 V ≤ V_{DD} < 3.3 V, 1.6 V ≤ Vb ≤ 2.0 V, Note 6 Cb = 30 pF, Rb = 5.5 kΩ		483		483		483	ns
SIp setup time (to SCKp↓) Note 5	t_{SIK1}	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ Vb ≤ 4.0 V, Cb = 30 pF, Rb = 1.4 kΩ	44		110		110		ns
		2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ Vb ≤ 2.7 V, Cb = 30 pF, Rb = 2.7 kΩ	44		110		110		ns
		1.8 V ≤ V_{DD} < 3.3 V, 1.6 V ≤ Vb ≤ 2.0 V, Note 6 Cb = 30 pF, Rb = 5.5 kΩ	110		110		110		ns
SIp hold time (from SCKp↓) Note 5	t_{KSI1}	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ Vb ≤ 4.0 V, Cb = 30 pF, Rb = 1.4 kΩ	19		19		19		ns
		2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ Vb ≤ 2.7 V, Cb = 30 pF, Rb = 2.7 kΩ	19		19		19		ns
		1.8 V ≤ V_{DD} < 3.3 V, 1.6 V ≤ Vb ≤ 2.0 V, Note 6 Cb = 30 pF, Rb = 5.5 kΩ	19		19		19		ns
Delay time from SCKp↑ to SOp output Note 5	t_{KSO1}	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ Vb ≤ 4.0 V, Cb = 30 pF, Rb = 1.4 kΩ		25		25		25	ns
		2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ Vb ≤ 2.7 V, Cb = 30 pF, Rb = 2.7 kΩ		25		25		25	ns
		1.8 V ≤ V_{DD} < 4.0 V, 1.6 V ≤ Vb ≤ 2.0 V, Note 6 Cb = 30 pF, Rb = 5.5 kΩ		25		25		25	ns

(**Notes**, **Caution** and **Remarks** are listed on the next page.)

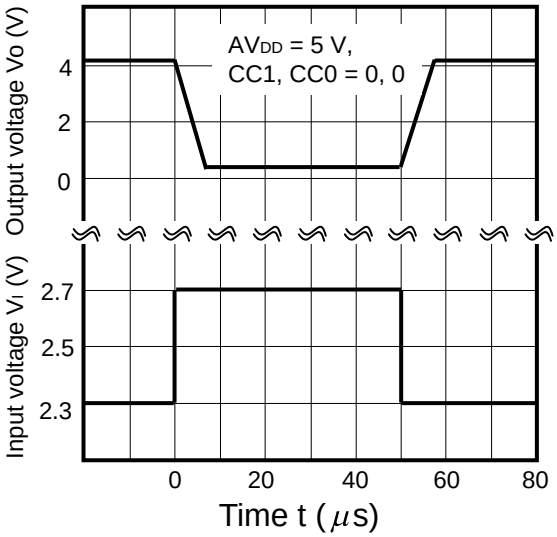
Output response (Differential amplifier)



Output response (Differential amplifier)



Output response (Instrumentation amplifier)



Output response (Instrumentation amplifier)