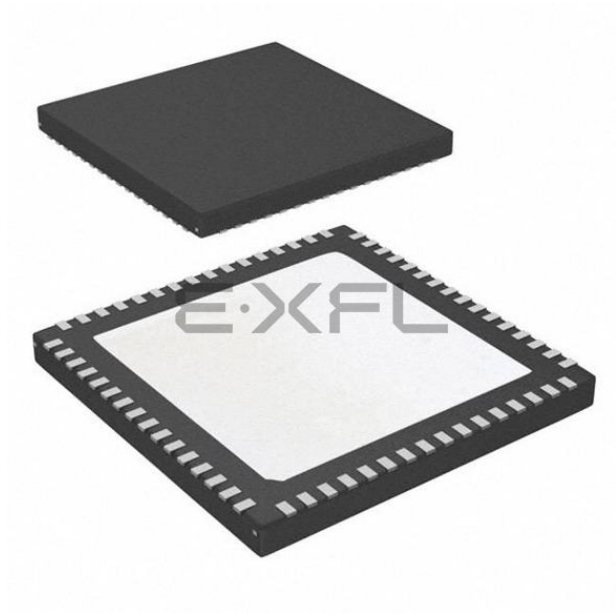
Renesas Electronics America Inc - R5F10FLEDNA#W0 Datasheet



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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	RL78
Core Size	16-Bit
Speed	32MHz
Connectivity	CSI, I²C, LINbus, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	20
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	1.6V ~ 5.5V
Data Converters	A/D 13x8/12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-WFQFN Exposed Pad
Supplier Device Package	64-WQFN (9x9)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f10fledna-w0

(2/2)

<R>

RL78/G1E (64-pin products)		RL78/G1A (64-pin products)	
Function Name	Alternate Function	Function Name	Alternate Function
P70	ANI28/SCK21/KR0/SCLK Note	P70	ANI28/SCK21/SCL21/KR0
P71	SI21/KR1/SDO Note	P71	SI21/SDA21/KR1
P72	SO21/KR2/SDI Note	P72	SO21/KR2
P73	KR3/$\overline{CS}$ Note	P73	SO01/KR3
		P74	SI01/SDA01/INTP8/KR4
		P75	SCK01/SCL01/INTP9/KR5
		P76	INTP10/KR6
		P77	INTP11/KR7
		P120	ANI19
P121	Same as RL78/G1A (64-pin products)	P121	X1
P122	Same as RL78/G1A (64-pin products)	P122	X2/EXCLK
		P123	XT1
		P124	XT2/EXCLKS
P130	Same as RL78/G1A (64-pin products)	P130	–
P137	Same as RL78/G1A (64-pin products)	P137	INTP0
		P140	PCLBUZ0/INTP6
		P141	PCLBUZ1/INTP7
		P150	ANI8
		P151	ANI9/(KR6)
		P152	ANI10/(KR7)
		P153	ANI11/(KR8)
		P154	ANI12/(KR9)

Note $\overline{SCLK}$, SDO, SDI, $\overline{CS}$ represent the pin functions of analog block. P70 to P73 which are connected to the pins of the chip of analog block inside the package have some alternate functions for analog block.

<R> **Remark** Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR). About format, see Figure in **3. 4. 3. 8 Peripheral I/O redirection register (PIOR)**.

<R> 2. 2. 2 80-pin products

Function Name	I/O Circuit Type	I/O	Function
AV_{DD3}	–	–	Power supply pin for filter
SC_IN	ANALOG6	Input	Input pin for filter signal processing
CLK_SYNCH	ANALOG7	Input	Pin for inputting synchronous detector control clock
SYNCH_OUT	ANALOG11	Output	Synchronous detector output pin
AGND2	–	–	GND pin for gain adjustment amplifier
GAINAMP_OUT	ANALOG10	Output	Output pin for gain adjustment amplifier
GAINAMP_IN	ANALOG6	Input	Input pin for gain adjustment amplifier
MPXIN61	ANALOG6	Input	Multiplexer 6 input pin 1 (Configurable amplifier Ch3 input pin 1 (+))
MPXIN51	ANALOG6		Multiplexer 5 input pin 1 (Configurable amplifier Ch3 input pin 1 (-))
MPXIN60	ANALOG6		Multiplexer 6 input pin 0 (Configurable amplifier Ch3 input pin 0 (+))
MPXIN50	ANALOG6		Multiplexer 5 input pin 0 (Configurable amplifier Ch3 input pin 0 (-))
AMP3_OUT	ANALOG10	Output	Configurable amplifier Ch3 output pin
DAC3_OUT/ VREFIN3	ANALOG2	I/O	D/A converter Ch3 output pin/configurable amplifier Ch3 reference voltage input pin
AMP2_OUT	ANALOG11	Output	Configurable amplifier Ch2 output pin
AGND1	–	–	GND pin for configurable amplifiers Ch1 to Ch3
AMP1_OUT	ANALOG11	Output	Configurable amplifier Ch1 output pin
AV_{DD1}	–	–	Power supply pin for configurable amplifiers Ch1 to Ch3
DAC2_OUT/ VREFIN2	ANALOG2	I/O	D/A converter Ch2 output pin/configurable amplifier Ch2 reference voltage input pin
DAC1_OUT/ VREFIN1	ANALOG2		D/A converter Ch1 output pin/configurable amplifier Ch1 reference voltage input pin
MPXIN41	ANALOG6	Input	Multiplexer 4 input pin 1 (Configurable amplifier Ch2 input pin 1 (+))
MPXIN31	ANALOG6		Multiplexer 3 input pin 1 (Configurable amplifier Ch2 input pin 1 (-))
MPXIN40	ANALOG6		Multiplexer 4 input pin 0 (Configurable amplifier Ch2 input pin 0 (+))
MPXIN30	ANALOG6		Multiplexer 3 input pin 0 (Configurable amplifier Ch2 input pin 0 (-))
MPXIN21	ANALOG6		Multiplexer 2 input pin 1 (Configurable amplifier Ch1 input pin 1 (+))
MPXIN11	ANALOG6		Multiplexer 1 input pin 1 (Configurable amplifier Ch1 input pin 1 (-))
MPXIN20	ANALOG6		Multiplexer 2 input pin 0 (Configurable amplifier Ch1 input pin 0 (+))
MPXIN10	ANALOG6		Multiplexer 1 input pin 0 (Configurable amplifier Ch1 input pin 0 (-))
AGND3	–	–	GND pin for variable output voltage regulator and reference voltage generator
BGR_OUT	ANALOG9	Output	Reference voltage generator output pin
AV_{DD2}	–	–	Power supply pin for variable output voltage regulator and reference voltage generator
LDO_OUT	ANALOG3	Output	Variable output voltage regulator output pin
TEMP_OUT	ANALOG4	Output	Temperature sensor output pin
$\overline{\text{ARESET}}$	ANALOG5	Input	External reset signal input for the functions of analog block
DV_{DD}	–	–	Power supply pin for SPI
$\overline{\text{SCLK}}$	ANALOG8	Input	Serial clock input pin for SPI
SDO	ANALOG12	Output	Serial data output pin for SPI
SDI	ANALOG8	Input	Serial data input pin for SPI
$\overline{\text{CS}}$	ANALOG8	Input	Chip select input pin for SPI
DGND	–	–	GND pin for SPI
DAC4_OUT/ VREFIN4	ANALOG13	I/O	D/A converter Ch4 output pin/gain adjustment amplifier, filter reference voltage input pin
HPF_OUT	ANALOG1	Output	High-pass filter output pin
CLK_HPF	ANALOG7	Input	Pin for inputting high-pass filter control clock
CLK_LPF	ANALOG7	Input	Pin for inputting low-pass filter control clock
AGND4	–	–	GND pin for filter
LPF_OUT	ANALOG1	Output	Low-pass filter output pin

2. 5. 24 AGND1

This is the ground pin for configurable amplifiers Ch1 to Ch3.

2. 5. 25 AV_{DD1}

This is the power supply pin for configurable amplifiers Ch1 to Ch3.

2. 5. 26 AGND3

This is the GND pin for variable output voltage regulator and reference voltage generator.

2. 5. 27 BGR_OUT

This is the output pin for reference voltage generator.

2. 5. 28 AV_{DD2}

This is the power supply pin for variable output voltage regulator and reference voltage generator.

2. 5. 29 LDO_OUT

This is the output pin for variable output voltage regulator.

2. 5. 30 TEMP_OUT

This is the output pin for temperature sensor.

2. 5. 31 $\overline{\text{ARESET}}$

This is the active-low system reset input pin for the function of analog block. After turning on DV_{DD}, it is necessary to input the external reset signal to this pin before starting SPI communication. When controlling the external reset signal by the microcontroller block of this package, it is recommended to directly connect this pin to P130 which is to be a low-level output port on reset. If the resource pin of $\overline{\text{ARESET}}$ is to be Hi-Z at a short moment, this pin must be connected to DGND via a resistor. For details of the functions, see **4. 10 Analog Reset**.

2. 5. 32 DV_{DD}

This is the power supply pin for SPI.

2. 5. 33 $\overline{\text{SCLK}}$

This is the serial clock input pin for SPI.

2. 5. 34 SDO

This is the serial data output pin for SPI.

3. 3 CPU Architecture

In this section, the differences of the functions and registers from RL78/G1A (64-pin products) are described. For details, see **CHAPTER 3 CPU ARCHITECURE** in **RL78/G1A Hardware User's Manual (R01UH0305E)**.

3. 3. 1 Memory space

See **3. 1 Memory Space** in **RL78/G1A Hardware User's Manual (R01UH0305E)**.

3. 3. 2 Processor registers

3. 3. 2. 1 Control registers

See **3. 2. 1 Control registers** in **RL78/G1A Hardware User's Manual (R01UH0305E)**.

3. 3. 2. 2 General-purpose registers

See **3. 2. 2 General-purpose registers** in **RL78/G1A Hardware User's Manual (R01UH0305E)**.

3. 3. 2. 3 ES and CS registers

See **3. 2. 3 ES and CS registers** in **RL78/G1A Hardware User's Manual (R01UH0305E)**.

Table 3-3. List of Differences in Expanded Special Function Registers (2nd SFRs) (4/6)

Address	RL78/G1E (64-pin products)			RL78/G1A (64-pin products)		
	2nd SFRs Name	Symbol		2nd SFRs Name	Symbol	
F0148H	Same as RL78/G1A (64-pin products)	SIR10L	SIR10	Serial flag clear trigger register 10	SIR10L	SIR10
F0149H		—			—	
F014AH	Same as RL78/G1A (64-pin products)	SIR11L	SIR11	Serial flag clear trigger register 11	SIR11L	SIR11
F014BH		—			—	
F0150H	Serial mode register 10 Note	SMR10		Serial mode register 10	SMR10	
F0151H						
F0152H	Serial mode register 11 Note	SMR11		Serial mode register 11	SMR11	
F0153H						
F0158H	Serial communication operation setting register 10 Note	SCR10		Serial communication operation setting register 10	SCR10	
F0159H						
F015AH	Serial communication operation setting register 11 Note	SCR11		Serial communication operation setting register 11	SCR11	
F015BH						
F0160H	Same as RL78/G1A (64-pin products)	SE1L	SE1	Serial channel enable status register 1	SE1L	SE1
F0161H		—			—	
F0162H	Same as RL78/G1A (64-pin products)	SS1L	SS1	Serial channel start register 1	SS1L	SS1
F0163H		—			—	
F0164H	Same as RL78/G1A (64-pin products)	ST1L	ST1	Serial channel stop register 1	ST1L	ST1
F0165H		—			—	
F0166H	Same as RL78/G1A (64-pin products)	SPS1L	SPS1	Serial clock select register 1	SPS1L	SPS1
F0167H		—			—	
F0168H	Same as RL78/G1A (64-pin products)	SO1		Serial output register 1	SO1	
F0169H						
F016AH	Same as RL78/G1A (64-pin products)	SOE1L	SOE1	Serial output enable register 1	SOE1L	SOE1
F016BH		—			—	
F0174H	Same as RL78/G1A (64-pin products)	SOL1L	SOL1	Serial output level register 1	SOL1L	SOL1
F0175H		—			—	

Note The bit setting is different from that of RL78/G1A (64-pin products).

3. 4. 3. 5 Port output mode register (POMxx)

(1) 64-pin products

Symbol	7	6	5	4	3	2	1	0	Address	After Reset	R/W
POM0	0	0	0	0	POM03	POM02	0	0	F0050H	00H	R/W
POM1	0	0	0	POM14	POM13	POM12	POM11	POM10	F0051H	00H	R/W

<R> **Caution Be sure to clear bits 0, 1 and 4 to 7 of the POM0 register, and bits 5 to 7 of the POM1 register to "0".**

<R> **(2) 80-pin products**

Symbol	7	6	5	4	3	2	1	0	Address	After Reset	R/W
POM0	0	0	0	POM04	POM03	POM02	0	0	F0050H	00H	R/W
POM1	0	0	POM15	POM14	POM13	POM12	POM11	POM10	F0051H	00H	R/W
POM5	0	0	0	0	0	0	0	POM50	F0055H	00H	R/W

Caution Be sure to clear bits 0, 1 and 5 to 7 of the POM0 register, bits 6 and 7 of the POM1 register, and bits 1 to 7 of the POM5 register to "0".

3. 4. 3. 6 Port mode control register (PMCxx)

<R> **(1) 64-pin products**

Symbol	7	6	5	4	3	2	1	0	Address	After Reset	R/W
PMC0	1	1	1	1	PMC03	PMC02	1	1	F0060H	FFH	R/W
PMC1	1	1	1	PMC14	PMC13	PMC12	PMC11	PMC10	F0061H	FFH	R/W
PMC4	1	1	1	1	1	1	PMC41	1	F0064H	FFH	R/W
PMC7	1	1	1	1	1	1	1	PMC70	F0067H	FFH	R/W

Caution Be sure to set bits 0, 1 and 4 to 7 of the PMC0 register, bits 5 to 7 of the PMC1 register, bits 0 and 2 to 7 of the PMC4 register, and bits 1 to 7 of the PMC7 register to "0".

<R> **(2) 80-pin products**

Symbol	7	6	5	4	3	2	1	0	Address	After Reset	R/W
PMC0	1	1	1	1	PMC03	PMC02	1	1	F0060H	FFH	R/W
PMC1	1	1	PMC15	PMC14	PMC13	PMC12	PMC11	PMC10	F0061H	FFH	R/W
PMC4	1	1	1	1	1	1	PMC41	1	F0064H	FFH	R/W
PMC5	1	1	1	1	1	1	PMC51	PMC50	F0065H	FFH	R/W
PMC7	1	1	1	1	1	1	1	PMC70	F0067H	FFH	R/W

Caution Be sure to set bits 0, 1 and 4 to 7 of the PMC0 register, bits 6 and 7 of the PMC1 register, bits 0 and 2 to 7 of the PMC4 register, bits 2 to 7 of the PMC5 register, and bits 1 to 7 of the PMC7 register to "0".

<R> 3. 4. 4. 5 Handling different potential (1.8 V ,2.5 V or 3V) by using I/O buffers

It is possible to connect an external device operating on a different potential (1.8 V, 2.5 V or 3V) by switching I/O buffers with the port input mode register (PIMxx) and port output mode register (POMxx).

When receiving input from an external device with a different potential (1.8 V, 2.5 V or 3V), set the port input mode registers 0 and 1 (PIM0 and PIM1) on a bit-by-bit basis to enable normal input (CMOS)/TTL input buffer switching.

When outputting data to an external device with a different potential (1.8 V, 2.5 V or 3V), set the port output mode registers 0 and 1 (POM0 and POM1) on a bit-by-bit basis to enable N-ch open drain (V_{DD} tolerance) switching.

Following, describes the connection of a serial interface.

(1) Setting procedure when using input ports of UART0 to UART2, CSI00, CSI10, and CSI20 functions for the TTL input buffer

In case of UART0: P11
In case of UART1: P03
In case of UART2: P14
In case of CSI00: P10, P11
In case of CSI10: P03, P04
In case of CSI20: P14, P15

<1> Using an external resistor, pull up externally the input pin to be used to the power supply of the target device (on-chip pull-up resistor cannot be used).

<2> Set the corresponding bit of the PIM0 and PIM1 registers to 1 to switch to the TTL input buffer. For V_{IH} and V_{IL}, refer to the DC characteristics when the TTL input buffer is selected.

<3> Enable the operation of the serial array unit and set the mode to the UART/CSI mode.

3. 5 Clock Generator

In this section, the differences of the functions and registers from RL78/G1A (64-pin products) are described. For details, see **CHAPTER 5 CLOCK GENERATOR** in **RL78/G1A Hardware User's Manual (R01UH0305E)**.

3. 5. 1 Functions of clock generator

The clock generator generates the clock to be supplied to the CPU and peripheral hardware.

The following two kinds of system clocks and clock oscillators are selectable.

Caution The subsystem clock is not provided in the RL78/G1E (64-pin products, 80-pin products).

(1) Main system clock

<1> X1 oscillator

This circuit oscillates a clock of f_X = 1 to 20 MHz by connecting a resonator to X1 and X2.

Oscillation can be stopped by executing the STOP instruction or setting of the MSTOP bit (bit 7 of the clock operation status control register (CSC)).

<2> High-speed on-chip oscillator (High-speed OCD)

<R> The frequency at which to oscillate can be selected from among f_{IH} = 32, 24, 16, 12, 8, 6, 4, 3, 2 or 1 MHz (typ.) by using the option byte (000C2H). After a reset release, the CPU always starts operating with this high-speed on-chip oscillator clock. Oscillation can be stopped by executing the STOP instruction or setting the HIOSTOP bit (bit 0 of the CSC register).

The frequency specified by using an option byte can be changed by using the high-speed on-chip oscillator frequency select register (HOCODIV). For details about the frequency, see **3. 5. 3. 8 High-speed on-chip oscillator frequency select register (HOCODIV)**.

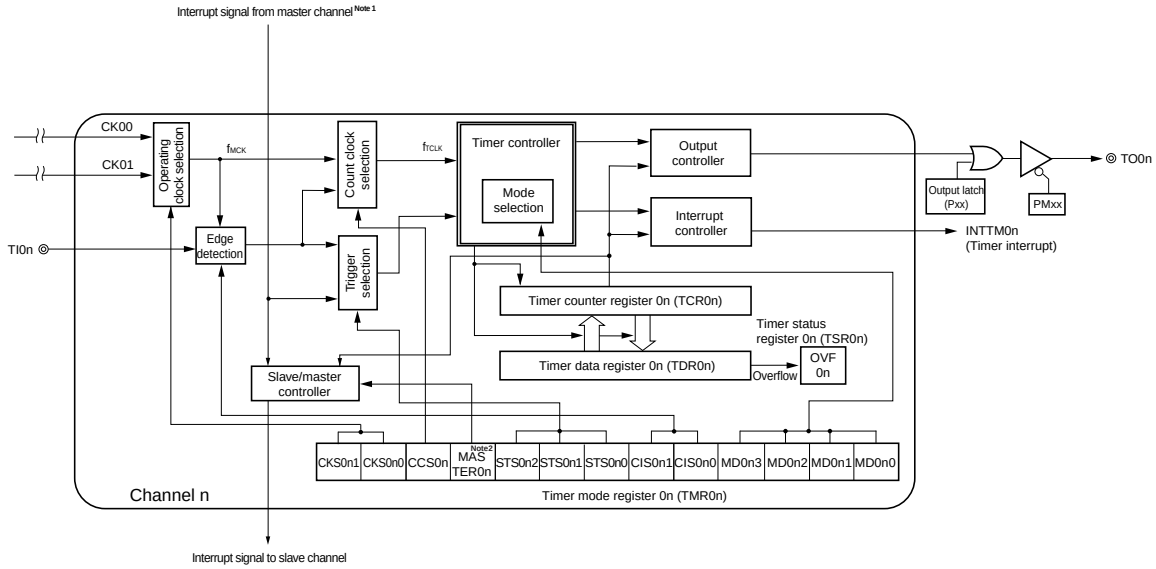
The frequencies that can be specified for the high-speed on-chip oscillator by using the option byte and the high-speed on-chip oscillator frequency select register (HOCODIV) are shown below.

Power Supply Voltage	Flash Operation Mode	Oscillation Frequency (MHz)									
		1	2	3	4	6	8	12	16	24	32
2.7 V ≤ V_{DD} ≤ 5.5 V	HS (high-speed main) mode	√	√	√	√	√	√	√	√	√	√
2.4 V ≤ V_{DD} ≤ 5.5 V		√	√	√	√	√	√	√	√	–	–
1.8 V ≤ V_{DD} ≤ 5.5 V	LS (low-speed main) mode	√	√	√	√	√	√	–	–	–	–
1.6 V ≤ V_{DD} ≤ 5.5 V	LV (low-voltage main) mode	√	√	–	√	–	–	–	–	–	–

An external main system clock (f_{EX} = 1 to 20 MHz) can also be supplied from the EXCLK/X2/P122 pin. An external main system clock input can be disabled by executing the STOP instruction or setting of the MSTOP bit.

As the main system clock, a high-speed system clock (X1 clock or external main system clock) or high-speed on-chip oscillator clock can be selected by setting of the MCM0 bit (bit 4 of the system clock control register (CKC)).

Figure 3-4. Internal Block Diagram of Channel 0, 4 of Timer Array Unit 0

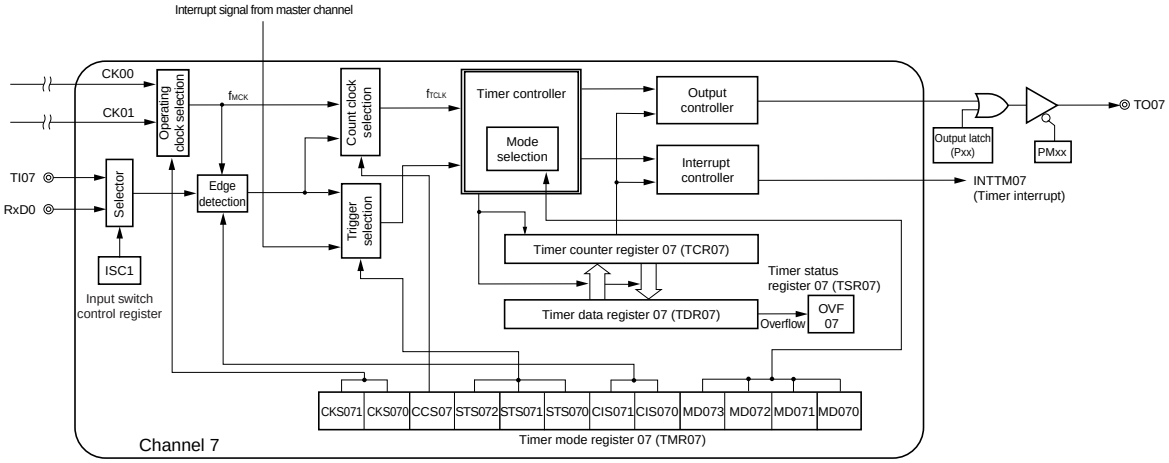


Notes 1. Channels 4 only

2. n = 4 only

Remark n = 0, 4

Figure 3-5. Internal Block Diagram of Channel 7 of Timer Array Unit 0



<R> Figure 3-9 shows the block diagram of the serial array unit 0.

Figure 3-9. Block Diagram of Serial Array Unit 0

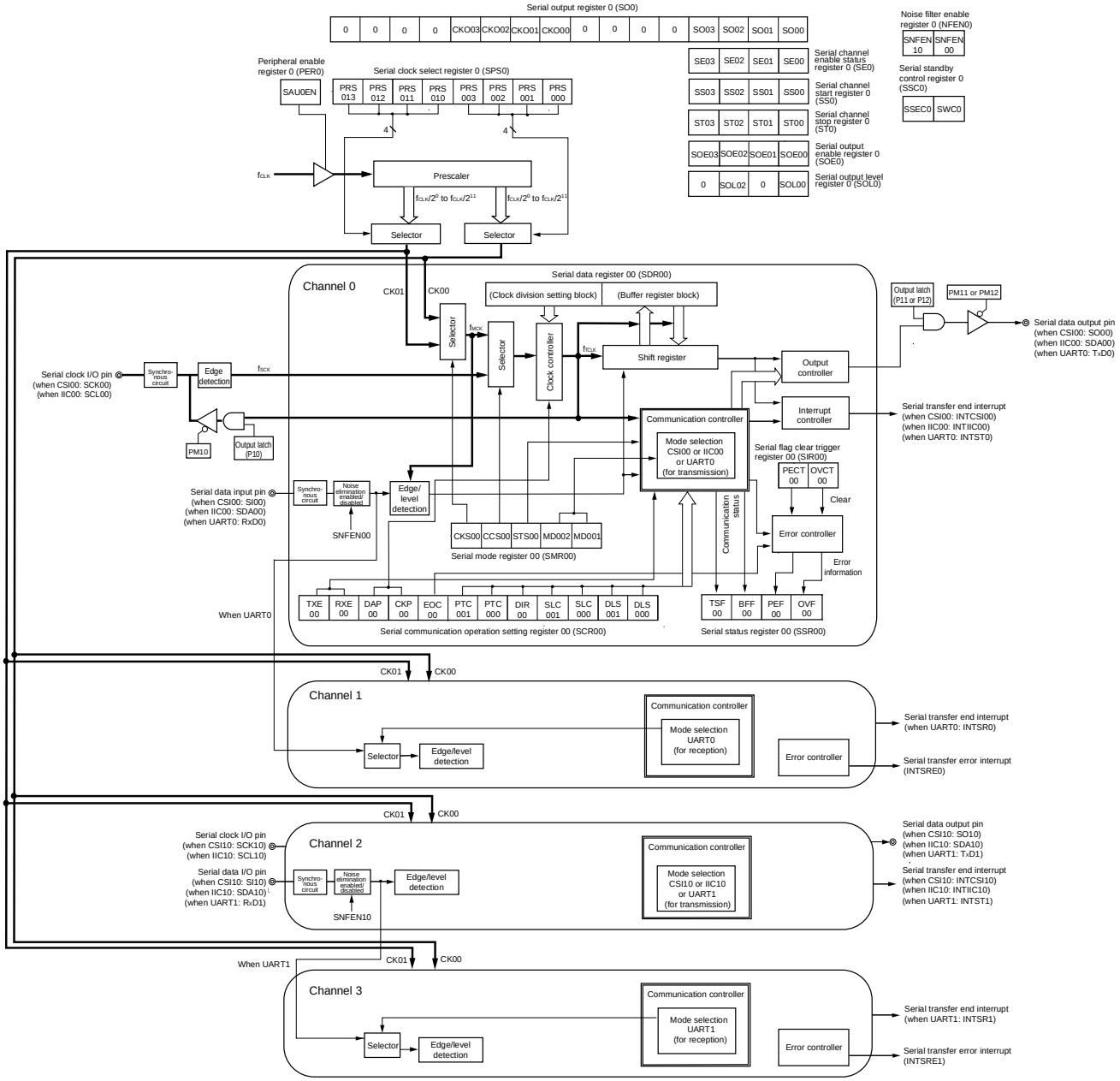


Table 3-13. Interrupt Source List (1/3)

Interrupt Type	Default Priority[Note 1]	Interrupt Source		Internal/External	Vector Table Address	Basic Configuration Type[Note 2]	RL78/G1E	
		Name	Trigger				64-pin	80-pin
Maskable	0	INTWDTI	Watchdog timer interval[Note 3] (75% of overflow time + 1/2f_{IL})	Internal	0004H	(A)	√	√
	1	INTLVI	Voltage detection[Note 4]		0006H		√	√
	2	INTP0	Pin input edge detection	External	0008H	(B)	√	√
	3	INTP1			000AH		–	√
	4	INTP2			000CH		–	√
	5	INTP3			000EH		–	–
	6	INTP4			0010H		–	–
	7	INTP5			0012H		–	–
	8	INTST2/ INTCSI20/ INTIIC20	UART2 transmission transfer end or buffer empty interrupt/ CSI20 transfer end or buffer empty interrupt/ IIC20 transfer end	Internal	0014H	(A)	√[Note 5]	√
	9	INTSR2/ INTCSI21/ INTIIC21	UART2 reception transfer end or buffer empty interrupt/ CSI21 transfer end or buffer empty interrupt/ IIC21 transfer end		0016H		√[Note 6]	√[Note 6]
	10	INTSRE2	UART2 reception communication error occurrence		0018H		√	√
	11	INTDMA0	End of DMA0 transfer		001AH		√	√
	12	INTDMA1	End of DMA1 transfer		001CH		√	√
	13	INTST0/ INTCSI00/ INTIIC00	UART0 transmission transfer end or buffer empty interrupt/ CSI00 transfer end or buffer empty interrupt/ IIC00 transfer end		001EH		√	√
	14	INTSR0/ INTCSI01/ INTIIC01	UART0 reception transfer end or buffer empty interrupt/ CSI01 transfer end or buffer empty interrupt/ IIC01 transfer end		0020H		√[Note 7]	√[Note 7]
	15	INTSRE0	UART0 reception communication error occurrence		0022H		√	√
<R>		INTTM01H	End of timer channel 1 count or capture (at higher 8-bit timer operation)				√	√

Notes 1. The default priority determines the sequence of interrupts if two or more maskable interrupts occur simultaneously. Zero indicates the highest priority and 53 indicates the lowest priority.

2. Basic configuration types (A) to (D) correspond to (A) to (D) in Figure 3-13.

3. When bit 7 (WDTINT) of the option byte (000C0H) is set to 1.

4. When bit 7 (LVIMD) of the voltage detection level register (LVIS) is cleared to 0.

5. INTST2 only.

6. INTSR2 and INTCSI21 only.

7. INTSR0 only.

Address: FFFD8H After reset: FFH R/W

Symbol	7	6	5	4	3	<2>	<1>	<0>
PR02L	1	1	1	1	1	TMPR007	TMPR006	TMPR005

Address: FFFDCH After reset: FFH R/W

Symbol	7	6	5	4	3	<2>	<1>	<0>
PR12L	1	1	1	1	1	TMPR107	TMPR106	TMPR105

Address: FFFD9H After reset: FFH R/W

Symbol	<7>	6	<5>	4	3	2	1	0
PR02H	FLPR0	1	MDPR0	1	1	1	1	1

Address: FFFDDH After reset: FFH R/W

Symbol	<7>	6	<5>	4	3	2	1	0
PR12H	FLPR1	1	MDPR1	1	1	1	1	1

Cautions 1. Be sure to set bits 3 to 7 of the PR00L register to “1”.

2. Be sure to set bits 3 to 7 of the PR10L register to “1”.

3. Be sure to set bit 3 of the PR01L register to “1”.

4. Be sure to set bit 3 of the PR11L register to “1”.

5. Be sure to set bits 1 and 4 to 6 of the PR01H register to “1”.

6. Be sure to set bits 1 and 4 to 6 of the PR11H register to “1”.

7. Be sure to set bits 3 to 7 of the PR02L register to “1”.

8. Be sure to set bits 3 to 7 of the PR12L register to “1”.

9. Be sure to set bits 0 to 4 and 6 of the PR02H register to “1”.

10. Be sure to set bits 0 to 4 and 6 of the PR12H register to “1”.

3. 16. 3. 5 Program status word (PSW)

The bit setting is same as that of RL78/G1A (64-pin products). For details, see **16. 3. 5 Program status word (PSW)** in **RL78/G1A Hardware User's Manual (R01UH0305E)**.

3. 16. 4 Interrupt servicing operations

See **16. 4 Interrupt Servicing Operations** in **RL78/G1A Hardware User's Manual (R01UH0305E)**.

3. 21. 3 Registers controlling voltage detector

The bit settings which are different from that of RL78/G1A (64-pin products) are shown below. For details of each register, see **21. 3 Registers Controlling Voltage Detector** in **RL78/G1A Hardware User's Manual (R01UH0305E)**.

3. 21. 3. 1 Voltage detection register (LVIM)

The bit setting is same as that of RL78/G1A (64-pin products). For details, see **21. 3. 1 Voltage detection register (LVIM)** in **RL78/G1A Hardware User's Manual (R01UH0305E)**.

3. 21. 3. 2 Voltage detection level register (LVIS)

The bit setting is same as that of RL78/G1A (64-pin products). For details, see **21. 3. 2 Voltage detection level register (LVIS)** in **RL78/G1A Hardware User's Manual (R01UH0305E)**.

Format of User Option Byte (000C1H/010C1H) (2/2)

Address: 000C1H/010C1H[Note]

7	6	5	4	3	2	1	0
VPOC2	VPOC1	VPOC0	1	LVIS1	LVIS0	LVIMDS1	LVIMDS0

- LVD setting (interrupt mode)

<R>

Detection voltage		Option byte setting value						
V_{LVDH}		VPOC2	VPOC1	VPOC0	LVIS1	LVIS0	Mode setting	
Rising edge	Falling edge						LVIMDS1	LVIMDS0
3.13	3.06	0	0	1	0	0	0	1
3.75	3.67	0	1	0	0	0		
4.06	3.98	0	1	1	0	0		
–		Value other than above is setting prohibited.						

- LVD off (use of external reset input via $\overline{\text{RESET}}$ pin)

<R>

Detection voltage		Option byte setting value						
V_{LVD}		VPOC2	VPOC1	VPOC0	LVIS1	LVIS0	Mode setting	
Rising edge	Falling edge						LVIMDS1	LVIMDS0
–	–	1	×	×	×	×	×	1
–		Value other than above is setting prohibited.						

Note Set the same value as 000C1H to 010C1H when the boot swap operation is used because 000C1H is replaced by 010C1H.

<R> **Cautions1. Set bit 4 to 1.**

2. After power is supplied, the reset state must be retained until the operating voltage becomes in the range defined in 5. 2. 3 AC characteristics. This is done by utilizing the voltage detector or controlling the externally input reset signal. After the power supply is turned off, this LSI should be placed in the STOP mode, or placed in the reset state by utilizing the voltage detector or controlling the externally input reset signal, before the voltage falls below the operating range. The range of operating voltage varies with the setting of the user option byte (000C2H or 010C2H).

<R> **Remarks 1.** ×: don't care

2. For details on the LVD circuit, see **3. 21 Voltage Detector**.

3. The detection voltage is a TYP. value. For details, see **5. 2. 5. 4 LVD circuit characteristics**.

<R> **3. 25. 2 Serial programming using external device (that Incorporates UART)**

See **25. 2 Serial Programming Using External Device (that Incorporates UART)** in **RL78/G1A Hardware User's Manual (R01UH0305E)**.

3. 25. 3 Connection of pins on board

See **25. 3 Connection of Pins on Board** in **RL78/G1A Hardware User's Manual (R01UH0305E)**.

<R> **3. 25. 4 Serial programming method**

See **25. 4 Serial Programming Method** in **RL78/G1A Hardware User's Manual (R01UH0305E)**.

<R> **3. 25. 5 Processing time for each command when PG-FP5 Is in use (Reference value)**

See **25. 5 Processing Time for Each Command When PG-FP5 Is in Use (Reference Value)** in **RL78/G1A Hardware User's Manual (R01UH0305E)**.

<R> **3. 25. 6 Self-programming**

See **25. 6 Self-Programming** in **RL78/G1A Hardware User's Manual (R01UH0305E)**.

<R> **3. 25. 7 Security Settings**

See **25. 7 Security Settings** in **RL78/G1A Hardware User's Manual (R01UH0305E)**.

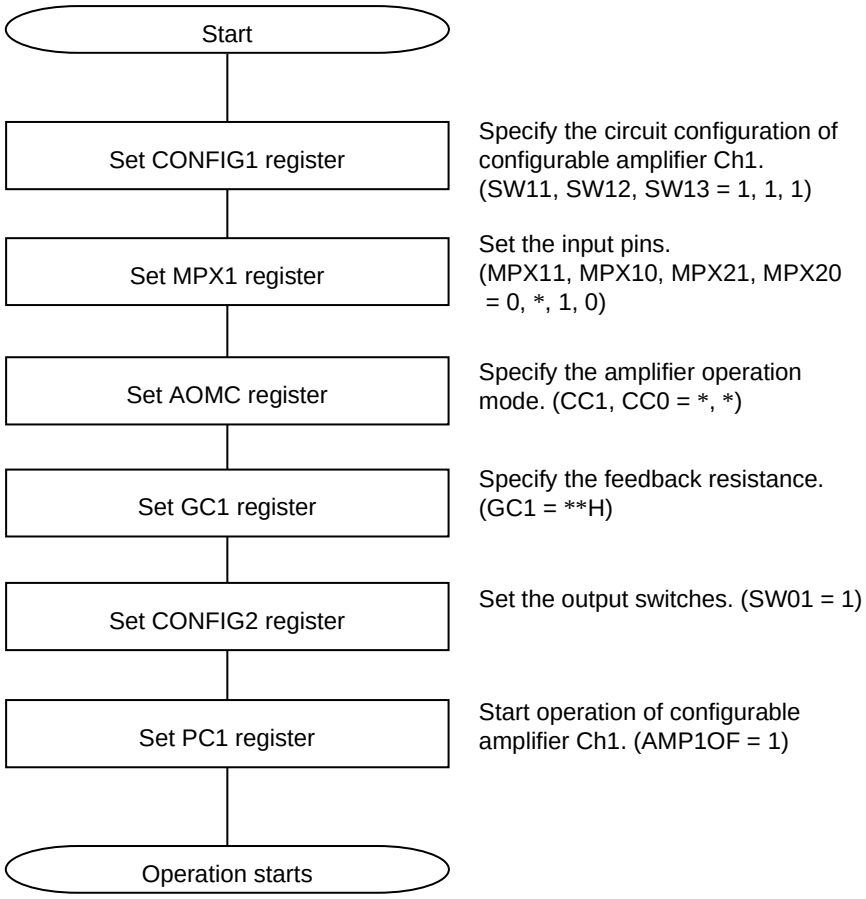
<R> **3. 25. 8 Data flash**

See **25. 8 Data Flash** in **RL78/G1A Hardware User's Manual (R01UH0305E)**.

(4) Procedure when using the amplifiers as a transimpedance amplifier

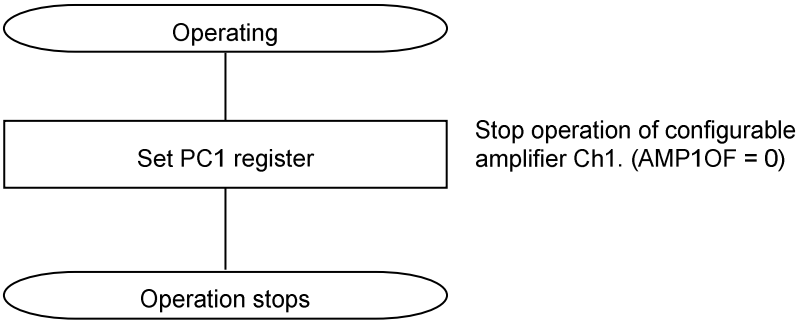
When using the configurable amplifiers as transimpedance amplifiers, follow the procedures below to start and stop the amplifiers.

Example of procedure for starting configurable amplifier Ch1 (transimpedance amplifier)

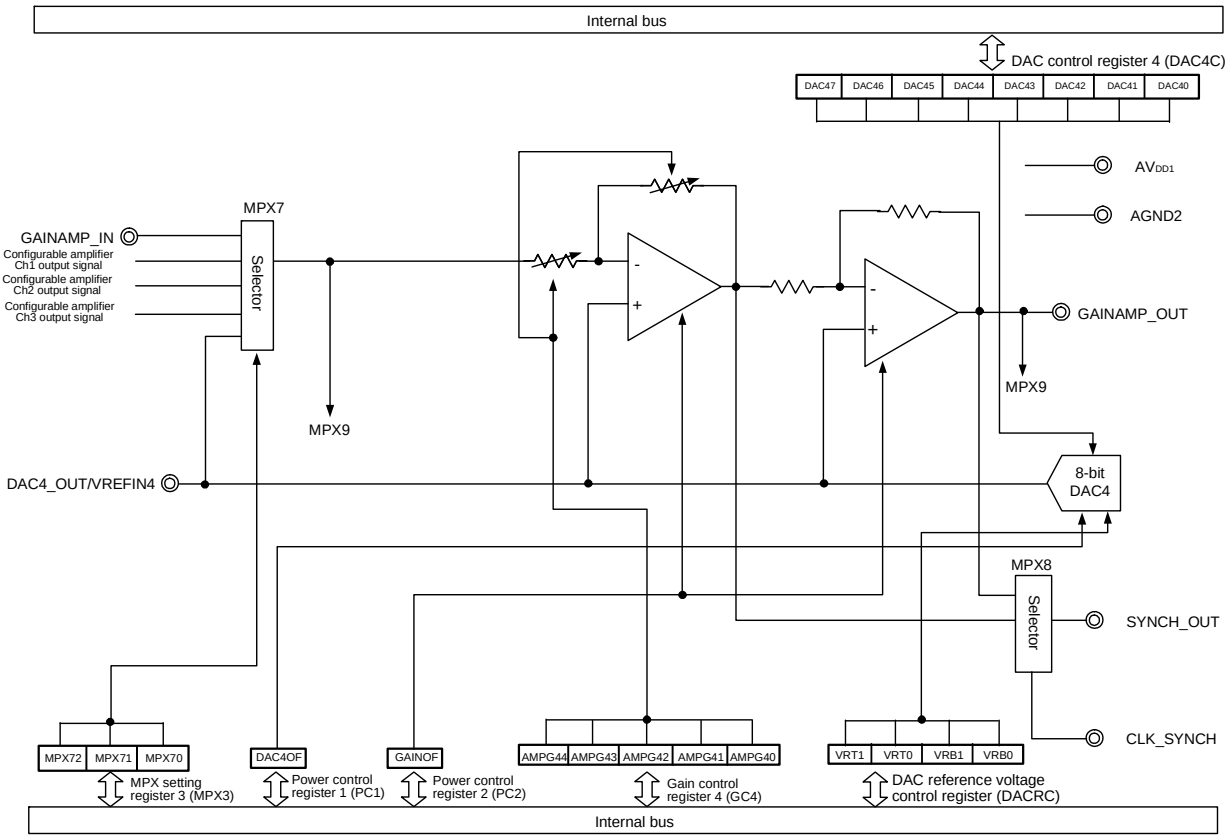


Remark *: don't care

Example of procedure for stopping configurable amplifier Ch1 (transimpedance amplifier)



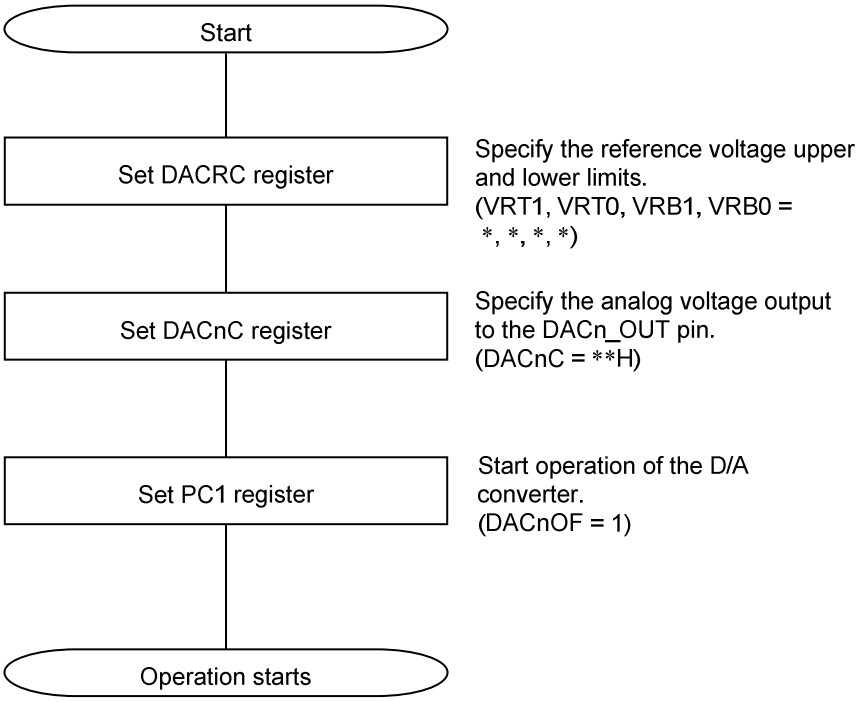
- **80-pin products**



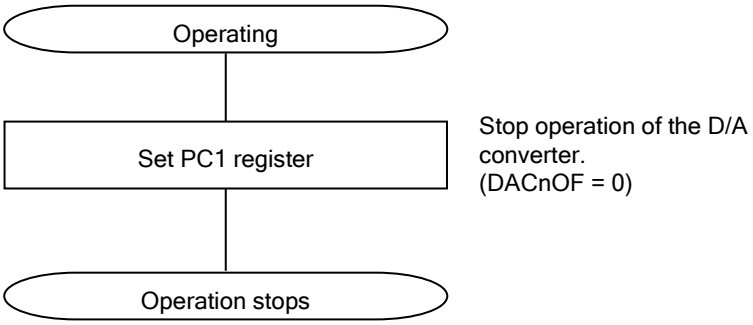
4. 3. 4 Procedure for operating the D/A converters

Follow the procedures below to start and stop the D/A converters.

Example of procedure for starting the D/A converters



Example of procedure for stopping the D/A converters



Remark *: don't care
n = 1 to 4

<R> 4. 4. 3 Registers controlling the low-pass filter

The low-pass filter is controlled by the following 2 registers:

- MPX setting register 3 (MPX3)
- Power control register 2 (PC2)

(1) MPX setting register 3 (MPX3)

<R> This register is used to control MPX7, MPX9, MPX10, and MPX11.

When selecting the signal to be input to the filter circuits, use bits 5 and 4. When switching the order in which signals are processed by the low-pass and high-pass filters, use bit 3.

Reset signal input clears this register to 00H.

- **64-pin products**

Address: 05H After reset: 00H R/W

	7	6	5	4	3	2	1	0
MPX3	0	0	SCF2	SCF1	0	MPX72	MPX71	MPX70

SCF2	SCF1	Source of input to filter circuits
0	0	–
0	1	MPX7 output signal
1	0	Gain adjustment amplifier output signal
1	1	Setting prohibited

Caution Be sure to clear bit 3 to "0".

<R> **Remark** Bits 7 and 6 are fixed at 0 of read only.

- **80-pin products**

Address: 05H After reset: 00H R/W

	7	6	5	4	3	2	1	0
MPX3	0	0	SCF2	SCF1	SCF0	MPX72	MPX71	MPX70

SCF2	SCF1	Source of input to filter circuits
0	0	SC_IN pin
0	1	MPX7 output signal
1	0	Gain adjustment amplifier output signal
1	1	Setting prohibited

SCF0	Specification of the order of filter signal processing
0	The MPX9 output signal passes the low-pass filter and then is input to the high-pass filter.
1	The MPX9 output signal passes the high-pass filter and then is input to the low-pass filter.

<R> **Remark** Bits 7 and 6 are fixed at 0 of read only.