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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

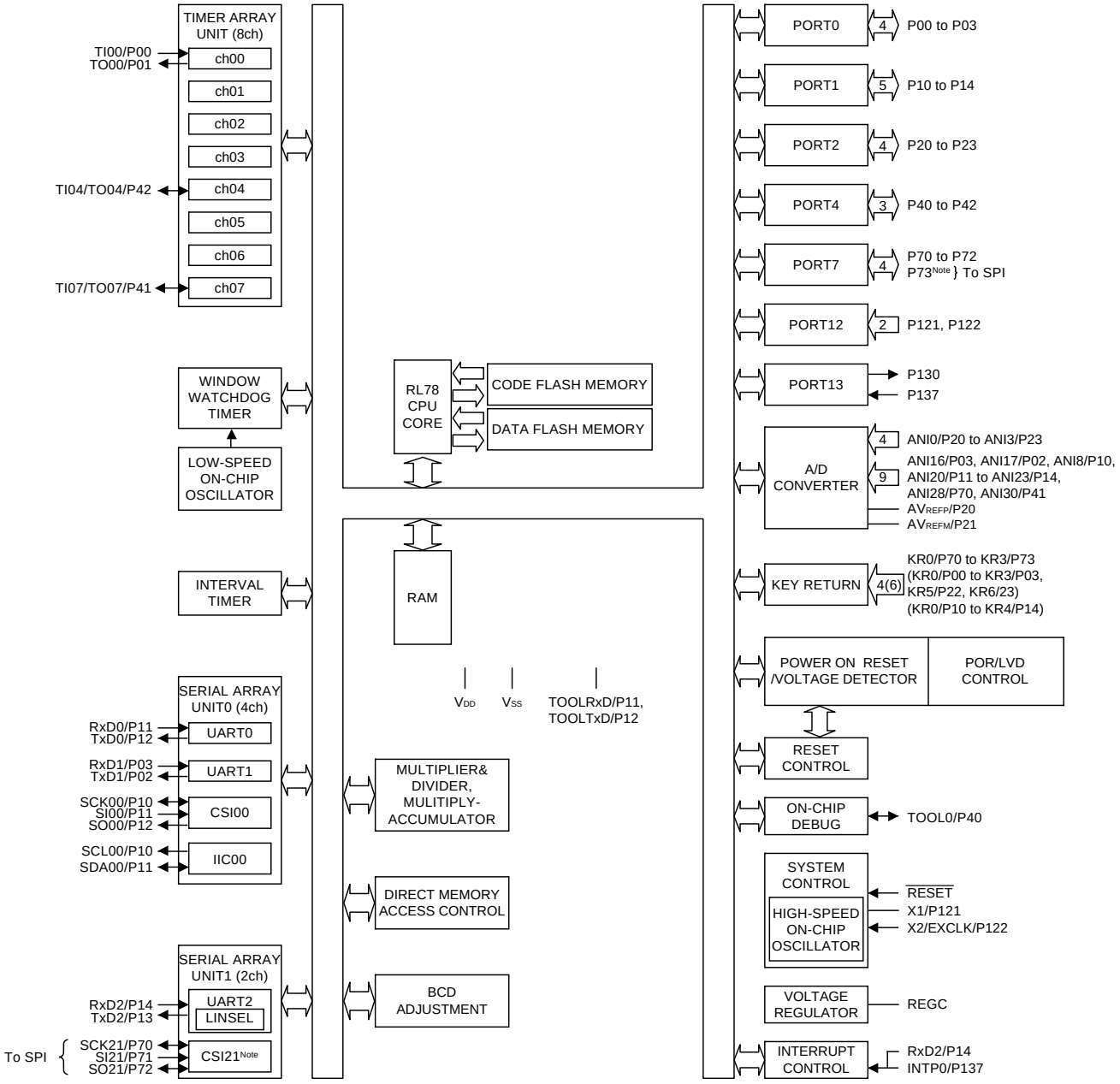
Details	
Product Status	Obsolete
Core Processor	RL78
Core Size	16-Bit
Speed	32MHz
Connectivity	CSI, I²C, LINbus, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	26
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	1.6V ~ 5.5V
Data Converters	A/D 17x8/12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	80-LQFP
Supplier Device Package	80-LFQFP (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f10fmcafb-x0

<R> 1. 4 Pin Identification

○ Microcontroller Block

ANI0-ANI4,	Analog Input	RxD0-RxD2	Receive Data
ANI16-ANI18,		SCK00, SCK10,	Serial Clock Input/Output
ANI20-ANI26,		SCK20, SCK21	
ANI28, ANI30		SCL00, SCL10,	Serial Clock Input/Output
AV_{REFM}	Analog Reference Voltage	SCL20	
	Minus	SDA00, SDA10,	Serial Data Input/Output
AV_{REFP}	Analog Reference Voltage	SDA20	
	Plus	SI00, SI10,	Serial Data Input
EXCLK	External Clock Input	SI20, SI21	
	(Main System Clock)	SO00, SO10	Serial Data Output
INTP0-INTP2	External Interrupt Input	SO20, SO21	
INTP6		TI00, TI04,	Timer Input
KR0-KR7	Key Return	TI07	
P00-P04	Port 0	TO00, TO04,	Timer Output
P10-P15	Port 1	TO07	
P20-P24	Port 2	TOOL0	Data Input/Output for Tool
P40-P42	Port 4	TOOLRxD,	Data Input/Output for External
P50, P51	Port 5		Device
P70-P73	Port 7	TOOLTxD	
P121, P122	Port 12	TxD0-TxD2	Transmit Data
P130, P137	Port 13	V_{DD}	Power Supply
P140	Port 14	V_{SS}	Ground
PCLBUZ0	Programmable Clock Output/	X1, X2	Crystal Oscillator
	Buzzer Output		(Main System Clock)
REGC	Regulator Capacitance	AV_{DD}	Analog Power Supply
$\overline{\text{RESET}}$	Reset	AV_{SS}	Analog Ground

<R> **(1) Block diagram in microcontroller block (64-pin products)**



Note Connected inside the package.

(2/3)

<R>

Function Name	RL78/G1E (64-pin)	RL78/G1E (80-pin)	RL78/G1A (64-pin)
KR0	√	√	√
KR1	√	√	√
KR2	√	√	√
KR3	√	√	√
KR4	(√)	(√)	√
KR5	(√)	(√)	√
KR6	(√)	(√)	√
KR7	–	(√)	√
KR8	–	–	√
KR9	–	–	√
PCLBUZ0	–	√	√
PCLBUZ1	–	–	√
REGC	√	√	√
RTC1HZ	–	–	√
$\overline{\text{RESET}}$	√	√	√
RXD0	√	√	√
RXD1	√	√	√
RXD2	√	√	√
SCK00	√	√	√
SCK01	–	–	√
SCK10	–	√	√
SCK11	–	–	√
SCK20	–	√	√
SCK21	√	√	√
SCLA0	–	–	√
SCL00	√	√	√
SCL01	–	–	√
SCL10	–	√	√
SCL11	–	–	√
SCL20	–	√	√
SCL21	–	–	√
SDAA0	–	–	√
SDA00	√	√	√
SDA01	–	–	√
SDA10	–	√	√
SDA11	–	–	√
SDA20	–	√	√
SDA21	–	–	√
SI00	√	√	√
SI01	–	–	√
SI10	–	√	√
SI11	–	–	√
SI20	–	√	√
SI21	√	√	√

<R> **Remark** Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR).

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Item		RL78/G1E		RL78/G1A (64-pin products)	Remarks
		64-pin products	80-pin products		
Low-speed on-chip oscillator		15 kHz (TYP.): V_{DD} = 1.6 to 5.5 V		15 kHz (TYP.): V_{DD} = 1.6 to 3.6 V	Some differences. See the section 3. 5 about details. Subsystem clock is not available for RL78/G1E.
Minimum instruction execution time		0.03125 μs (High-speed on-chip oscillator: f_{IH} = 32 MHz operation)		0.03125 μs (High-speed on-chip oscillator: f_{IH} = 32 MHz operation)	
		0.05 μs (High-speed system clock: f_{MX} = 20 MHz operation)		0.05 μs (High-speed system clock: f_{MX} = 20 MHz operation)	
		–		30.5 μs (Subsystem clock: f_{SUB} = 32.768 kHz operation)	
Timer	16-bit timer	8 channels		8 channels	Some differences. See the section 3. 6 about details.
	Watchdog Timer	1 channel		1 channel	See the section 3. 10 about details.
	Real-time clock (RTC)	–		1 channel	RTC is not provided in RL78/G1E. (See 3. 7)
	12-bit Interval timer (IT)	1 channel		1 channel	See the section 3. 8 about details.
	Timer output	3 channels (PWM outputs: 2 Note)		7 channels (PWM outputs: 6 Note)	See the section 3. 6 about details.
	RTC output	–		1 channel • 1 Hz (subsystem clock: f_{SUB} = 32.768 kHz)	RTC is not provided in RL78/G1E. (See 3. 7)

Note The number of PWM outputs varies depending on the setting of channels in use.

3. 3. 2. 5 Expanded special function registers (2nd SFRs)

The differences in expanded special function registers (2nd SFRs) between RL78/G1E (64-pin products, 80-pin products) and RL78/G1A (64-pin products) are shown in the tables below.

(1) 64-pin products

Table 3-3. List of Differences in Expanded Special Function Registers (2nd SFRs) (1/6)

Address	RL78/G1E (64-pin products)		RL78/G1A (64-pin products)	
	2nd SFRs Name	Symbol	2nd SFRs Name	Symbol
F0010H	Same as RL78/G1A (64-pin products)	ADM2	A/D converter mode register 2	ADM2
F0011H	Same as RL78/G1A (64-pin products)	ADUL	Conversion result comparison upper limit setting register	ADUL
F0012H	Same as RL78/G1A (64-pin products)	ADLL	Conversion result comparison lower limit setting register	ADLL
F0013H	Same as RL78/G1A (64-pin products)	ADTES	A/D test register	ADTES
F0030H	Pull-up resistor option register 0 Note	PU0	Pull-up resistor option register 0	PU0
F0031H	Pull-up resistor option register 1 Note	PU1	Pull-up resistor option register 1	PU1
F0033H			Pull-up resistor option register 3	PU3
F0034H	Pull-up resistor option register 4 Note	PU4	Pull-up resistor option register 4	PU4
F0035H			Pull-up resistor option register 5	PU5
F0037H	Pull-up resistor option register 7 Note	PU7	Pull-up resistor option register 7	PU7
F003CH			Pull-up resistor option register 12	PU12
F003EH			Pull-up resistor option register 14	PU14
F0040H	Port input mode register 0 Note	PIM0	Port input mode register 0	PIM0
F0041H	Port input mode register 1 Note	PIM1	Port input mode register 1	PIM1
F0050H	Port output mode register 0 Note	POM0	Port output mode register 0	POM0
F0051H	Port output mode register 1 Note	POM1	Port output mode register 1	POM1
F0055H			Port output mode register 5	POM5
F0057H			Port output mode register 7	POM7
F0060H	Same as RL78/G1A (64-pin products)	PMC0	Port mode control register 0	PMC0
F0061H	Port mode control register 1 Note	PMC1	Port mode control register 1	PMC1
F0063H			Port mode control register 3	PMC3
F0064H	Same as RL78/G1A (64-pin products)	PMC4	Port mode control register 4	PMC4
F0065H			Port mode control register 5	PMC5
F0067H	Same as RL78/G1A (64-pin products)	PMC7	Port mode control register 7	PMC7
F006CH			Port mode control register 12	PMC12
F0070H	Same as RL78/G1A (64-pin products)	NFEN0	Noise filter enable register 0	NFEN0
F0071H	Noise filter enable register 1 Note	NFEN1	Noise filter enable register 1	NFEN1

Note The bit setting is different from that of RL78/G1A (64-pin products).

Caution Do not write data to the registers which is in the row with painted gray.

Table 3-4. List of Differences in Expanded Special Function Registers (2nd SFRs) (4/6)

Address	RL78/G1E (80-pin products)			RL78/G1A (64-pin products)		
	2nd SFRs Name	Symbol		2nd SFRs Name	Symbol	
F0148H	Same as RL78/G1A (64-pin products)	SIR10L	SIR10	Serial flag clear trigger register 10	SIR10L	SIR10
F0149H		—			—	
F014AH	Same as RL78/G1A (64-pin products)	SIR11L	SIR11	Serial flag clear trigger register 11	SIR11L	SIR11
F014BH		—			—	
F0150H	Same as RL78/G1A (64-pin products)	SMR10		Serial mode register 10	SMR10	
F0151H						
F0152H	Serial mode register 11 Note	SMR11		Serial mode register 11	SMR11	
F0153H						
F0158H	Same as RL78/G1A (64-pin products)	SCR10		Serial communication operation setting register 10	SCR10	
F0159H						
F015AH	Serial communication operation setting register 11 Note	SCR11		Serial communication operation setting register 11	SCR11	
F015BH						
F0160H	Same as RL78/G1A (64-pin products)	SE1L	SE1	Serial channel enable status register 1	SE1L	SE1
F0161H		—			—	
F0162H	Same as RL78/G1A (64-pin products)	SS1L	SS1	Serial channel start register 1	SS1L	SS1
F0163H		—			—	
F0164H	Same as RL78/G1A (64-pin products)	ST1L	ST1	Serial channel stop register 1	ST1L	ST1
F0165H		—			—	
F0166H	Same as RL78/G1A (64-pin products)	SPS1L	SPS1	Serial clock select register 1	SPS1L	SPS1
F0167H		—			—	
F0168H	Same as RL78/G1A (64-pin products)	SO1		Serial output register 1	SO1	
F0169H						
F016AH	Same as RL78/G1A (64-pin products)	SOE1L	SOE1	Serial output enable register 1	SOE1L	SOE1
F016BH		—			—	
F0174H	Same as RL78/G1A (64-pin products)	SOL1L	SOL1	Serial output level register 1	SOL1L	SOL1
F0175H		—			—	

Note The bit setting is different from that of RL78/G1A (64-pin products).

Table 3-4. List of Differences in Expanded Special Function Registers (2nd SFRs) (5/6)

Address	RL78/G1E (80-pin products)			RL78/G1A (64-pin products)		
	2nd SFRs Name	Symbol		2nd SFRs Name	Symbol	
F0180H	Same as RL78/G1A (64-pin products)	TCR00		Timer counter register 00	TCR00	
F0181H						
F0182H	Same as RL78/G1A (64-pin products)	TCR01		Timer counter register 01	TCR01	
F0183H						
F0184H	Same as RL78/G1A (64-pin products)	TCR02		Timer counter register 02	TCR02	
F0185H						
F0186H	Same as RL78/G1A (64-pin products)	TCR03		Timer counter register 03	TCR03	
F0187H						
F0188H	Same as RL78/G1A (64-pin products)	TCR04		Timer counter register 04	TCR04	
F0189H						
F018AH	Same as RL78/G1A (64-pin products)	TCR05		Timer counter register 05	TCR05	
F018BH						
F018CH	Same as RL78/G1A (64-pin products)	TCR06		Timer counter register 06	TCR06	
F018DH						
F018EH	Same as RL78/G1A (64-pin products)	TCR07		Timer counter register 07	TCR07	
F018FH						
F0190H	Same as RL78/G1A (64-pin products)	TMR00		Timer mode register 00	TMR00	
F0191H						
F0192H	Timer mode register 01 Note	TMR01		Timer mode register 01	TMR01	
F0193H						
F0194H	Timer mode register 02 Note	TMR02		Timer mode register 02	TMR02	
F0195H						
F0196H	Timer mode register 03 Note	TMR03		Timer mode register 03	TMR03	
F0197H						
F0198H	Same as RL78/G1A (64-pin products)	TMR04		Timer mode register 04	TMR04	
F0199H						
F019AH	Timer mode register 05 Note	TMR05		Timer mode register 05	TMR05	
F019BH						
F019CH	Timer mode register 06 Note	TMR06		Timer mode register 06	TMR06	
F019DH						
F019EH	Same as RL78/G1A (64-pin products)	TMR07		Timer mode register 07	TMR07	
F019FH						
F01A0H	Same as RL78/G1A (64-pin products)	TSR00L	TSR00	Timer status register 00	TSR00L	TSR00
F01A1H		—			—	
F01A2H	Same as RL78/G1A (64-pin products)	TSR01L	TSR01	Timer status register 01	TSR01L	TSR01
F01A3H		—			—	
F01A4H	Same as RL78/G1A (64-pin products)	TSR02L	TSR02	Timer status register 02	TSR02L	TSR02
F01A5H		—			—	
F01A6H	Same as RL78/G1A (64-pin products)	TSR03L	TSR03	Timer status register 03	TSR03L	TSR03
F01A7H		—			—	
F01A8H	Same as RL78/G1A (64-pin products)	TSR04L	TSR04	Timer status register 04	TSR04L	TSR04
F01A9H		—			—	
F01AAH	Same as RL78/G1A (64-pin products)	TSR05L	TSR05	Timer status register 05	TSR05L	TSR05
F01ABH		—			—	
F01ACH	Same as RL78/G1A (64-pin products)	TSR06L	TSR06	Timer status register 06	TSR06L	TSR06
F01ADH		—			—	
F01AEH	Same as RL78/G1A (64-pin products)	TSR07L	TSR07	Timer status register 07	TSR07L	TSR07
F01AFH		—			—	

Note The bit setting is different from that of RL78/G1A (64-pin products).

3. 4. 2. 1 Port 0

Port 0 is an I/O port with an output latch. Port 0 can be set to the input mode or output mode in 1-bit units using port mode register 0 (PM0). When the P00 to P04 pins are used as an input port, use of an on-chip pull-up resistor can be specified in 1-bit units by pull-up resistor option register 0 (PU0). Input to the P00, P01, P03 and P04 pins can be specified through a normal input buffer or a TTL input buffer in 1-bit units using port input mode register 0 (PIM0). Output from the P02 to P04 pins can be specified as normal CMOS output or N-ch open-drain output (V_{DD} tolerance) in
<R> 1-bit units using port output mode register 0 (POM0). The P02 and P03 pins can be specified as digital input/output or analog input in 1-bit units, using port mode control register 0 (PMC0). This port can be also used for timer I/O, A/D converter analog input, serial interface data I/O, clock I/O, and key interrupt input.

When reset signal is generated, the following configuration will be set.

- P00, P01 and P04 pins ⋯ Input mode
- P02 and P03 pins ⋯ Analog input

3. 4. 2. 2 Port 1

Port 1 is an I/O port with an output latch. Port 1 can be set to the input mode or output mode in 1-bit units using port mode register 1 (PM1). When the P10 to P15 pins are used as an input port, use of an on-chip pull-up resistor can be specified in 1-bit units by pull-up resistor option register 1 (PU1). Input to the P10, P11, P14 to P15 pins can be specified through a normal input buffer or a TTL input buffer in 1-bit units using port input mode register 1 (PIM1). Output from the P10 to P15 pins can be specified as normal CMOS output or N-ch open-drain output (V_{DD} tolerance) in
<R> 1-bit units using port output mode register 1 (POM1). The P10 to P15 pins can be specified as digital input/output or analog input in 1-bit units, using port mode control register 1 (PMC1). This port can be also used for A/D converter analog input, serial interface data I/O, programming UART I/O, and key return input.

When reset signal is generated, the P10 to P15 pins will be set to analog input.

3. 4. 2. 3 Port 2

Port 2 is an I/O port with an output latch. Port 2 can be set to the input mode or output mode in 1-bit units using port mode register 2 (PM2). This port can be also used for A/D converter analog input and reference voltage input, and key return input pin. Setting digital or analog to each pin can be done in A/D port configuration register (ADPC).

When reset signal is generated, the P20/ANI0 to P24/ANI4 pins will be set to analog input.

3. 4. 3. 5 Port output mode register (POMxx)

(1) 64-pin products

Symbol	7	6	5	4	3	2	1	0	Address	After Reset	R/W
POM0	0	0	0	0	POM03	POM02	0	0	F0050H	00H	R/W
POM1	0	0	0	POM14	POM13	POM12	POM11	POM10	F0051H	00H	R/W

<R> **Caution Be sure to clear bits 0, 1 and 4 to 7 of the POM0 register, and bits 5 to 7 of the POM1 register to "0".**

<R> **(2) 80-pin products**

Symbol	7	6	5	4	3	2	1	0	Address	After Reset	R/W
POM0	0	0	0	POM04	POM03	POM02	0	0	F0050H	00H	R/W
POM1	0	0	POM15	POM14	POM13	POM12	POM11	POM10	F0051H	00H	R/W
POM5	0	0	0	0	0	0	0	POM50	F0055H	00H	R/W

Caution Be sure to clear bits 0, 1 and 5 to 7 of the POM0 register, bits 6 and 7 of the POM1 register, and bits 1 to 7 of the POM5 register to "0".

3. 4. 3. 6 Port mode control register (PMCxx)

<R> **(1) 64-pin products**

Symbol	7	6	5	4	3	2	1	0	Address	After Reset	R/W
PMC0	1	1	1	1	PMC03	PMC02	1	1	F0060H	FFH	R/W
PMC1	1	1	1	PMC14	PMC13	PMC12	PMC11	PMC10	F0061H	FFH	R/W
PMC4	1	1	1	1	1	1	PMC41	1	F0064H	FFH	R/W
PMC7	1	1	1	1	1	1	1	PMC70	F0067H	FFH	R/W

Caution Be sure to set bits 0, 1 and 4 to 7 of the PMC0 register, bits 5 to 7 of the PMC1 register, bits 0 and 2 to 7 of the PMC4 register, and bits 1 to 7 of the PMC7 register to "0".

<R> **(2) 80-pin products**

Symbol	7	6	5	4	3	2	1	0	Address	After Reset	R/W
PMC0	1	1	1	1	PMC03	PMC02	1	1	F0060H	FFH	R/W
PMC1	1	1	PMC15	PMC14	PMC13	PMC12	PMC11	PMC10	F0061H	FFH	R/W
PMC4	1	1	1	1	1	1	PMC41	1	F0064H	FFH	R/W
PMC5	1	1	1	1	1	1	PMC51	PMC50	F0065H	FFH	R/W
PMC7	1	1	1	1	1	1	1	PMC70	F0067H	FFH	R/W

Caution Be sure to set bits 0, 1 and 4 to 7 of the PMC0 register, bits 6 and 7 of the PMC1 register, bits 0 and 2 to 7 of the PMC4 register, bits 2 to 7 of the PMC5 register, and bits 1 to 7 of the PMC7 register to "0".

3. 5. 2 Configuration of clock generator

The clock generator includes the following hardware.

Table 3-6. Configuration of Clock Generator

Item	Configuration
Control registers	Clock operation mode control register (CMC) System clock control register (CKC) Clock operation status control register (CSC) Oscillation stabilization time counter status register (OSTC) Oscillation stabilization time select register (OSTS) Peripheral enable register 0 (PER0) <R> Subsystem clock supply mode control register (OSMC) High-speed on-chip oscillator frequency select register (HOCODIV) High-speed on-chip oscillator trimming register (HIOTRM)
Oscillators	X1 oscillator High-speed on-chip oscillator Low-speed on-chip oscillator

3. 11. 3. 4 A/D converter mode register 2 (ADM2)

The bit setting is same as that of RL78/G1A (64-pin products). For details, see **11. 3. 4 A/D converter mode register 2 (ADM2)** in **RL78/G1A Hardware User's Manual (R01UH0305E)**.

3. 11. 3. 5 12-bit A/D conversion result register (ADCR)

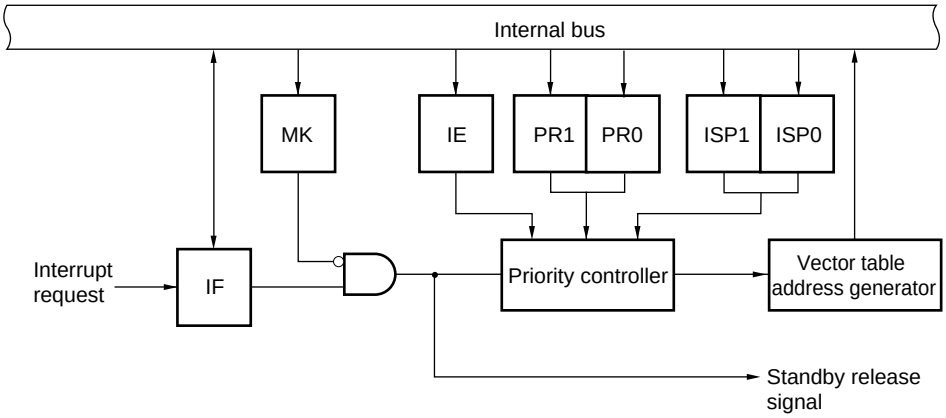
The bit setting is same as that of RL78/G1A (64-pin products). For details, see **11. 3. 5 12-bit A/D conversion result register (ADCR)** in **RL78/G1A Hardware User's Manual (R01UH0305E)**.

3. 11. 3. 6 8-bit A/D conversion result register (ADCRH)

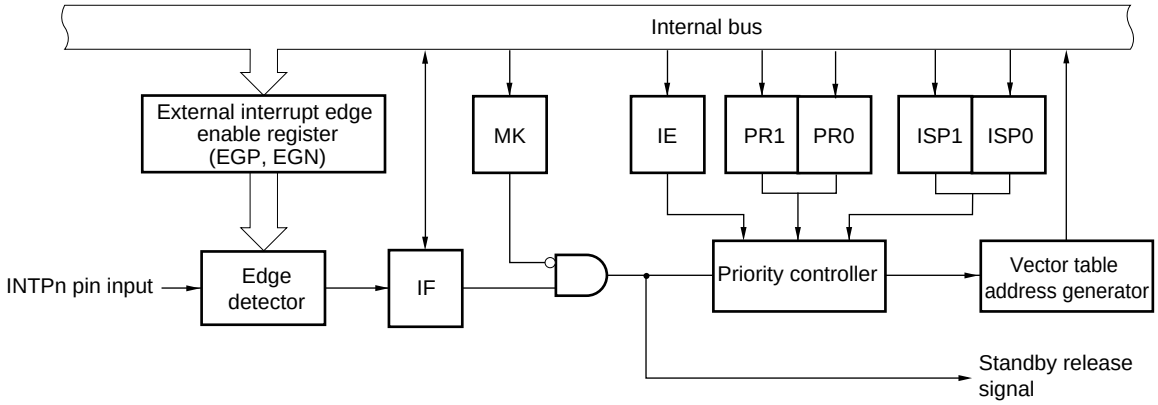
The bit setting is same as that of RL78/G1A (64-pin products). For details, see **11. 3. 6 8-bit A/D conversion result register (ADCRH)** in **RL78/G1A Hardware User's Manual (R01UH0305E)**.

Figure 3-13. Basic Configuration of Interrupt Function (1/2)

(a) Internal maskable interrupt



(b) External maskable interrupt (INTPn)



IF: Interrupt request flag
IE: Interrupt enable flag
ISP0: In-service priority flag 0
ISP1: In-service priority flag 1
MK: Interrupt mask flag
PR0: Priority specification flag 0
PR1: Priority specification flag 1

Remark 64-pin products: n = 0
80-pin products: n = 0 to 3, 6

3. 17. 3 Register controlling key interrupt

The bit settings which are different from that of RL78/G1A (64-pin products) are shown below. For details of each register, see **17. 3 Register Controlling Key Interrupt** in **RL78/G1A Hardware User's Manual (R01UH0305E)**.

3. 17. 3. 1 Key return control register (KRCTL)

The bit setting is same as that of RL78/G1A (64-pin products). For details, see **17. 3. 1 Key return control register (KRCTL)** in **RL78/G1A Hardware User's Manual (R01UH0305E)**.

3. 17. 3. 2 Key return mode register 0 (KRM0)

(1) 64-pin products

Address: FFF37H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
KRM0	0	KRM06	KRM05	KRM04	KRM03	KRM02	KRM01	KRM00

Caution Be sure to clear bit 7 of the KRM0 register to "0".

<R> (2) 80-pin products

Address: FFF37H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
KRM0	KRM07	KRM06	KRM05	KRM04	KRM03	KRM02	KRM01	KRM00

3. 17. 3. 3 Key return flag register (KRF)

The bit setting is same as that of RL78/G1A (64-pin products). For details, see **17. 3. 3 Key return flag register (KRF)** in **RL78/G1A Hardware User's Manual (R01UH0305E)**.

3. 24 Option Byte

3. 24. 1 Functions of option bytes

Addresses 000C0H to 000C3H of the flash memory of the RL78/G1E form an option byte area.

Option bytes consist of user option byte (000C0H to 000C2H) and on-chip debug option byte (000C3H).

Upon power application or resetting and starting, an option byte is automatically referenced and a specified function is set. For the bits to which no function is allocated, be sure to set the value specified in this manual.

To use the boot swap operation during self programming, 000C0H to 000C3H are replaced by 010C0H to 010C3H. Therefore, set the same values as 000C0H to 000C3H to 010C0H to 010C3H.

Caution Be sure to specify option byte settings regardless of whether they are used or not.

3. 24. 1. 1 User option byte (000C0H to 000C2H/010C0H to 010C2H)

<R> **(1) 000C0H/010C0H**

- ○ Setting of watchdog timer operation
  - Enabling or disabling of counter operation
  - Enabling or disabling of counter operation in the HALT or STOP mode
- ○ Setting of overflow time of watchdog timer
- ○ Setting of window open period of watchdog timer
- ○ Setting of interval interrupt of watchdog timer
  - Whether or not to use the interval interrupt is selectable

Caution Set the same value as 000C0H to 010C0H when the boot swap operation is used because 000C0H is replaced by 010C0H.

<R> **(2) 000C1H/010C1H**

- ○ Setting of LVD operation mode
  - Interrupt & reset mode.
  - Reset mode.
  - Interrupt mode.
  - LVD off (by controlling the externally input reset signal on the $\overline{\text{RESET}}$ pin)
- ○ Setting of LVD detection level (V_{LVDH}, V_{LVDL}, V_{LVD})

<R> **Cautions1. After power is supplied, the reset state must be retained until the operating voltage becomes in the range defined in 5. 2. 3 AC characteristics. This is done by utilizing the voltage detection circuit or controlling the externally input reset signal. After the power supply is turned off, this LSI should be placed in the STOP mode, or placed in the reset state by utilizing the voltage detection circuit or controlling the externally input reset signal, before the voltage falls below the operating range. The range of operating voltage varies with the setting of the user option byte (000C2H or 010C2H).**

2. Set the same value as 000C1H to 010C1H when the boot swap operation is used because 000C1H is replaced by 010C1H.

<R> **Table 3-18. Wiring Between RL78/G1E and Dedicated Flash Memory Programmer**

Pin Configuration of Dedicated Flash Memory Programmer				Pin Name	Pin No.	
Signal Name		I/O	Pin Function		64-pin products	80-pin products
PG-FP5 FL-PR5	E1 On-chip Debugging Emulator				WQFN (9 × 9)	LQFP (12 × 12)
–	TOOL0	I/O	Transmit/receive signal	TOOL0/P40	15	18
SI / RxD	–	I/O				
–	$\overline{\text{RESET}}$	Output	Reset signal	$\overline{\text{RESET}}$	16	19
/RESET	–	Output				
V_{DD}		I/O	V_{DD} voltage generation/ power monitoring	V_{DD}	22	25
GND		–	Ground	V_{SS}	21	24
				EV_{SS0}	–	–
				REGC Note	20	23
EMV_{DD}		–	Driving power for TOOL0 pin	V_{DD}	22	25
				EV_{DD0}	–	–

<R> **Note** Connect REGC pin to ground via a capacitor (0.47 to 1 μF).

Remark Pins that are not indicated in the above table can be left open when using the flash memory programmer for flash programming.

3. 25. 1. 1 Programming environment

See **25. 1. 1 Programming environment** in **RL78/G1A Hardware User's Manual (R01UH0305E)**.

3. 25. 1. 2 Communication mode

See **25. 1. 2 Communication mode** in **RL78/G1A Hardware User's Manual (R01UH0305E)**.

- 80-pin products

Address: 04H After reset: 00H R/W

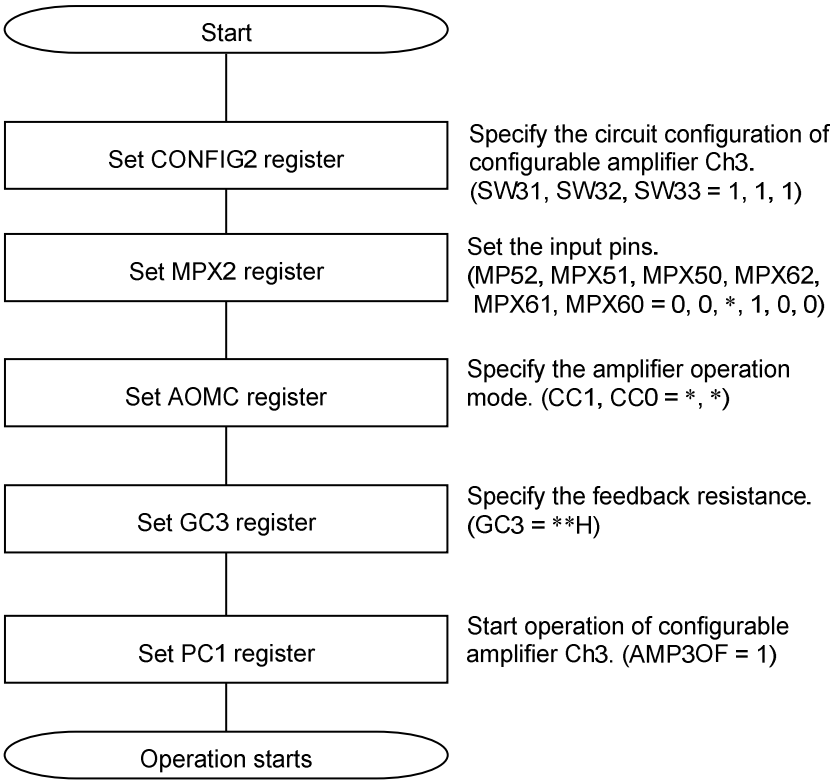
	7	6	5	4	3	2	1	0
MPX2	0	MPX52	MPX51	MPX50	0	MPX62	MPX61	MPX60

MPX52	MPX51	MPX50	Source of configurable amplifier Ch3 inverse input
0	0	0	MPXIN50 pin
0	0	1	MPXIN51 pin
0	1	0	Configurable amplifier Ch1 output signal
0	1	1	Configurable amplifier Ch2 output signal
1	0	0	D/A converter Ch3 output signal or VREFIN3 pin
Other than above			Setting prohibited

MPX62	MPX61	MPX60	Source of configurable amplifier Ch3 non-inverted input
0	0	0	MPXIN60 pin
0	0	1	MPXIN61 pin
0	1	0	Configurable amplifier Ch1 output signal
0	1	1	Configurable amplifier Ch2 output signal
1	0	0	D/A converter Ch3 output signal or VREFIN3 pin
Other than above			Setting prohibited

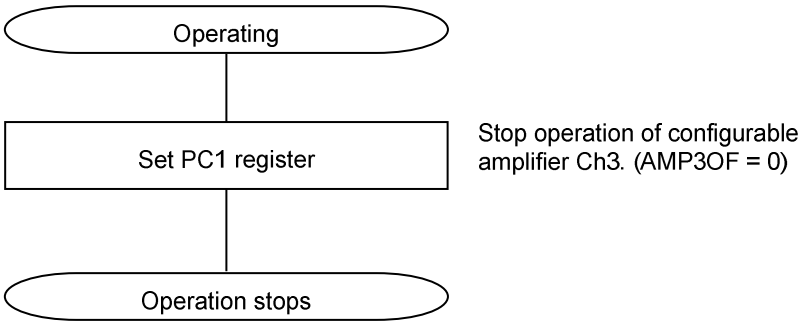
Remark Bits 7 and 3 can be set to 1, but this has no effect on the function.

Example of procedure for starting configurable amplifier Ch3 (transimpedance amplifier)



Remark *: don't care

Example of procedure for stopping configurable amplifier Ch3 (transimpedance amplifier)



5. 2. 3 AC characteristics

(T_A = –40 to +85°C, 1.6 V ≤ AV_{DD} ≤ 3.6 V, 1.6 V ≤ V_{DD} ≤ 5.5 V, AV_{DD} ≤ V_{DD}, V_{SS} = 0 V)

Parameter	Symbol	Conditions			MIN.	TYP.	MAX.	Unit
Instruction cycle (minimum instruction execution time)	T_{CY}	Main system clock (f_{MAIN}) operation	HS (high-speed main) mode	2.7 V ≤ V_{DD} ≤ 5.5 V	0.03125		1	μs
				2.4 V ≤ V_{DD} < 2.7 V	0.0625		1	μs
			LV (Low-voltage main) mode	1.6 V ≤ V_{DD} ≤ 5.5 V	0.25		1	μs
			LS (Low-speed main) mode	1.8 V ≤ V_{DD} ≤ 5.5 V	0.125		1	μs
		In the self programming mode	HS (high-speed main) mode	2.7 V ≤ V_{DD} ≤ 5.5 V	0.03125		1	μs
				2.4 V ≤ V_{DD} < 2.7 V	0.0625		1	μs
			LV (Low-voltage main) mode	1.8 V ≤ V_{DD} ≤ 5.5 V	0.25		1	μs
			LS (Low-speed main) mode	1.8 V ≤ V_{DD} ≤ 5.5 V	0.125		1	μs
External main system clock frequency	f_{EX}	2.7 V ≤ V_{DD} ≤ 5.5 V			1.0		20.0	MHz
		2.4 V ≤ V_{DD} < 2.7 V			1.0		16.0	
		1.8 V ≤ V_{DD} < 2.4 V			1.0		8.0	
		1.6 V ≤ V_{DD} < 1.8 V			1.0		4.0	
External main system clock input high-level width, low-level width	t_{EXH}, t_{EXL}	2.7 V ≤ V_{DD} ≤ 5.5 V			24			ns
		2.4 V ≤ V_{DD} < 2.7 V			30			
		1.8 V ≤ V_{DD} < 2.4 V			60			
		1.6 V ≤ V_{DD} < 1.8 V			120			
TI00, TI04, TI07 input high/low level width	t_{TIH}, t_{TIL}				1/f_{MCK} + 10			ns
TO00, TO04, TO07 output frequency	f_{TO}	HS (high-speed main) mode		4.0 V ≤ V_{DD} ≤ 5.5 V			16	MHz
				2.7 V ≤ V_{DD} < 4.0 V			8	
				1.8 V ≤ V_{DD} < 2.7 V			4	
				1.6 V ≤ V_{DD} < 1.8 V			2	
		LV (Low-voltage main) mode		1.6 V ≤ V_{DD} < 5.5 V			2	
		LS (Low-speed main) mode		1.8 V ≤ V_{DD} ≤ 5.5 V			4	
				1.6 V ≤ V_{DD} < 1.8 V			2	
PCLBUZ0 output frequency	f_{PCL}	HS (high-speed main) mode		4.0 V ≤ V_{DD} ≤ 5.5 V			16	MHz
				2.7 V ≤ V_{DD} < 4.0 V			8	
				1.8 V ≤ V_{DD} < 2.7 V			4	
				1.6 V ≤ V_{DD} < 1.8 V			2	
		LV (Low-voltage main) mode		1.8 V ≤ V_{DD} ≤ 5.5 V			4	
				1.6 V ≤ V_{DD} < 1.8 V			2	
		LS (Low-speed main) mode		1.8 V ≤ V_{DD} ≤ 5.5 V			4	
				1.6 V ≤ V_{DD} < 1.8 V			2	
Interrupt input high level width, low level width	t_{INIH}, t_{INIL}	INTP0, INTP1, INTP2, INTP6		1.6 V ≤ V_{DD} ≤ 5.5 V	1			μs
<R> Key interrupt input high level width, low level width	t_{KR}	KR0 to KR7		1.8 V ≤ V_{DD} ≤ 5.5 V 1.8 V ≤ AV_{DD} ≤ 3.6 V	250			ns
				1.6 V ≤ V_{DD} < 1.8 V 1.6 V ≤ AV_{DD} < 1.8 V	1			μs
$\overline{\text{RESET}}$ low level width	t_{RSL}				10			μs

Remark f_{MCK}: Timer array unit operation clock frequency. (Operation clock to be set by the timer clock select register 0 (TPS0) and CKS0n bit of timer mode register 0n (TMR0n). n: Channel number (n = 0 to 7))

5. 3 Electrical Specifications of Analog Block

<R> 5. 3. 1 Operating conditions of analog block

Parameter	Symbol	Conditions	Ratings			Unit
			MIN	TYP.	MAX.	
Power supply voltage range	V_{DDOP}	AV_{DD1}, AV_{DD2}, AV_{DD3}, DV_{DD}	3.0	–	5.5	V

5. 3. 3. 2 Gain adjustment amplifier characteristics

(1) 64-pin products

(–40°C ≤ T_A ≤ 85°C, AV_{DD1} = AV_{DD2} = AV_{DD3} = DV_{DD} = 5.0 V, VREFIN4 = 1.7 V, GAINOF = 1, DAC4OF = 0)

Parameter	Symbol	Conditions	Ratings			Unit
			MIN	TYP	MAX	
Current consumption	IccA		–	530	1,300	μA
Input voltage	VINL		AGND2 - 0.1	–	–	V
	VINH		–	–	AV_{DD1} - 0.05	V
Output voltage	VOUTL1	IOL = -100 μA	–	AGND2 + 0.02	AGND2 + 0.05	V
	VOUTH1	IOH = 100 μA	AV_{DD1} - 0.05	AV_{DD1} - 0.02	–	V
Gain bandwidth	GBW2	CL = 30 pF, GC4 = 11H (40 dB)	–	0.86	–	MHz
Input conversion offset voltage	VOFF	GC4 = 00H (6 dB), T_A = 25°C, GAINAMP_IN = 2.5 V	-30	–	30	mV
Input conversion offset voltage temperature coefficient	VOTC2	CLK_SYNCH = L, GAINAMP_OUT pin	–	±18	–	μV/°C
Slew rate	SR	CL = 30 pF	–	0.9	–	V/μs
Equivalent input noise	En_Gain	f = 1 kHz, GC4 = 11H (40 dB)	–	700	–	nV/√ Hz
Power supply rejection ratio	PSRR2	f = 1 kHz, GC4 = 00H (6 dB)	–	45	–	dB
Gain setting error	GAIN_Accu1	T_A = 25°C	-0.6	–	0.6	dB
	GAIN_Accu2	T_A = –40 to 85°C	-1.0	–	1.0	dB