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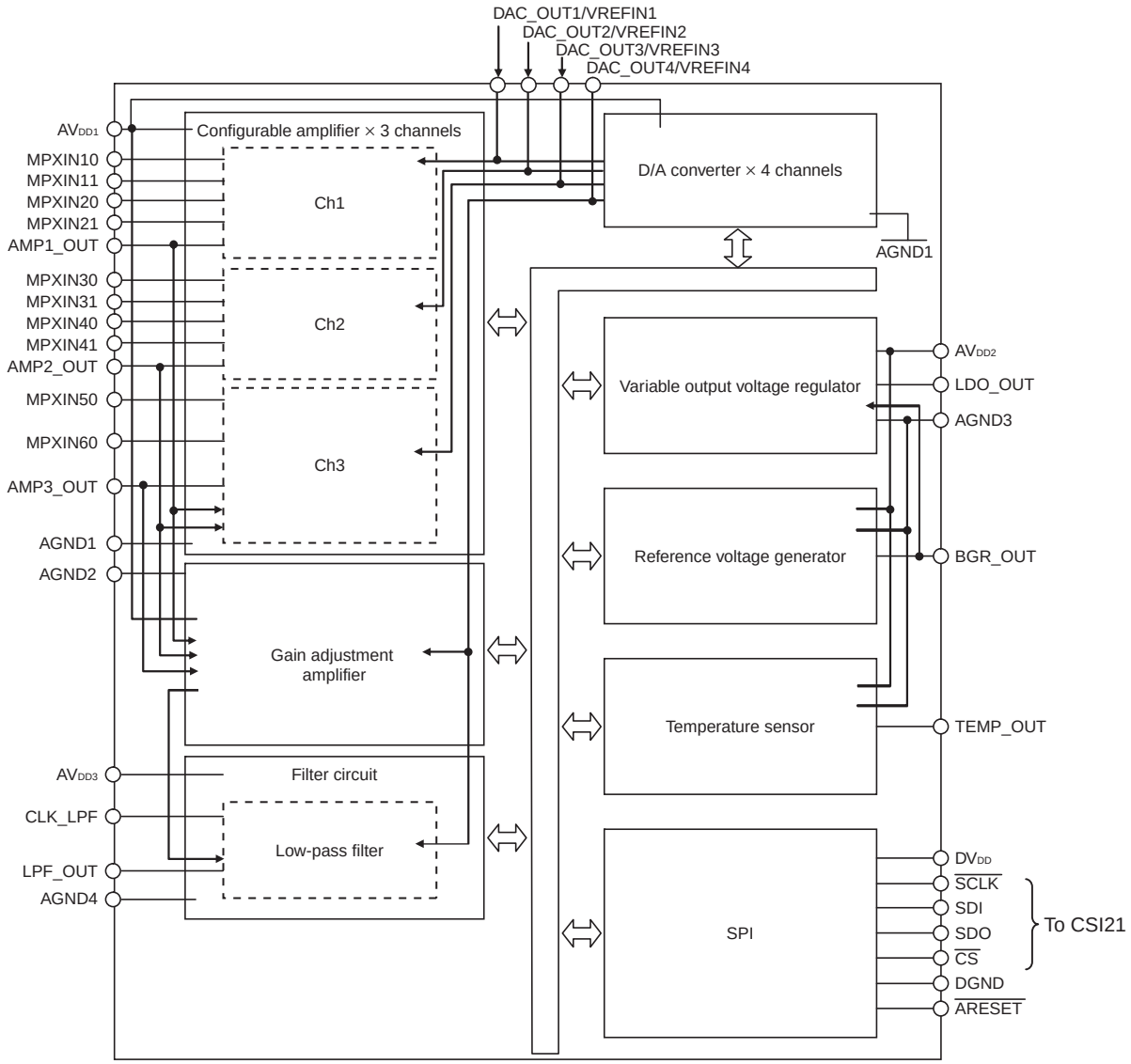
Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	RL78
Core Size	16-Bit
Speed	32MHz
Connectivity	CSI, I²C, LINbus, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	26
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	1.6V ~ 5.5V
Data Converters	A/D 17x8/12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	80-LQFP
Supplier Device Package	80-LFQFP (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f10fmcdfb-v0

(2) Block diagram in analog block (64-pin products)



(2/2)

<R>

RL78/G1E (80-pin products)		RL78/G1A (64-pin products)	
Function Name	Alternate Function	Function Name	Alternate Function
P70	ANI28/SCK21/KR0/$\overline{\text{SCLK}}$ Note	P70	ANI28/SCK21/SCL21/KR0
P71	SI21/KR1/SDO Note	P71	SI21/SDA21/KR1
P72	SO21/KR2/SDI Note	P72	SO21/KR2
P73	KR3/$\overline{\text{CS}}$ Note	P73	SO01/KR3
		P74	SI01/SDA01/INTP8/KR4
		P75	SCK01/SCL01/INTP9/KR5
		P76	INTP10/KR6
		P77	INTP11/KR7
		P120	ANI19
P121	Same as RL78/G1A (64-pin products)	P121	X1
P122	Same as RL78/G1A (64-pin products)	P122	X2/EXCLK
		P123	XT1
		P124	XT2/EXCLKS
P130	Same as RL78/G1A (64-pin products)	P130	–
P137	Same as RL78/G1A (64-pin products)	P137	INTP0
P140	Same as RL78/G1A (64-pin products)	P140	PCLBUZ0/INTP6
		P141	PCLBUZ1/INTP7
		P150	ANI8
		P151	ANI9/(KR6)
		P152	ANI10/(KR7)
		P153	ANI11/(KR8)
		P154	ANI12/(KR9)

Note $\overline{\text{SCLK}}$, SDO, SDI, $\overline{\text{CS}}$ represent the pin functions of analog block. P70 to P73 which are connected to the pins of the chip of analog block inside the package have some alternate functions for analog block.

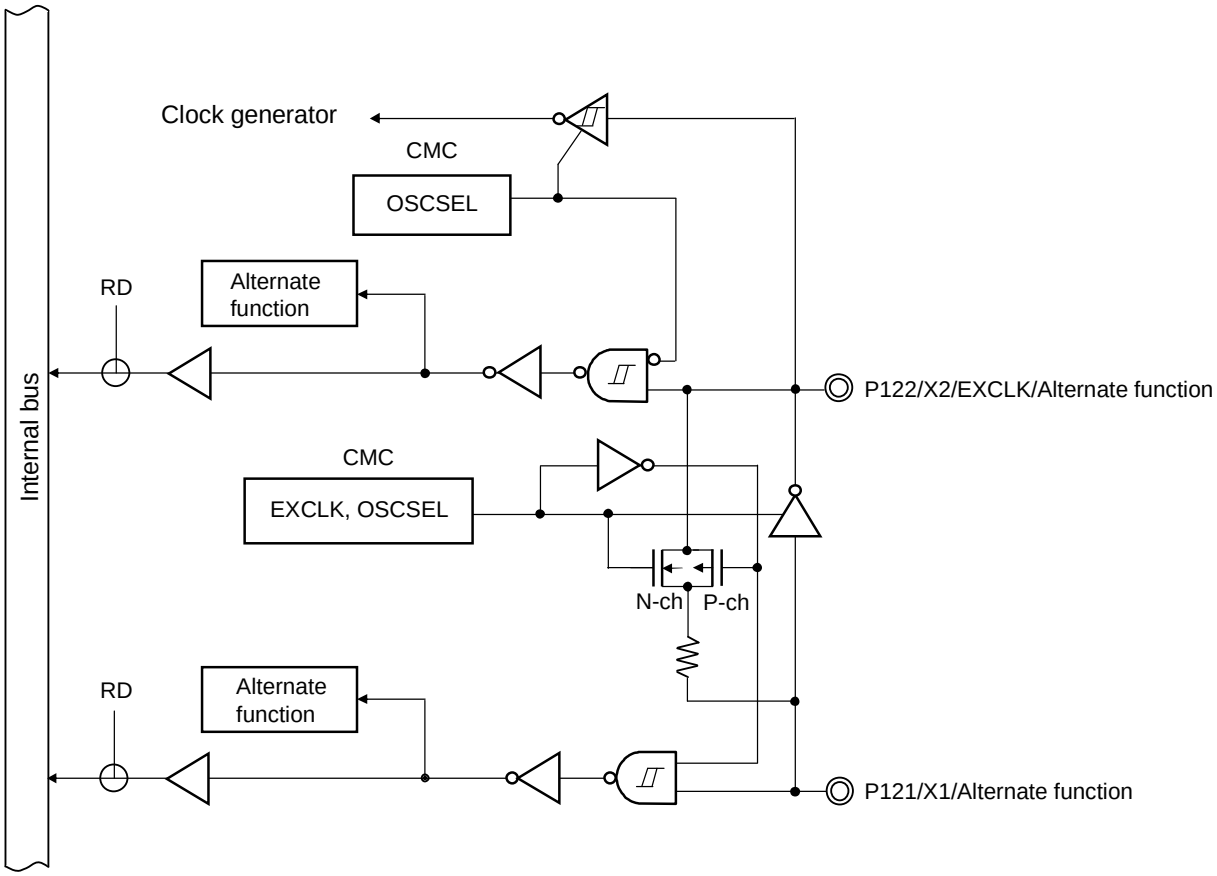
<R> **Remark** Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR). About format, see Figure in **3. 4. 3. 8 Peripheral I/O redirection register (PIOR)**.

(3) Comparison of functions other than port functions (60-pin products and 80-pin products)

About the comparison of functions other than port pins, See **2. 1. 2. 1 Functions available for each product**.

<R>

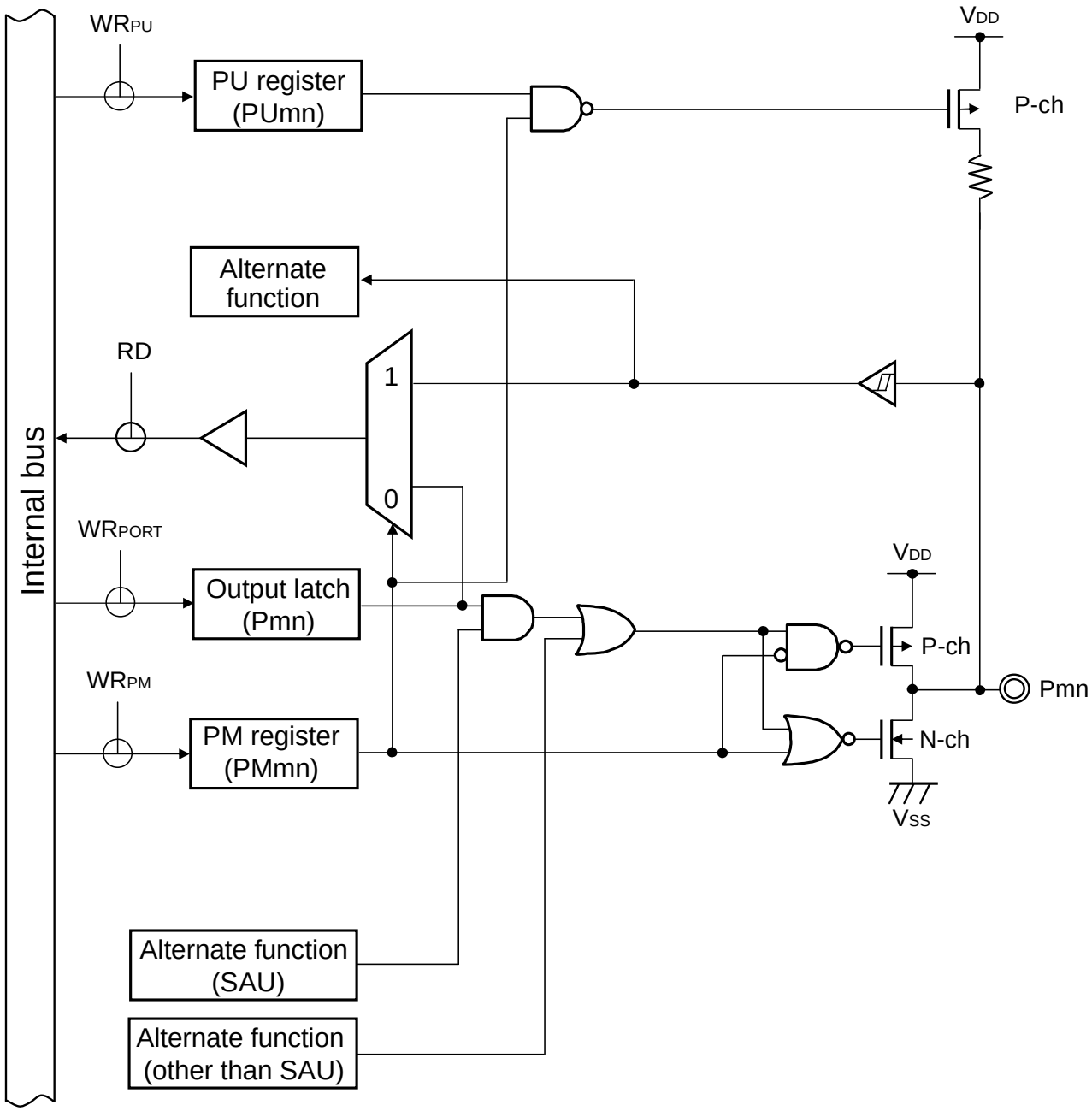
Figure 2-4. Pin Block Diagram for Pin Type 2-2-1



Remark For alternate functions, see **2. 1. 1 Port functions**.

<R>

Figure 2-7. Pin Block Diagram for Pin Type 7-1-2



Remarks 1. For alternate functions, see **2. 1. 1 Port functions**.

2. SAU: Serial array unit

3. 3. 2. 4 Special function registers (SFRs)

The differences in special function registers (SFRs) between RL78/G1E (64-pin products, 80-pin products) and RL78/G1A (64-pin products) are shown in the tables below.

(1) 64-pin products

Table 3-1. List of Differences in Special Function Registers (SFRs) (1/4)

Address	RL78/G1E (64-pin products)			RL78/G1A (64-pin products)		
	SFRs Name	Symbol		SFRs Name	Symbol	
FFF00H	Port register 0 Note	P0		Port register 0	P0	
FFF01H	Port register 1 Note	P1		Port register 1	P1	
FFF02H	Port register 2 Note	P2		Port register 2	P2	
FFF03H				Port register 3	P3	
FFF04H	Port register 4 Note	P4		Port register 4	P4	
FFF05H				Port register 5	P5	
FFF06H				Port register 6	P6	
FFF07H	Port register 7 Note	P7		Port register 7	P7	
FFF0CH	Port register 12 Note	P12		Port register 12	P12	
FFF0DH	Same as RL78/G1A (64-pin products)	P13		Port register 13	P13	
FFF0EH				Port register 14	P14	
FFF0FH				Port register 15	P15	
FFF10H	Same as RL78/G1A (64-pin products)	TXD0/ SIO00	SDR00	Serial data register 00	TXD0/ SIO00	SDR00
FFF11H		—			—	
FFF12H	Same as RL78/G1A (64-pin products)	RXD0/ SIO01	SDR01	Serial data register 01	RXD0/ SIO01	SDR01
FFF13H		—			—	
FFF18H	Same as RL78/G1A (64-pin products)	TDR00		Timer data register 00	TDR00	
FFF19H						
FFF1AH	Same as RL78/G1A (64-pin products)	TDR01L	TDR01	Timer data register 01	TDR01L	TDR01
FFF1BH		TDR01H			TDR01H	
FFF1EH	Same as RL78/G1A (64-pin products)	ADCR		12-bit A/D conversion result register	ADCR	
FFF1FH	Same as RL78/G1A (64-pin)	ADCRH		8-bit A/D conversion result register	ADCRH	
FFF20H	Port mode register 0 Note	PM0		Port mode register 0	PM0	
FFF21H	Port mode register 1 Note	PM1		Port mode register 1	PM1	
FFF22H	Port mode register 2 Note	PM2		Port mode register 2	PM2	
FFF23H				Port mode register 3	PM3	
FFF24H	Port mode register 4 Note	PM4		Port mode register 4	PM4	
FFF25H				Port mode register 5	PM5	
FFF26H	Port mode register 6 Note	PM6		Port mode register 6	PM6	
FFF27H	Port mode register 7 Note	PM7		Port mode register 7	PM7	
FFF2CH				Port mode register 12	PM12	
FFF2EH	Port mode register 14 Note	PM14		Port mode register 14	PM14	
FFF2FH	Port mode register 15 Note	PM15		Port mode register 15	PM15	
FFF30H	Same as RL78/G1A (64-pin products)	ADM0		A/D converter mode register 0	ADM0	
FFF31H	Analog input channel specification register Note	ADS		Analog input channel specification register	ADS	
FFF32H	A/D converter mode register 1 Note	ADM1		A/D converter mode register 1	ADM1	

Note The bit setting is different from that of RL78/G1A (64-pin products).

Caution Do not write data to the registers which is in the row with painted gray.

Table 3-1. List of Differences in Special Function Registers (SFRs) (4/4)

Address	RL78/G1E (64-pin products)			RL78/G1A (64-pin products)		
	SFRs Name	Symbol		SFRs Name	Symbol	
FFFB0H	Same as RL78/G1A (64-pin products)	DSA0		DMA SFR address register 0	DSA0	
FFFB1H	Same as RL78/G1A (64-pin products)	DSA1		DMA SFR address register 1	DSA1	
FFFB2H	Same as RL78/G1A (64-pin products)	DRA0L	DRA0	DMA RAM address register 0L	DRA0L	DRA0
FFFB3H	Same as RL78/G1A (64-pin products)	DRA0H		DMA RAM address register 0H	DRA0H	
FFFB4H	Same as RL78/G1A (64-pin products)	DRA1L	DRA1	DMA RAM address register 1L	DRA1L	DRA1
FFFB5H	Same as RL78/G1A (64-pin products)	DRA1H		DMA RAM address register 1H	DRA1H	
FFFB6H	Same as RL78/G1A (64-pin products)	DBC0L	DBC0	DMA byte count register 0L	DBC0L	DBC0
FFFB7H	Same as RL78/G1A (64-pin products)	DBC0H		DMA byte count register 0H	DBC0H	
FFFB8H	Same as RL78/G1A (64-pin products)	DBC1L	DBC1	DMA byte count register 1L	DBC1L	DBC1
FFFB9H	Same as RL78/G1A (64-pin products)	DBC1H		DMA byte count register 1H	DBC1H	
FFFBAH	Same as RL78/G1A (64-pin products)	DMC0		DMA mode control register 0	DMC0	
FFFBBH	Same as RL78/G1A (64-pin products)	DMC1		DMA mode control register 1	DMC1	
FFFBCH	Same as RL78/G1A (64-pin products)	DRC0		DMA operation control register 0	DRC0	
FFFBDH	Same as RL78/G1A (64-pin products)	DRC1		DMA operation control register 1	DRC1	
FFFD0H	Interrupt mask flag register 2L Note	IF2L	IF2	Interrupt mask flag register 2L	IF2L	IF2
FFFD1H	Interrupt mask flag register 2H Note	IF2H		Interrupt mask flag register 2H	IF2H	
FFFD4H	Interrupt mask flag register 0L Note	MK2L	MK2	Interrupt mask flag register 0L	MK2L	MK2
FFFD5H	Interrupt mask flag register 2H Note	MK2H		Interrupt mask flag register 2H	MK2H	
FFFD8H	Priority specification flag register 02L Note	PR02L	PR02	Priority specification flag register 02L	PR02L	PR02
FFFD9H	Priority specification flag register 02H Note	PR02H		Priority specification flag register 02H	PR02H	
FFFDCH	Priority specification flag register 12L Note	PR12L	PR12	Priority specification flag register 12L	PR12L	PR12
FFFDDH	Priority specification flag register 12H Note	PR12H		Priority specification flag register 12H	PR12H	
FFFE0H	Interrupt mask flag register 0L Note	IF0L	IF0	Interrupt mask flag register 0L	IF0L	IF0
FFFE1H	Interrupt mask flag register 0H Note	IF0H		Interrupt mask flag register 0H	IF0H	
FFFE2H	Interrupt mask flag register 1L Note	IF1L	IF1	Interrupt mask flag register 1L	IF1L	IF1
FFFE3H	Interrupt mask flag register 1H Note	IF1H		Interrupt mask flag register 1H	IF1H	
FFFE4H	Interrupt mask flag register 0L Note	MK0L	MK0	Interrupt mask flag register 0L	MK0L	MK0
FFFE5H	Interrupt mask flag register 0H Note	MK0H		Interrupt mask flag register 0H	MK0H	
FFFE6H	Interrupt mask flag register 1L Note	MK1L	MK1	Interrupt mask flag register 1L	MK1L	MK1
FFFE7H	Interrupt mask flag register 1H Note	MK1H		Interrupt mask flag register 1H	MK1H	
FFFE8H	Priority specification flag register 00L Note	PR00L	PR00	Priority specification flag register 00L	PR00L	PR00
FFFE9H	Priority specification flag register 00H Note	PR00H		Priority specification flag register 00H	PR00H	
FFFEAH	Priority specification flag register 01L Note	PR01L	PR01	Priority specification flag register 01L	PR01L	PR01
FFFEBH	Priority specification flag register 01H Note	PR01H		Priority specification flag register 01H	PR01H	
FFFECH	Priority specification flag register 10L Note	PR10L	PR10	Priority specification flag register 10L	PR10L	PR10
FFFEDH	Priority specification flag register 10H Note	PR10H		Priority specification flag register 10H	PR10H	
FFFEEH	Priority specification flag register 11L Note	PR11L	PR11	Priority specification flag register 11L	PR11L	PR11
FFFEFH	Priority specification flag register 11H Note	PR11H		Priority specification flag register 11H	PR11H	
FFFF0H FFFF1H	Same as RL78/G1A (64-pin products)	MDAL		Multiplication/division data register A (L)	MDAL	
FFFF2H FFFF3H	Same as RL78/G1A (64-pin products)	MDAH		Multiplication/division data register A (H)	MDAH	
FFFF4H FFFF5H	Same as RL78/G1A (64-pin products)	MDBH		Multiplication/division data register B (L)	MDBH	
FFFF6H FFFF7H	Same as RL78/G1A (64-pin products)	MDBL		Multiplication/division data register B (H)	MDBL	
FFFFEH	Same as RL78/G1A (64-pin products)	PMC		Processor mode control register	PMC	

Note The bit setting is different from that of RL78/G1A (64-pin products).

Table 3-3. List of Differences in Expanded Special Function Registers (2nd SFRs) (2/6)

Address	RL78/G1E (64-pin products)			RL78/G1A (64-pin products)		
	2nd SFRs Name	Symbol		2nd SFRs Name	Symbol	
F0073H	Same as RL78/G1A (64-pin products)	ISC		Input switch control register	ISC	
F0074H	Timer input select register 0 Note	TIS0		Timer input select register 0	TIS0	
F0076H	A/D port configuration register Note	ADPC		A/D port configuration register	ADPC	
F0077H	Peripheral I/O redirection register Note	PIOR		Peripheral I/O redirection register	PIOR	
F0078H	Same as RL78/G1A (64-pin products)	IAWCTL		Invalid memory access detection control register	IAWCTL	
F007CH	Same as RL78/G1A (64-pin products)	GAIDIS		Global analog input disable register	GAIDIS	
F007DH				Global digital input disable register	GDIDIS	
F0090H	Same as RL78/G1A (64-pin products)	DFLCTL		Data flash control register	DFLCTL	
F00A0H	Same as RL78/G1A (64-pin products)	HIOTRM		High-speed on-chip oscillator trimming register	HIOTRM	
F00A8H	Same as RL78/G1A (64-pin products)	HOCODIV		High-speed on-chip oscillator frequency select register	HOCODIV	
F00E0H	Same as RL78/G1A (64-pin products)	MDCL		Multiplication/division data register C (L)	MDCL	
F00E2H	Same as RL78/G1A (64-pin products)	MDCH		Multiplication/division data register C (H)	MDCH	
F00E8H	Same as RL78/G1A (64-pin products)	MDUC		Multiplication/division control register	MDUC	
F00F0H	Peripheral enable register 0 Note	PER0		Peripheral enable register 0	PER0	
<R> F00F3H	Subsystem clock supply mode control register Note	OSMC		Subsystem clock supply mode control register	OSMC	
F00F5H	Same as RL78/G1A (64-pin products)	RPECTL		RAM parity error control register	RPECTL	
F00FEH	Same as RL78/G1A (64-pin products)	BCDADJ		BCD adjust result register	BCDADJ	
F0100H	Same as RL78/G1A (64-pin products)	SSR00L	SSR00	Serial status register 00	SSR00L	SSR00
F0101H		—			—	
F0102H	Same as RL78/G1A (64-pin products)	SSR01L	SSR01	Serial status register 01	SSR01L	SSR01
F0103H		—			—	
F0104H	Same as RL78/G1A (64-pin products)	SSR02L	SSR02	Serial status register 02	SSR02L	SSR02
F0105H		—			—	
F0106H	Same as RL78/G1A (64-pin products)	SSR03L	SSR03	Serial status register 03	SSR03L	SSR03
F0107H		—			—	
F0108H	Same as RL78/G1A (64-pin products)	SIR00L	SIR00	Serial flag clear trigger register 00	SIR00L	SIR00
F0109H		—			—	
F010AH	Same as RL78/G1A (64-pin products)	SIR01L	SIR01	Serial flag clear trigger register 01	SIR01L	SIR01
F010BH		—			—	
F010CH	Same as RL78/G1A (64-pin products)	SIR02L	SIR02	Serial flag clear trigger register 02	SIR02L	SIR02
F010DH		—			—	
F010EH	Same as RL78/G1A (64-pin products)	SIR03L	SIR03	Serial flag clear trigger register 03	SIR03L	SIR03
F010FH		—			—	

Note The bit setting is different from that of RL78/G1A (64-pin products).

Caution Do not write data to the registers which is in the row with painted gray.

3. 6. 3 Registers controlling timer array unit

The bit settings which are different from that of RL78/G1A (64-pin products) are shown below. For details of each register, see **6. 3 Registers Controlling Timer Array Unit** in **RL78/G1A Hardware User's Manual (R01UH0305E)**.

<R> 3. 6. 3. 1 Peripheral enable register 0 (PER0)

Address: F00F0H After reset: 00H R/W

Symbol	<7>	6	<5>	4	<3>	<2>	1	<0>
PER0	RTCEN	0	ADCEN	0	SAU1EN	SAU0EN	0	TAU0EN

TAU0EN	Control of timer array 0 unit input clock
0	Stops input clock supply. • SFR used by timer array unit 0 cannot be written. • Timer array unit 0 is in the reset status.
1	Enables input clock supply. • SFR used by timer array unit 0 can be read/written.

Cautions 1. When setting the timer array unit, be sure to set the TAUmEN bit to 1 first. If TAUmEN = 0, writing to a control register of timer array unit is ignored, and all read values are default values (except for the timer input select register 0 (TIS0), input switch control register (ISC), noise filter enable register 1 (NFEN1), port mode control registers 0, 1, 4 (PMC0, PMC1, PMC4), port mode registers 0, 1, 4 (PM0, PM1, PM4), and port registers 0, 1, 4 (P0, P1, P4)).

- **Timer clock select register m (TPSm)**
- **Timer mode register mn (TMRmn)**
- **Timer status register mn (TSRmn)**
- **Timer channel enable status register m (TEm)**
- **Timer channel start register m (TSm)**
- **Timer channel stop register m (TTm)**
- **Timer output enable register m (TOEm)**
- **Timer output register m (TOm)**
- **Timer output level register m (TOLm)**
- **Timer output mode register m (TOMm)**

2. Be sure to clear bits 1, 4, and 6 to "0".

3. 6. 3. 2 Timer clock select register m (TPSm)

The bit setting is same as that of RL78/G1A (64-pin products). For details, see **6. 3. 2 Timer clock select register m (TPSm)** in **RL78/G1A Hardware User's Manual (R01UH0305E)**.

<R> **3. 9. 3. 2 Registers controlling port functions of pins to be used for clock or buzzer output**

Using a port pin for clock or buzzer output requires setting of the registers that control the port functions multiplexed on the target pin (port mode register (PMxx), port register (Pxx)). For details, see **3. 4. 3. 1 Port mode registers (PMxx)** and **3. 4. 3. 2 Port registers (Pxx)**.

For details of setting example, see **9. 3. 2 Registers controlling port functions of pins to be used for clock or buzzer output** in **RL78/G1A Hardware User's Manual (R01UH0305E)**.

3. 9. 4 Operations of clock output/buzzer output controller

See **9. 4 Operations of Clock Output/Buzzer Output Controller** in **RL78/G1A Hardware User's Manual (R01UH0305E)**.

3. 9. 5 Cautions of clock output/buzzer output controller

See **9. 5 Cautions of Clock Output/Buzzer Output Controller** in **RL78/G1A Hardware User's Manual (R01UH0305E)**.

<R> **3. 12. 3 Registers controlling serial array unit**

The bit settings which are different from that of RL78/G1A (64-pin products) are shown below. For details of each register, see **12. 3 Registers Controlling Serial Array Unit** in **RL78/G1A Hardware User's Manual (R01UH0305E)**.

3. 12. 3. 1 Peripheral enable register 0 (PER0)

Address: F00F0H After reset: 00H R/W

Symbol	<7>	6	<5>	4	<3>	<2>	1	<0>
PER0	RTCEN	0	ADCEN	0	SAU1EN	SAU0EN	0	TAU0EN

SAU1EN	Control of serial array unit 1 input clock supply
0	Stops input clock supply. • SFR used by the serial array unit 1 cannot be written. • The serial array unit 1 is in the reset status.
1	Enables input clock supply. • SFR used by the serial array unit 1 can be read/written.

<R>

SAU0EN	Control of serial array unit 0 input clock supply
0	Stops input clock supply. • SFR used by the serial array unit 0 cannot be written. • The serial array unit 0 is in the reset status.
1	Enables input clock supply. • SFR used by the serial array unit 0 can be read/written.

<R>

Caution Be sure to clear bits 1, 4, and 6 to "0".

3. 12. 3. 2 Serial clock select register m (SPSm)

The bit setting is same as that of RL78/G1A (64-pin products). For details, see **12. 3. 2 Serial clock select register m (SPSm)** in **RL78/G1A Hardware User's Manual (R01UH0305E)**.

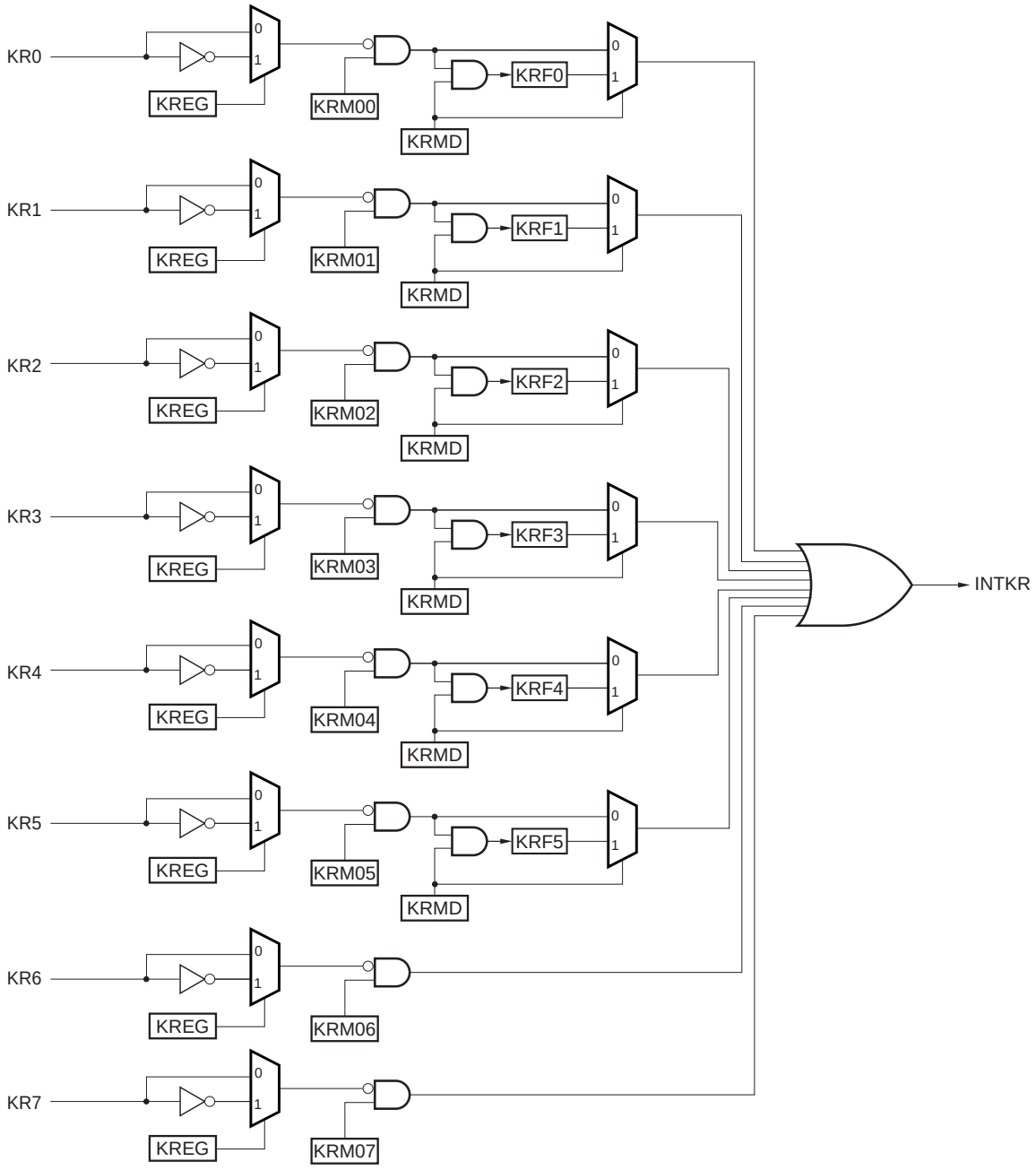
Notes 1. If one of the interrupt sources INTST1, INTCSI10, and INTIIC10 is generated, bit 0 of the IF1L register is set to 1. Bit 0 of the MK1L, PR01L, and PR11L registers can be used for all three of these interrupt sources.

2. If one of the interrupt sources INTSR1, INTCSI11, and INTIIC11 is generated, bit 1 of the IF1L register is set to 1. Bit 1 of the MK1L, PR01L, and PR11L registers can be used for all three of these interrupt sources.

<R> **3.** Do not use the error interrupt of UART1 reception and the interrupt of channel 3 of TAU0 (while the higher 8 bits are operating at a timer) at the same time because they share flags for the interrupt request sources. If the error interrupt of UART1 reception is not used (EOC03 = 0), UART1 and channel 3 of TAU0 (while the higher 8 bits are operating at a timer) can be used at the same time. If the interrupt source INTSRE1 or INTTM03H is generated, bit 2 of the IF1L register is set to 1. Bit 2 of the MK1L, PR01L, and PR11L registers can be used for both these interrupt sources.

<R>

Figure 3-14. Block Diagram of Key Interrupt



Remark KR0 to KR3 (KR0 to KR6): 64-pin products
KR0 to KR3 (KR0 to KR7): 80-pin products
Functions in parentheses can be assigned via settings in the peripheral I/O redirection register (PIOR)

4. 1. 3 Registers controlling the configurable amplifiers

The configurable amplifiers are controlled by the following 9 registers:

- Configuration register 1 (CONFIG1)
- Configuration register 2 (CONFIG2)
- MPX setting register 1 (MPX1)
- MPX setting register 2 (MPX2)
- Gain control register 1 (GC1)
- Gain control register 2 (GC2)
- Gain control register 3 (GC3)
- AMP operation mode control register (AOMC)
- Power control register 1 (PC1)

(5) Gain control register 1 (GC1)

This register is used to specify the gain and feedback resistance of configurable amplifier Ch1.

The value to specify depends on the configuration of configurable amplifier Ch1.

When using configurable amplifiers Ch1 to Ch3 together as an instrumentation amplifier, be sure to set gain control register 1 (GC1) to 03H.

Reset signal input clears this register to 00H.

Address: 06H After reset: 00H R/W

	7	6	5	4	3	2	1	0
GC1	0	0	0	AMPG14	AMPG13	AMPG12	AMPG11	AMPG10

Table 4-1. Gain of Configurable Amplifier Ch1 (Non-Inverting Amplifier)

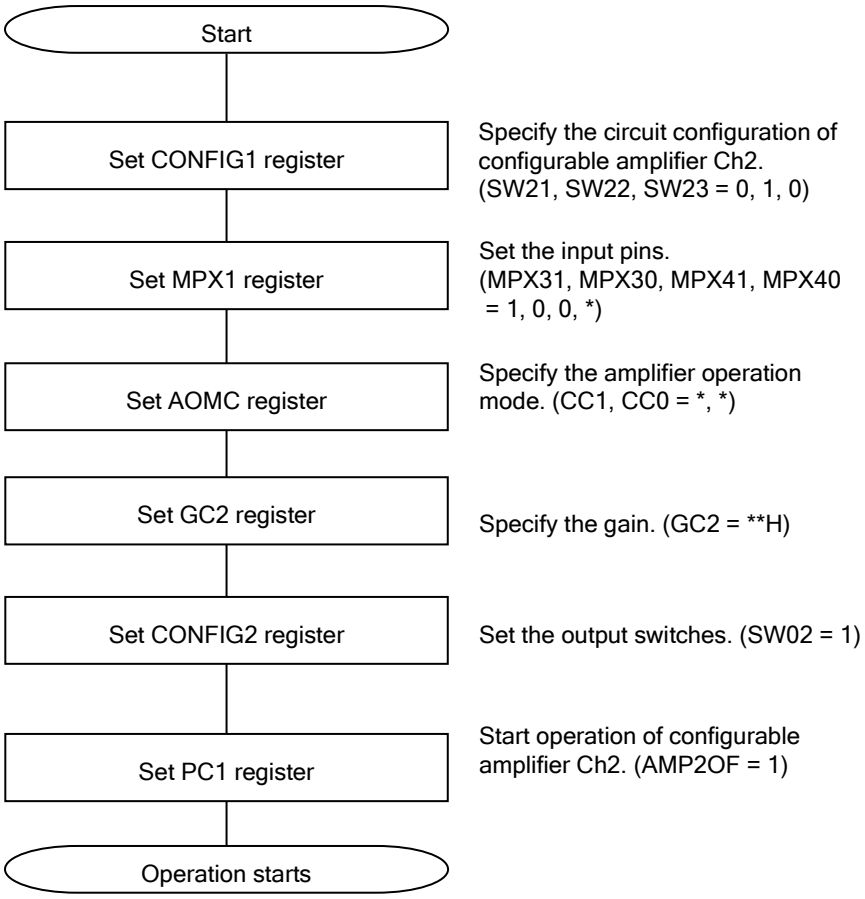
AMPG14	AMPG13	AMPG12	AMPG11	AMPG10	Gain of Configurable Amplifier Ch1 (Typ.)
0	0	0	0	0	9.5 dB
0	0	0	0	1	10.9 dB
0	0	0	1	0	12.4 dB
0	0	0	1	1	14.0 dB
0	0	1	0	0	15.6 dB
0	0	1	0	1	17.3 dB
0	0	1	1	0	19.0 dB
0	0	1	1	1	20.8 dB
0	1	0	0	0	22.7 dB
0	1	0	0	1	24.5 dB
0	1	0	1	0	26.4 dB
0	1	0	1	1	28.3 dB
0	1	1	0	0	30.3 dB
0	1	1	0	1	32.2 dB
0	1	1	1	0	34.2 dB
0	1	1	1	1	36.1 dB
1	0	0	0	0	38.1 dB
1	0	0	0	1	40.1 dB
Other than above					Setting prohibited

<R> **Remark** Bits 7 to 5 are fixed at 0 of read only.

Table 4-9. Feedback Resistance of Configurable Amplifier Ch3 (Transimpedance Amplifier)

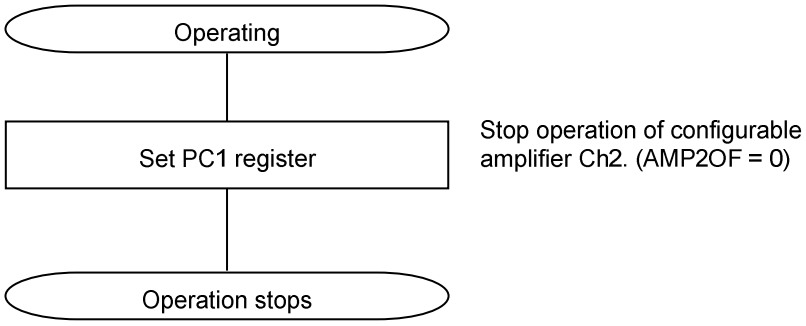
AMPG34	AMPG33	AMPG32	AMPG31	AMPG30	Feedback Resistance of Configurable Amplifier Ch3 (Typ.)
0	0	0	0	0	20 kΩ
0	0	0	0	1	
0	0	0	1	0	
0	0	0	1	1	40 kΩ
0	0	1	0	0	
0	0	1	0	1	
0	0	1	1	0	80 kΩ
0	0	1	1	1	
0	1	0	0	0	
0	1	0	0	1	160 kΩ
0	1	0	1	0	
0	1	0	1	1	
0	1	1	0	0	320 kΩ
0	1	1	0	1	
0	1	1	1	0	
0	1	1	1	1	640 kΩ
1	0	0	0	0	
1	0	0	0	1	
Other than above					Setting prohibited

Example of procedure for starting configurable amplifier Ch2 (non-inverting amplifier)



Remark *: don't care

Example of procedure for stopping configurable amplifier Ch2 (non-inverting amplifier)



4. 10. 2 Registers controlling the analog reset

(1) Reset control register (RC)

This register is used to control the reset feature in the analog block.

<R> An internal reset can be generated by writing 1 to the RESET bit. The reset control register (RC) is not initialized by generating internal reset of the reset control register, but it can be done by generating external reset from $\overline{\text{ARESET}}$ pin. External reset from $\overline{\text{ARESET}}$ pin clears this register to 00H.

Address: 13H After reset: 00H Note R/W

	7	6	5	4	3	2	1	0
RC	0	0	0	0	0	0	0	RESET

RESET	Reset request by internal reset signal
0	Do not make a reset request by using the internal reset signal, or cancel the reset.
1	Make a reset request by using the internal reset signal, or the reset signal is currently being input.

<R> **Note** The reset control register is not initialized by generating internal reset of the reset control register, but it can be done to 00H by generating external reset from $\overline{\text{ARESET}}$ pin or by writing 0 to the RESET bit of the reset control register (RC).

Caution When the RESET bit is 1, writing to any register other than the reset control register (RC) is ignored. Initializing the reset control register (RC) to 00H by external reset, or writing 0 to the RESET bit enables writing to all the registers.

<R> **Remark** Bits 7 to 1 are fixed at 0 of read only.

CHAPTER 5 ELECTRICAL SPECIFICATIONS

In this capter, the electrical specification is described for the target products shown below.

Target products A: Consumer applications T_A = −40 to +85°C
R5F10FLCANA, R5F10FLCANA, R5F10FLDANA, R5F10FLDANA,
R5F10FLEANA, R5F10FLEANA, R5F10FMCAFB, R5F10FMCAFB,
R5F10FMDAFB, R5F10FMDAFB, R5F10FMEAFB, R5F10FMEAFB

Target products D: Industrial applications T_A = −40 to +85°C
R5F10FLCDNA, R5F10FLCDNA, R5F10FLDDNA, R5F10FLDDNA,
R5F10FLEDNA, R5F10FLEDNA, R5F10FMCDFB, R5F10FMCDFB,
R5F10FMDDFB, R5F10FMDDFB, R5F10FMEDFB, R5F10FMEDFB

Cautions 1. The RL78/G1E microcontrollers have an on-chip debug function, which is provided for development and evaluation. Do not use the on-chip debug function in products designated for mass production, because the guaranteed number of rewritable times of the flash memory may be exceeded when this function is used, and product reliability therefore cannot be guaranteed. Renesas Electronics is not liable for problems occurring when the on-chip debug function is used.

2. The pins mounted depend on the product, so that refer to CHAPTER 2 PIN FUNCTIONS. In this Chapter, most of the descriptions use the case of 80-pin products as an example.

<R> **(4) Communication between devices at same potential (CSI mode)**
(slave mode, SCKp ... External clock input) (1/2)

(T_A = –40 to +85°C, 1.6 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V) (1/2)

Parameter	Symbol	Conditions		HS Note 1		LS Note 2		LV Note 3		Unit
				MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
SCKp cycle time Note 4	t_{KCY2}	4.0V ≤ V_{DD} ≤ 5.5V	20MHz < f_{MCK}	8/f_{MCK}		–		–		ns
			f_{MCK} ≤ 20MHz	6/f_{MCK}		6/f_{MCK}		6/f_{MCK}		ns
		2.7V ≤ V_{DD} ≤ 5.5V	16MHz < f_{MCK}	8/f_{MCK}		–		–		ns
			f_{MCK} ≤ 16MHz	6/f_{MCK}		6/f_{MCK}		6/f_{MCK}		ns
		2.4 V ≤ V_{DD} ≤ 5.5 V		6/f_{MCK} and 500ns		6/f_{MCK} and 500ns		6/f_{MCK} and 500ns		ns
		1.8 V ≤ V_{DD} ≤ 5.5 V		6/f_{MCK} and 750ns		6/f_{MCK} and 750ns		6/f_{MCK} and 750ns		ns
		1.7 V ≤ V_{DD} ≤ 5.5 V		6/f_{MCK} and 1500ns		6/f_{MCK} and 1500ns		6/f_{MCK} and 1500ns		ns
		1.6 V ≤ V_{DD} ≤ 5.5 V		–		6/f_{MCK} and 1500ns		6/f_{MCK} and 1500ns		ns
SCKp high-level width low-level width	t_{KH2}, t_{KL2}	4.0 V ≤ V_{DD} ≤ 5.5 V		t_{KCY2}/2 -7		t_{KCY2}/2 -7		t_{KCY2}/2 -7		ns
		2.7 V ≤ V_{DD} ≤ 5.5 V		t_{KCY2}/2 -8		t_{KCY2}/2 -8		t_{KCY2}/2 -8		ns
		1.8 V ≤ V_{DD} ≤ 5.5 V		t_{KCY2}/2 -18		t_{KCY2}/2 -18		t_{KCY2}/2 -18		ns
		1.7 V ≤ V_{DD} ≤ 5.5 V		t_{KCY2}/2 -66		t_{KCY2}/2 -66		t_{KCY2}/2 -66		ns
		1.6 V ≤ V_{DD} ≤ 5.5 V		–		t_{KCY2}/2 -66		t_{KCY2}/2 -66		ns

Notes 1. HS is condition of HS (high-speed main) mode.

2. LS is condition of LS (low-speed main) mode.

3. LV is condition of LV (low-voltage main) mode.

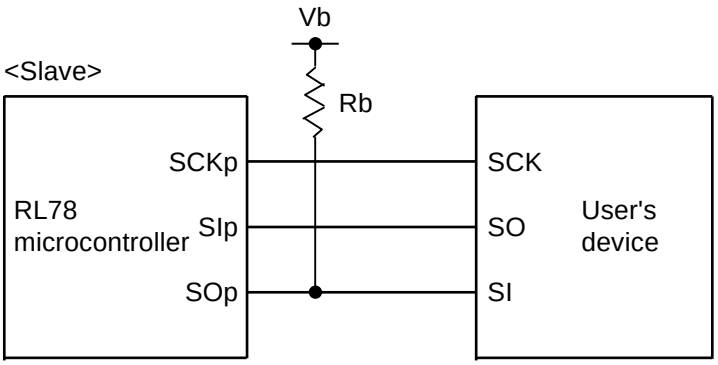
4. Transfer rate in the SNOOZE mode: MAX. 1 Mbps

Caution Select the normal input buffer for the SIp pin and SCKp pin and the normal output mode for the SOp pin by using port input mode register g (PIMg) and port output mode register g (POMg).

Remarks 1. p: CSI number (p = 00, 10, 20, 21), m: Unit number (m = 0, 1), n: Channel number (n = 0 to 2), g: PIM and POM numbers (g = 0, 1)

2. f_{MCK}: Serial array unit operating clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn).
m: Unit number, n: Channel number (mn = 00 to 03, 10, 11))

CSI mode connection diagram (during communication between devices at different potential)



Remarks 1. Rb [Ω]: Communication line (SOp) pull-up resistance, Cb [F]: Communication line (SOp) load capacitance, Vb [V]: Communication line voltage

2. p: CSI number (p = 00, 10, 20), m: Unit number, n: Channel number (mn = 00, 10, 20),
g: PIM and POM numbers (g = 0, 1)

3. f_{MCK}: Serial array unit operating clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00, 10, 20))

4. The AC characteristics of serial array units communicating with a device at different potential in CSI mode is observed at V_{IH} and V_{IL} below.
4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ Vb ≤ 4.0 V: V_{IH} = 2.2 V, V_{IL} = 0.8 V
2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ Vb ≤ 2.7 V: V_{IH} = 2.0 V, V_{IL} = 0.5 V
1.8 V ≤ V_{DD} < 3.3 V, 1.6 V ≤ Vb ≤ 2.0 V: V_{IH} = 1.5 V, V_{IL} = 0.32 V

5. CSI01, CSI11, and CSI21 cannot communicate with a device at different potential. Use other CSI channels for communication between devices at different potential.