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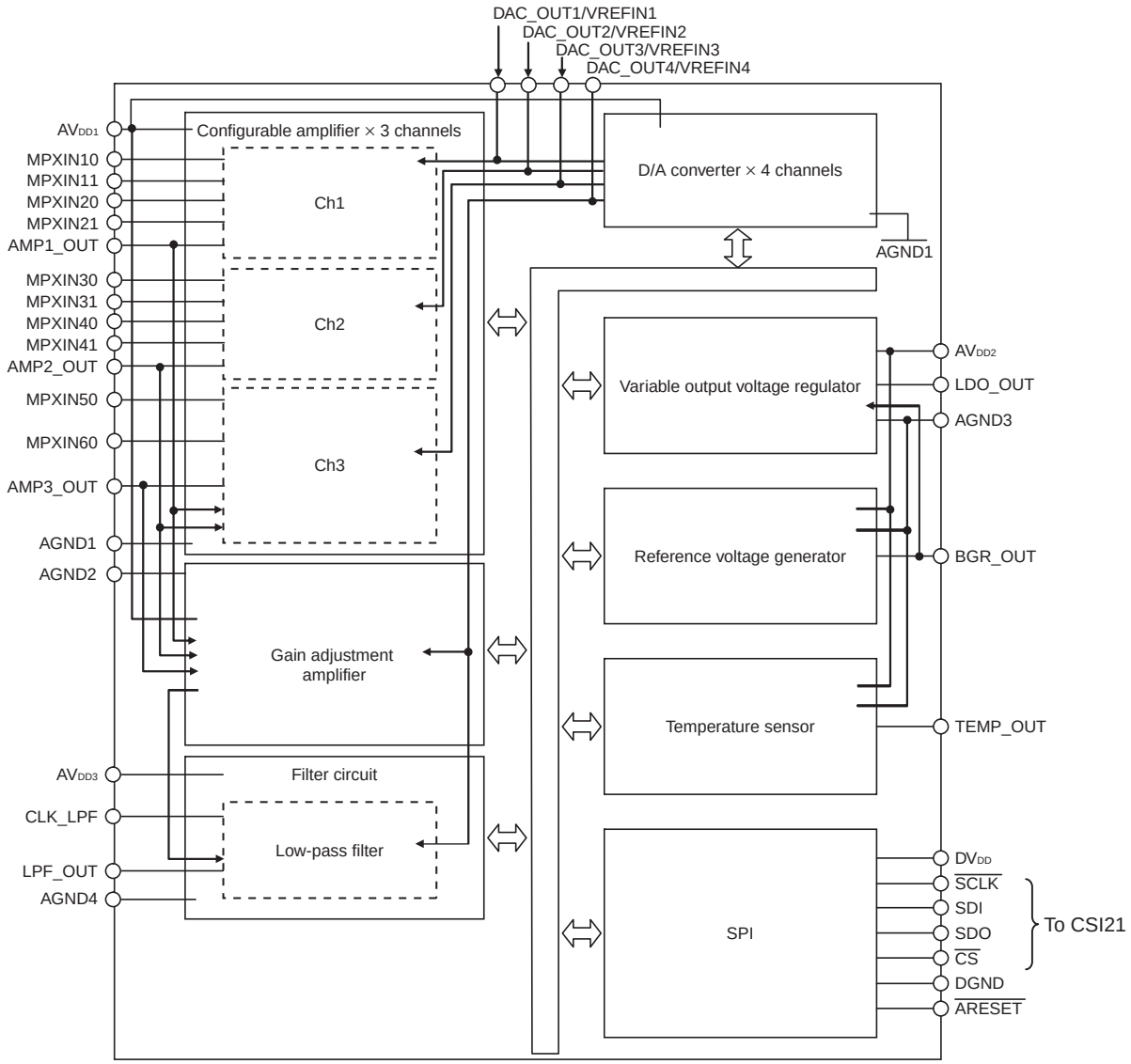
What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	RL78
Core Size	16-Bit
Speed	32MHz
Connectivity	CSI, I²C, LINbus, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	26
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	1.6V ~ 5.5V
Data Converters	A/D 17x8/12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	80-LQFP
Supplier Device Package	80-LFQFP (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f10fmcdfb-x0

(2) Block diagram in analog block (64-pin products)



2. 1. 1. 2 80-pin products

(1/2)

<R>

Function Name	Pin Type	I/O	After Reset	Alternate Function	Function
P00	8-1-1	I/O	Input port	TI00/(KR0)	Port 0. 5-bit I/O port. Input of P00, P01, P03, and P04 can be set to TTL input buffer. Output of P02 to P04 can be set to N-ch open-drain output (V_{DD} tolerance). P02 and P03 can be set to analog input. Note 1 Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting at input port.
P01				TO00/(KR1)	
P02	7-3-2		Analog input port	ANI17/SO10/TxD1/(KR2)	
P03	8-3-2			ANI16/SI10/RxD1/ SDA10/(KR3)	
P04	8-1-2		Input port	SCK10/SCL10/(KR4)	
P10	8-3-2	I/O	Analog input port	ANI18/SCK00/ SCL00/(KR0)	Port 1. 6-bit I/O port. Input of P10, P11, P14, and P15 can be set to TTL input buffer. Output of P10 to P15 can be set to N-ch open-drain output (V_{DD} tolerance). P10 to P15 can be set to analog input. Note 1 Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting at input port.
P11				ANI20/SI00/RxD0/ TOOLRxD/SDA00/(KR1)	
P12	7-3-2			ANI21/SO00/TxD0/ TOOLTxD/(KR2)	
P13				ANI22/TxD2/SO20/(KR3)	
P14	8-3-2			ANI23/RxD2/SI20/ SDA20/(KR4)	
P15				ANI24/SCK20/ SCL20/(KR5)	
P20	4-3-1	I/O	Analog input port	ANI0/AV_{REFP}	Port 2. 5-bit I/O port. Can be set to analog input. Note 2 Input/output can be specified in 1-bit units.
P21				ANI1/AV_{REFM}	
P22				ANI2/(KR5)	
P23				ANI3/(KR6)	
P24				ANI4/(KR7)	
P40	7-1-1	I/O	Input port	TOOL0	Port 4. 3-bit I/O port. P41 can be set to analog input. Note 1 Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting at input port.
P41	7-3-1		Analog input port	ANI30/TI07/TO07	
P42	7-1-1		Input port	TI04/TO04	

<R> **Notes 1.** Digital or analog for each pin can be selected with the port mode control register x (PMCx) (can be set in 1-bit units).

2. Digital or analog for each pin can be selected with the A/D port configuration register (ADPC).

<R> **Remark** Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR). About format, see Figure in **3. 4. 3. 8 Peripheral I/O redirection register (PIOR)**.

2. 5. 4 Port 4 (P40 to P42)

(1) Port mode

P40 to P42 function as an I/O port. P40 to P42 can be set to input or output port in 1-bit units using port mode register 4 (PM4).

(2) Control mode

P40 to P42 function as A/D converter analog input, data I/O for a flash memory programmer/debugger, and timer I/O.

(a) TI04, TI07

These are the pins for inputting an external count clock/capture trigger to 16-bit timers 04 and 07.

(b) TO04, TO07

These are the timer output pins from 16-bit timers 04 and 07.

(c) TOOL0

This is a data I/O pin for a flash memory programmer/debugger.

Be sure to pull up this pin externally when on-chip debugging is enabled (pulling it down is prohibited).

(d) ANI30

This is an analog input pin of A/D converter.

2. 5. 8 Port 13 (P130, P137)

(1) Port mode

P130 functions as an output port.

P137 functions as an input port.

(2) Control mode

P137 functions as external interrupt request input.

(a) INTP0

This is an external interrupt request input pin for which the valid edge (rising edge, falling edge, or both rising and falling edges) can be specified.

(4/4)

Item	RL78/G1E		RL78/G1A	Remarks
	64-pin products	80-pin products	(64-pin products)	
Standby function	HALT, STOP, SNOOZE mode		HALT, STOP, SNOOZE mode	See 3. 18.
Reset function	7 reset source		7 reset source	See 3. 19.
Power-on-reset circuit	Power-on-reset: 1.51 +/- 0.03V Power-down-reset: 1.50 +/- 0.03V		Power-on-reset: 1.51 +/- 0.03V Power-down-reset: 1.50 +/- 0.03V	See 3. 20.
Voltage detector	Detection level: 3 stages		Detection level: 12 stages	Some differences. See the section 3. 21 about details.
Safety functions	- Flash memory CRC operation function - CRC operation function - RAM parity error detection function - RAM guard function - SFR guard function - Invalid memory access detection function - Frequency detection function - A/D test function		- Flash memory CRC operation function - CRC operation function - RAM parity error detection function - RAM guard function - SFR guard function - Invalid memory access detection function - Frequency detection function - A/D test function	Some differences. See the section 3. 22 about details.
Regulator	1 channel		1 channel	See 3. 23
Option byte	Available		Available	Some differences. See the section 3. 24 about details.
Flash memory	Available		Available	Some differences. See the section 3. 25 about details.
On-chip debug function	Available		Available	See 3. 26
BCD correction circuit	Available		Available	See 3. 27
Instruction set	• Data transfer (8/16 bits) • Adder and subtractor/logical operation (8/16 bits) • Multiplication (8 bits × 8 bits) • Rotate, barrel shift, and bit manipulation (Set, reset, test, and Boolean operation), etc.		• Data transfer (8/16 bits) • Adder and subtractor / logical operation (8/16 bits) • Multiplication (8 bits × 8 bits) • Rotate, barrel shift, and bit manipulation (Set, reset, test, and Boolean operation), etc.	See 3. 28
Power supply voltage	V_{DD} = 1.6 to 5.5 V		V_{DD} = 1.6 to 3.6 V	V_{DD} range is different.

Table 3-4. List of Differences in Expanded Special Function Registers (2nd SFRs) (5/6)

Address	RL78/G1E (80-pin products)			RL78/G1A (64-pin products)		
	2nd SFRs Name	Symbol		2nd SFRs Name	Symbol	
F0180H	Same as RL78/G1A (64-pin products)	TCR00		Timer counter register 00	TCR00	
F0181H						
F0182H	Same as RL78/G1A (64-pin products)	TCR01		Timer counter register 01	TCR01	
F0183H						
F0184H	Same as RL78/G1A (64-pin products)	TCR02		Timer counter register 02	TCR02	
F0185H						
F0186H	Same as RL78/G1A (64-pin products)	TCR03		Timer counter register 03	TCR03	
F0187H						
F0188H	Same as RL78/G1A (64-pin products)	TCR04		Timer counter register 04	TCR04	
F0189H						
F018AH	Same as RL78/G1A (64-pin products)	TCR05		Timer counter register 05	TCR05	
F018BH						
F018CH	Same as RL78/G1A (64-pin products)	TCR06		Timer counter register 06	TCR06	
F018DH						
F018EH	Same as RL78/G1A (64-pin products)	TCR07		Timer counter register 07	TCR07	
F018FH						
F0190H	Same as RL78/G1A (64-pin products)	TMR00		Timer mode register 00	TMR00	
F0191H						
F0192H	Timer mode register 01 Note	TMR01		Timer mode register 01	TMR01	
F0193H						
F0194H	Timer mode register 02 Note	TMR02		Timer mode register 02	TMR02	
F0195H						
F0196H	Timer mode register 03 Note	TMR03		Timer mode register 03	TMR03	
F0197H						
F0198H	Same as RL78/G1A (64-pin products)	TMR04		Timer mode register 04	TMR04	
F0199H						
F019AH	Timer mode register 05 Note	TMR05		Timer mode register 05	TMR05	
F019BH						
F019CH	Timer mode register 06 Note	TMR06		Timer mode register 06	TMR06	
F019DH						
F019EH	Same as RL78/G1A (64-pin products)	TMR07		Timer mode register 07	TMR07	
F019FH						
F01A0H	Same as RL78/G1A (64-pin products)	TSR00L	TSR00	Timer status register 00	TSR00L	TSR00
F01A1H		—			—	
F01A2H	Same as RL78/G1A (64-pin products)	TSR01L	TSR01	Timer status register 01	TSR01L	TSR01
F01A3H		—			—	
F01A4H	Same as RL78/G1A (64-pin products)	TSR02L	TSR02	Timer status register 02	TSR02L	TSR02
F01A5H		—			—	
F01A6H	Same as RL78/G1A (64-pin products)	TSR03L	TSR03	Timer status register 03	TSR03L	TSR03
F01A7H		—			—	
F01A8H	Same as RL78/G1A (64-pin products)	TSR04L	TSR04	Timer status register 04	TSR04L	TSR04
F01A9H		—			—	
F01AAH	Same as RL78/G1A (64-pin products)	TSR05L	TSR05	Timer status register 05	TSR05L	TSR05
F01ABH		—			—	
F01ACH	Same as RL78/G1A (64-pin products)	TSR06L	TSR06	Timer status register 06	TSR06L	TSR06
F01ADH		—			—	
F01AEH	Same as RL78/G1A (64-pin products)	TSR07L	TSR07	Timer status register 07	TSR07L	TSR07
F01AFH		—			—	

Note The bit setting is different from that of RL78/G1A (64-pin products).

3. 4. 2. 9 Port 12

P121 and P122 pins are specified as an input-only port. This port can be also used for the pin connecting resonator for main system clock, and external clock input for main system clock.

When reset signal is generated, the P121 and P122 pins will be set to input mode.

3. 4. 2. 10 Port 13

P130 pin is specified as a 1-bit output-only port with an output latch. P137 pin is specified as a 1-bit input-only port and can be also used for external interrupt request input.

3. 4. 2. 11 Port 14

Port 14 is an I/O port with an output latch. Port 14 can be set to the input mode or output mode in 1-bit units using port mode register 14 (PM14). When the P140 pin is used as an input port, use of an on-chip pull-up resistor can be specified in 1-bit units by pull-up resistor option register 14 (PU14). This port can be also used for clock/buzzer output, and external interrupt request input.

When reset signal is generated, the P140 pin will be set to input mode.

3. 4. 2. 12 Port 15

Port 15 is not available for RL78/G1E.

<R> **3. 5. 3. 7 Subsystem clock supply mode control register (OSMC)**

Address: F00F3H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
OSMC	0	0	0	WUTMMCK0	0	0	0	0

WUTMMCK0	Operation clock for12-bit interval timer
0	Initial value
1	Low-speed on-chip oscillator clock

Cautions 1. Be sure to clear bit 7 to "0".

2. To use 12-bit interval timer, after reset release, set the WUTMMCK0 bit of the subsystem clock supply mode control register (OSMC) to "1" before setting the RTCEN bit of the peripheral enable register0 (PER0) to "1".

Remark The subsystem clock is not supported by RL78/G1E, but the subsystem clock supply mode control register is used to control the clock of 12-bit interval timer.

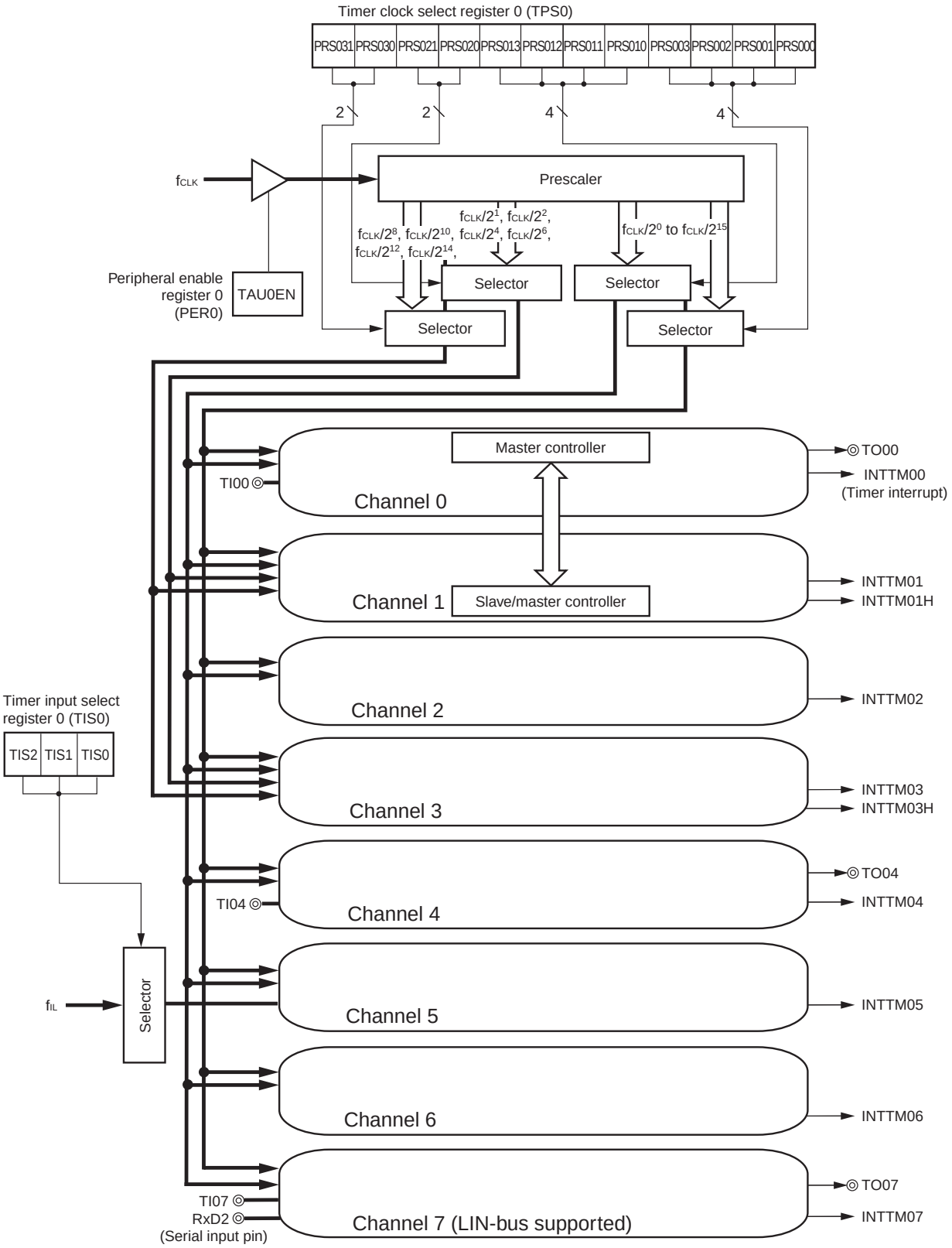
3. 5. 3. 8 High-speed on-chip oscillator frequency select register (HOCODIV)

The bit setting is same as that of RL78/G1A (64-pin products). For details, see **5. 3. 8 High-speed on-chip oscillator frequency select register (HOCODIV)** in **RL78/G1A Hardware User's Manual (R01UH0305E)**.

3. 5. 3. 9 High-speed on-chip oscillator trimming register (HIOTRM)

The bit setting is same as that of RL78/G1A (64-pin products). For details, see **5. 3. 9 High-speed on-chip oscillator trimming register (HIOTRM)** in **RL78/G1A Hardware User's Manual (R01UH0305E)**.

Figure 3-3. Entire Configuration of Timer Array Unit 0 (Example: 80-pin products)



Remark f_{IL}: ow-speed on-chip oscillator clock frequency

<R> 3. 6. 3. 15 Registers controlling port functions of pins to be used for timer I/O

Using port pins for the timer array unit functions requires setting of the registers that control the port functions multiplexed on the target pins (port mode register (PMxx), port register (Pxx), and port mode control register (PMCxx)). For details, see **3. 4. 3. 1 Port mode registers (PMxx)**, **3. 4. 3. 2 Port registers (Pxx)**, and **3. 4. 3. 6 Port mode control registers (PMCxx)**.

For details of setting example, see **6. 3. 15 Registers controlling port functions of pins to be used for timer I/O** in **RL78/G1A Hardware User's Manual (R01UH0305E)**.

3. 24 Option Byte

3. 24. 1 Functions of option bytes

Addresses 000C0H to 000C3H of the flash memory of the RL78/G1E form an option byte area.

Option bytes consist of user option byte (000C0H to 000C2H) and on-chip debug option byte (000C3H).

Upon power application or resetting and starting, an option byte is automatically referenced and a specified function is set. For the bits to which no function is allocated, be sure to set the value specified in this manual.

To use the boot swap operation during self programming, 000C0H to 000C3H are replaced by 010C0H to 010C3H. Therefore, set the same values as 000C0H to 000C3H to 010C0H to 010C3H.

Caution Be sure to specify option byte settings regardless of whether they are used or not.

3. 24. 1. 1 User option byte (000C0H to 000C2H/010C0H to 010C2H)

<R> **(1) 000C0H/010C0H**

- ○ Setting of watchdog timer operation
  - Enabling or disabling of counter operation
  - Enabling or disabling of counter operation in the HALT or STOP mode
- ○ Setting of overflow time of watchdog timer
- ○ Setting of window open period of watchdog timer
- ○ Setting of interval interrupt of watchdog timer
  - Whether or not to use the interval interrupt is selectable

Caution Set the same value as 000C0H to 010C0H when the boot swap operation is used because 000C0H is replaced by 010C0H.

<R> **(2) 000C1H/010C1H**

- ○ Setting of LVD operation mode
  - Interrupt & reset mode.
  - Reset mode.
  - Interrupt mode.
  - LVD off (by controlling the externally input reset signal on the $\overline{\text{RESET}}$ pin)
- ○ Setting of LVD detection level (V_{LVDH}, V_{LVDL}, V_{LVD})

<R> **Cautions1. After power is supplied, the reset state must be retained until the operating voltage becomes in the range defined in 5. 2. 3 AC characteristics. This is done by utilizing the voltage detection circuit or controlling the externally input reset signal. After the power supply is turned off, this LSI should be placed in the STOP mode, or placed in the reset state by utilizing the voltage detection circuit or controlling the externally input reset signal, before the voltage falls below the operating range. The range of operating voltage varies with the setting of the user option byte (000C2H or 010C2H).**

2. Set the same value as 000C1H to 010C1H when the boot swap operation is used because 000C1H is replaced by 010C1H.

3. 24. 2 Format of user option byte

For details of each register, see **24. 2 Format of User Option Byte** in **RL78/G1A Hardware User's Manual (R01UH0305E)**.

The bit settings which are different from that of RL78/G1A (64-pin products) are shown below.

Format of user option byte (000C1H/010C1H) (1/2)

Address: 000C1H/010C1H [Note]

7	6	5	4	3	2	1	0
VPOC2	VPOC1	VPOC0	1	LVIS1	LVIS0	LVIMDS1	LVIMDS0

<R> • LVD setting (interrupt & reset mode)

Detection voltage			Option byte setting value						
V_{LVDH}		V_{LVDL}	VPOC2	VPOC1	VPOC0	LVIS1	LVIS0	Mode setting	
Rising edge	Falling edge	Falling edge						LVIMDS1	LVIMDS0
3.13	3.06	1.84	0	0	1	0	0	1	0
3.75	3.67	2.45	0	1	0	0	0		
4.06	3.98	2.75	0	1	1	0	0		
–			Value other than above is setting prohibited.						

<R> • LVD setting (reset mode)

Detection voltage		Option byte setting value						
V_{LVDH}		VPOC2	VPOC1	VPOC0	LVIS1	LVIS0	Mode setting	
Rising edge	Falling edge						LVIMDS1	LVIMDS0
3.13	3.06	0	0	1	0	0	1	1
3.75	3.67	0	1	0	0	0		
4.06	3.98	0	1	1	0	0		
–		Value other than above is setting prohibited.						

Note Set the same value as 000C1H to 010C1H when the boot swap operation is used because 000C1H is replaced by 010C1H.

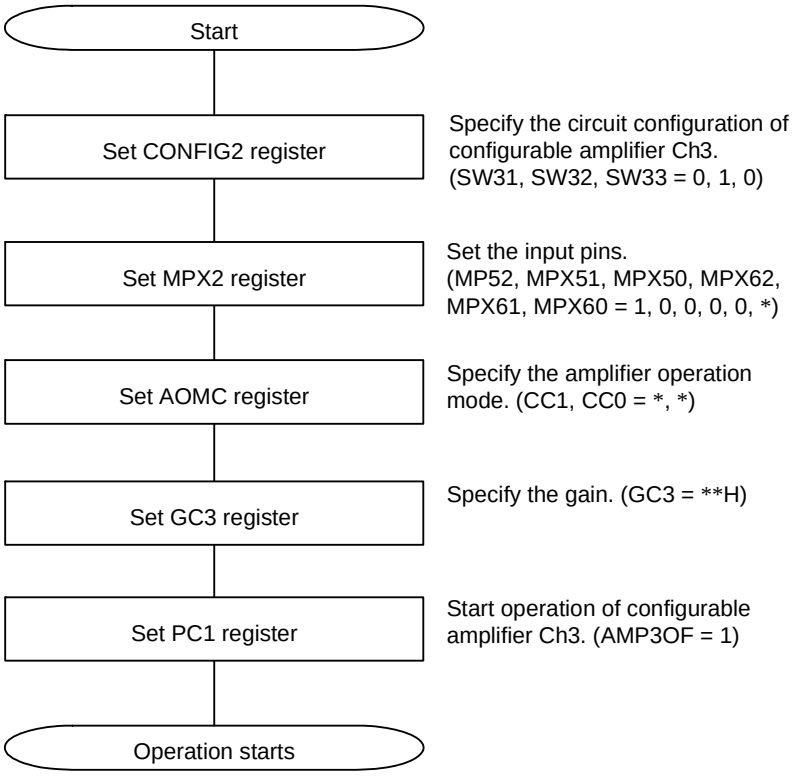
Cautions 1. Be sure to set bit 4 to "1".

2. After power is supplied, the reset state must be retained until the operating voltage becomes in the range defined in 5. 2. 3 AC Characteristics. This is done by utilizing the voltage detection circuit or controlling the externally input reset signal. After the power supply is turned off, this LSI should be placed in the STOP mode, or placed in the reset state by utilizing the voltage detection circuit or controlling the externally input reset signal, before the voltage falls below the operating range. The range of operating voltage varies with the setting of the user option byte (000C2H or 010C2H).

<R> **Remarks 1.** For details on the LVD circuit, see **3. 21 Voltage Detector**.

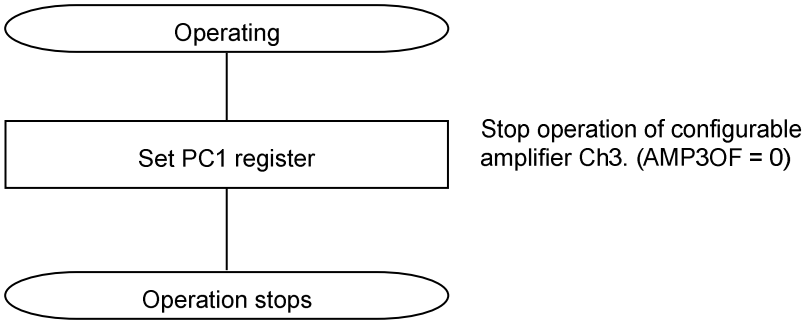
2. The detection voltage is a typical value. For details, see **5. 2. 5. 4 LVD circuit characteristics.**

Example of procedure for starting configurable amplifier Ch3 (non-inverting amplifier)

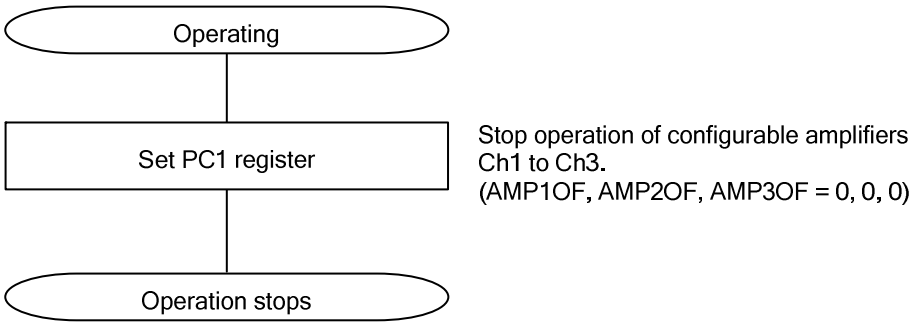


Remark *: don't care

Example of procedure for stopping configurable amplifier Ch3 (non-inverting amplifier)



Example of procedure for stopping configurable amplifiers (instrumentation amplifier)



4. 6. 3 Registers controlling the temperature sensor

The temperature sensor is controlled by power control register 2 (PC2).

(1) Power control register 2 (PC2)

This register is used to enable or disable operation of the gain adjustment amplifier, the low-pass filter, the high-pass filter, the variable output voltage regulator, the reference voltage generator, and the temperature sensor. Use this register to stop unused functions to reduce power consumption and noise.

When selecting the signal to be input to the temperature sensor, be sure to set bit 0 to 1.

Reset signal input clears this register to 00H.

- 64-pin products

Address: 12H After reset: 00 R/W

	7	6	5	4	3	2	1	0
PC2	0	0	0	GAINOF	LPFOF	0	LDOOF	TEMPOF

TEMPOF	Operation of temperature sensor
0	Stop operation of the temperature sensor.
1	Enable operation of the temperature sensor.

Caution Be sure to clear bit 2 to “0”.

Remark Bits 7 to 5 can be set to 1, but this has no effect on the function.

- 80-pin products

Address: 12H After reset: 00 R/W

	7	6	5	4	3	2	1	0
PC2	0	0	0	GAINOF	LPFOF	HPFOF	LDOOF	TEMPOF

TEMPOF	Operation of temperature sensor
0	Stop operation of the temperature sensor.
1	Enable operation of the temperature sensor.

Remark Bits 7 to 5 can be set to 1, but this has no effect on the function.

<R> **(2) Communication between devices at same potential (CSI mode) (master mode, SCKp ... internal clock output corresponding CSI00 only)**

(T_A = –40 to +85°C, 2.7 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions	HS Note 1		LS Note 2		LV Note 3		Unit
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
SCKp cycle time	t_{KCY1}	2.7 V ≤ V_{DD} ≤ 5.5 V t_{KCY1} ≥ 2/f_{CLK}	83.3 Note 4		250		500		ns
SCKp high-level width, low-level width	t_{KH1}, t_{KL1}	4.0 V ≤ V_{DD} ≤ 5.5 V	t_{KCY1}/2 -7		t_{KCY1}/2 -50		t_{KCY1}/2 -50		ns
		2.7 V ≤ V_{DD} ≤ 5.5 V	t_{KCY1}/2 -10		t_{KCY1}/2 -50		t_{KCY1}/2 -50		
Slp setup time (to SCKp↑) Note 5	t_{SIK1}	4.0 V ≤ V_{DD} ≤ 5.5 V	23		110		110		ns
		2.7 V ≤ V_{DD} ≤ 5.5 V	33		110		110		
Slp hold time (from SCKp↑) Note 5	t_{KSI1}	2.7 V ≤ V_{DD} ≤ 5.5 V	10		10		10		ns
Delay time from SCKp↓ to SOp output Note 6	t_{KSO1}	C = 20 pF Note 7		10		10		10	ns

<R> **Notes 1.** HS is condition of HS (high-speed main) mode.

2. LS is condition of LS (low-speed main) mode.

3. LV is condition of LV (low-voltage main) mode.

4. f_{MCK} must be 24 MHz or less.

5. This indicates the time when DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. When DAPmn = 0 and CKPmn = 1 or DAPmn = 1 and CKPmn = 0, this specification refers to SCKp↓.

6. This indicates the time when DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. When DAPmn = 0 and CKPmn = 1 or DAPmn = 1 and CKPmn = 0, this specification refers to SCKp↑.

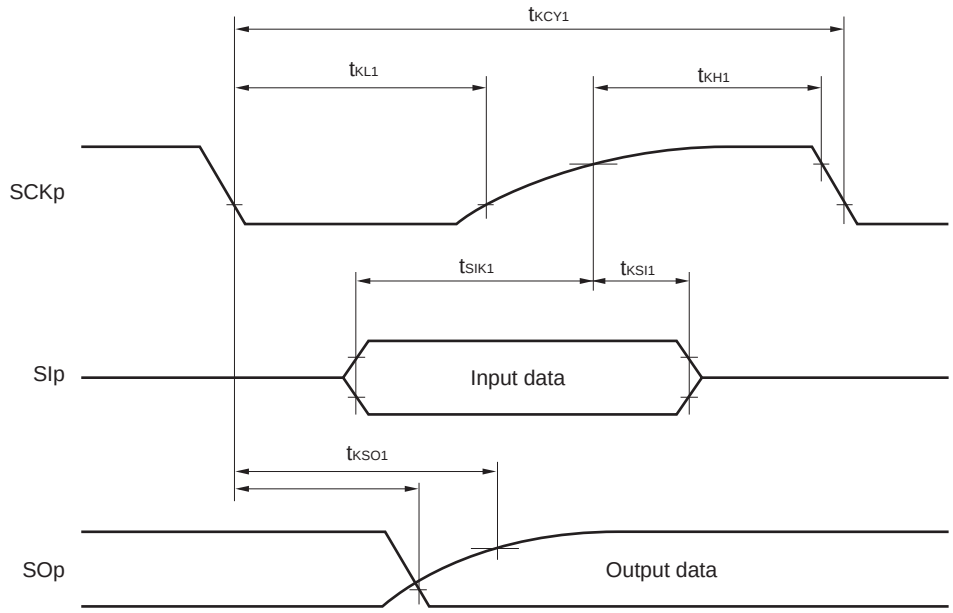
7. C is the load capacitance of the SCKp and SOp output lines.

Caution Select the normal input buffer for the SIp pin and the normal output mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg).

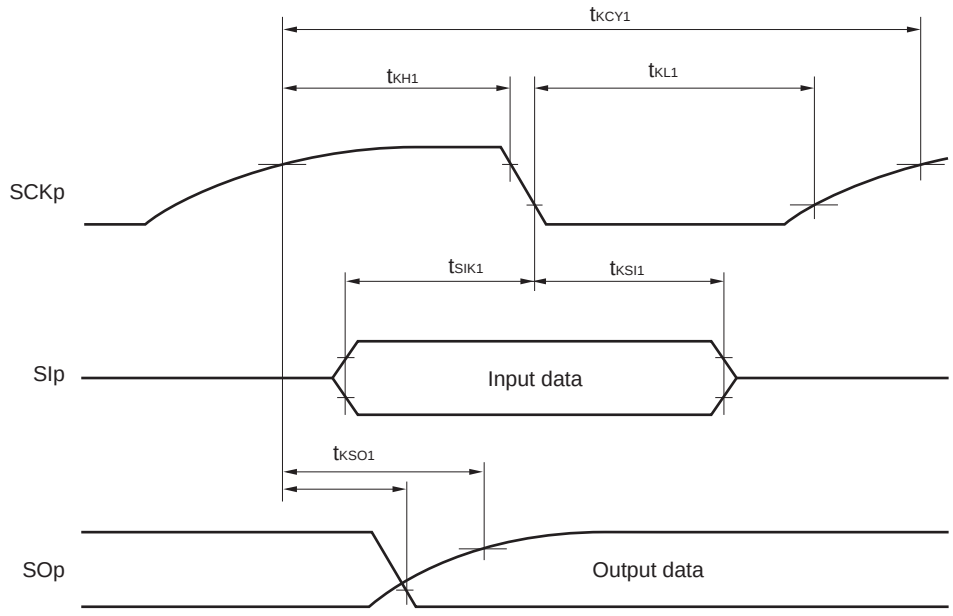
Remarks 1. p: CSI number (p = 00), m: Unit number (m = 0), n: Channel number (n = 0),
g: PIM and POM numbers (g = 1)

2. f_{MCK}: Serial array unit operating clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn).
m: Unit number, n: Channel number (mn = 00))

CSI mode serial transfer timing: master mode (during communication between devices at different potential)
(when DAPmn = 0 and CKPmn = 0 or DAPmn = 1 and CKPmn = 1)



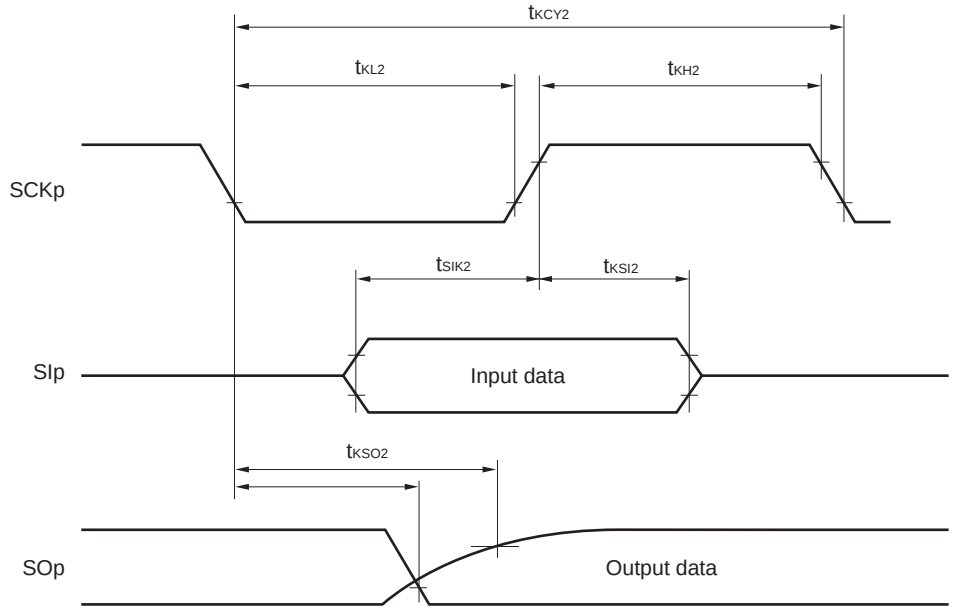
CSI mode serial transfer timing: master mode (during communication between devices at different potential)
(when DAPmn = 0 and CKPmn = 1 or DAPmn = 1 and CKPmn = 0)



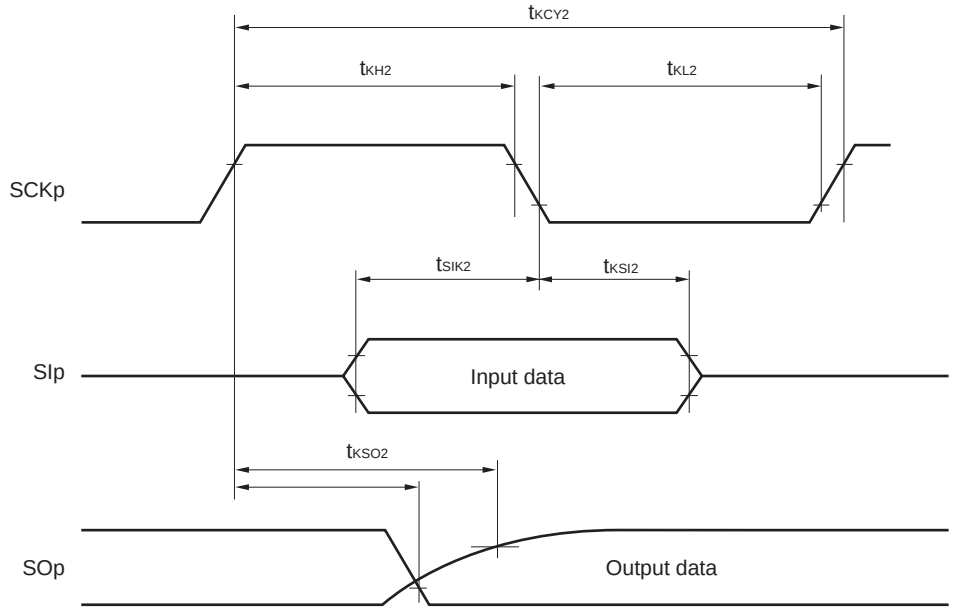
Remarks 1. p: CSI number (p = 00, 10, 20), m: Unit number, n: Channel number (mn = 00, 10, 20), g: PIM and POM numbers (g = 0, 1)

2. CSI21 cannot communicate with a device at different potential. Use other CSI channels for communication between devices at different potential.

CSI mode serial transfer timing: slave mode (during communication between devices at different potential)
(when DAPmn = 0 and CKPmn = 0 or DAPmn = 1 and CKPmn = 1)



CSI mode serial transfer timing: slave mode (during communication between devices at different potential)
(when DAPmn = 0 and CKPmn = 1 or DAPmn = 1 and CKPmn = 0)



Remarks 1. p: CSI number (p = 00, 10, 20), m: Unit number, n: Channel number (mn = 00, 10, 20),
g: PIM and POM numbers (g = 0, 1)

2. CSI21 cannot communicate with a device at different potential. Use other CSI channels for communication between devices at different potential.

B. 2 Revision History of Preceding Editions

Here is the revision history of the preceding editions. Chapter indicates the chapter of each edition.

(1/6)

Edition	Description	Chapter
Rev.1.00	The structure of **CHAPTERS** and **Sessions** are drastically changed.	Whole pages
	Modification of **1. 1 Features**	**CHAPTER 1 OUTLINE**
	Addition of Packaging, modification of Part Numbers and addition of **Cautions** in **1. 2 List of Part Numbers**	
	Modification of **Note 7.** for 64-pin products in **1. 3 Pin Configuration**	
	Modification of **Note 6.** for 80-pin products in **1. 3 Pin Configuration**	
	Addition of Items and **Notes** in **1. 6 Outline of Functions**	
	Error correction of the descriptions in **1. 6 Outline of Functions**	
	Modification of the tables for **Comparison of port functions with RL78/G1A** in **2. 1 Pin Functions in Microcontroller Block**	**CHAPTER 2 PIN FUNCTIONS**
	Error correction of the descriptions in **2. 1. 1 Port functions**	
	Addition of the descriptions in **2. 1. 2 Functions other than port Functions**	
	Error correction of the descriptions in **2. 2 Pin Functions in Analog Block**	
	Addition of **Notes** about the pin of $\overline{\text{ARESET}}$ in **2. 3 Recommended Connection of Unused Pins**	
	Addition of the descriptions for the pin of $\overline{\text{RESET}}$ and the pin of $\overline{\text{ARESET}}$ in **2. 5 Instruction of Pin Functions**	
	Addition of the items listed on the tables in **3. 2 Comparison of Each Function with RL78/G1A (64-pin products)**	**CHAPTER 3 MICROCONTROLLER BLOCK**
	Error correction of the descriptions on the tables in **3. 2 Comparison of Each Function with RL78/G1A (64-pin products)**	
	Modification of the tables for **List of Differences in Special Function Registers (SFRs)** in **3. 3. 2. 4 Special function registers (SFRs)**	
	Modification of the tables for **List of Differences in Expanded Special Function Registers (2nd SFRs)** in **3. 3. 2. 5 Expanded special function registers (2nd SFRs)**	
	Addition of the descriptions for each port in **3. 4. 2 Port configuration**	
	Error correction of the descriptions for each port in **3. 4. 2 Port configuration**	
	Addition of registers listed in **3. 4. 3 Registers controlling port functions**	
	Modification of the frequency for oscillation about the function of high-speed on-chip oscillator and addition of the table about the frequency for oscillation in **3. 5. 1 Functions of clock generator**	
	Addition of the registers listed in **3. 5. 3 Registers controlling clock generator**	
	Error correction of the descriptions about a crystal resonator in **3. 5. 7 Resonator and oscillator constants**	
	Addition of “Port mode control register” to **Table 3-8.**	
	Modification of the figures for Block Diagram on **Figure 3-4.** and **Figure 3-5.** in **3. 6. 2 Configuration of timer array unit**	
	Addition of the registers listed in **3. 6. 3 Registers controlling timer array unit**	
	Addition of the registers listed in **3. 8. 3 Registers controlling 12-bit interval timer**	