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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	RL78
Core Size	16-Bit
Speed	32MHz
Connectivity	CSI, I²C, LINbus, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	26
Program Memory Size	48KB (48K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	3K x 8
Voltage - Supply (Vcc/Vdd)	1.6V ~ 5.5V
Data Converters	A/D 17x8/12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	80-LQFP
Supplier Device Package	80-LFQFP (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f10fmdafb-v0

Table 1-1 Outline of Functions (Microcontroller Block) (2/2)

Item		64-pin products	80-pin products
		R5F10FLx	R5F10FMx
Serial interface		• 64-pin products CSI: 1 channel / simplified I^2C: 1 channel / UART: 1 channel UART: 1 channel CSI: 1 channel / UART (LIN-bus supported): 1 channel • 80-pin products CSI: 1 channel / simplified I^2C: 1 channel / UART: 1 channel CSI: 1 channel / simplified I^2C: 1 channel / UART: 1 channel CSI: 2 channels / simplified I^2C: 1 channel / UART (LIN-bus supported): 1 channel	
	I^2C bus	–	
Multiplier and divider / multiply accumulator		Multiplier: 16 bits × 16 bits (Unsigned or signed) Divider: 32 bits ÷ 32 bits (Unsigned) Multiply accumulator: 16 bits × 16 bits + 32 bits (Unsigned or signed)	
DMA controller		2 channels	
Vectored interrupt sources	Internal	25	
	External	2	5
Key interrupt		4 ch (7) Note 1	4 ch (8) Note 1
Reset		• Reset by $\overline{\text{RESET}}$ pin • Internal reset by watchdog timer • Internal reset by power-on-reset • Internal reset by voltage detector • Internal reset by illegal instruction execution Note 2 • Internal reset by RAM parity error • Internal reset by illegal-memory access	
Power-on-reset circuit		• Power-on-reset: 1.51 ±0.03 V • Power-down-reset: 1.50 ±0.03 V	
Voltage detector		Detection level: 3 stages	
On-chip debug function		Provided	

<R>

Notes 1. The number in parentheses is the channels of key interrupt when using the peripheral I/O redirection register (PIOR).

2. The illegal instruction is generated when instruction code FFH is executed. Rest by the illegal instruction execution is not issued by emulation with the in-circuit emulator or on-chip debug emulator.

Table 3-2. List of Differences in Special Function Registers (SFRs) (3/4)

Address	RL78/G1E (80-pin products)		RL78/G1A (64-pin products)	
	SFRs Name	Symbol	SFRs Name	Symbol
FFF90H	Same as RL78/G1A (64-pin products)	ITMC	Interval timer control register	ITMC
FFF91H				
FFF92H			Second count register	SEC
FFF93H			Minute count register	MIN
FFF94H			Hour count register	HOUR
FFF95H			Week count register	WEEK
FFF96H			Day count register	DAY
FFF97H			Month count register	MONTH
FFF98H			Year count register	YEAR
FFF99H			Watch error correction register	SUBCUD
FFF9AH			Alarm minute register	ALARMWM
FFF9BH			Alarm hour register	ALARMWH
FFF9CH			Alarm week register	ALARMWW
FFF9DH			Real-time clock control register 0	RTCC0
FFF9EH			Real-time clock control register 1	RTCC1
FFFA0H	Clock operation mode control register Note	CMC	Clock operation mode control register	CMC
FFFA1H	Clock operation status control register Note	CSC	Clock operation status control register	CSC
FFFA2H	Same as RL78/G1A (64-pin products)	OSTC	Oscillation stabilization time counter status register	OSTC
FFFA3H	Same as RL78/G1A (64-pin products)	OSTS	Oscillation stabilization time select register	OSTS
FFFA4H	System clock control register Note	CKC	System clock control register	CKC
FFFA5H	Clock output select register 0 Note	CKS0	Clock output select register 0	CKS0
FFFA6H			Clock output select register 1	CKS1
FFFA8H	Same as RL78/G1A (64-pin products)	RESF	Reset control flag register	RESF
FFFA9H	Same as RL78/G1A (64-pin products)	LVIM	Voltage detection register	LVIM
FFFAAH	Same as RL78/G1A (64-pin products)	LVIS	Voltage detection level register	LVIS
FFFABH	Same as RL78/G1A (64-pin products)	WDTE	Watchdog timer enable register	WDTE
FFFACH	Same as RL78/G1A (64-pin products)	CRCIN	CRC input register	CRCIN

Note The bit setting is different from that of RL78/G1A (64-pin products).

Caution Do not write data to the registers which is in the row with painted gray.

Table 3-4. List of Differences in Expanded Special Function Registers (2nd SFRs) (4/6)

Address	RL78/G1E (80-pin products)			RL78/G1A (64-pin products)		
	2nd SFRs Name	Symbol		2nd SFRs Name	Symbol	
F0148H	Same as RL78/G1A (64-pin products)	SIR10L	SIR10	Serial flag clear trigger register 10	SIR10L	SIR10
F0149H		—			—	
F014AH	Same as RL78/G1A (64-pin products)	SIR11L	SIR11	Serial flag clear trigger register 11	SIR11L	SIR11
F014BH		—			—	
F0150H	Same as RL78/G1A (64-pin products)	SMR10		Serial mode register 10	SMR10	
F0151H						
F0152H	Serial mode register 11 Note	SMR11		Serial mode register 11	SMR11	
F0153H						
F0158H	Same as RL78/G1A (64-pin products)	SCR10		Serial communication operation setting register 10	SCR10	
F0159H						
F015AH	Serial communication operation setting register 11 Note	SCR11		Serial communication operation setting register 11	SCR11	
F015BH						
F0160H	Same as RL78/G1A (64-pin products)	SE1L	SE1	Serial channel enable status register 1	SE1L	SE1
F0161H		—			—	
F0162H	Same as RL78/G1A (64-pin products)	SS1L	SS1	Serial channel start register 1	SS1L	SS1
F0163H		—			—	
F0164H	Same as RL78/G1A (64-pin products)	ST1L	ST1	Serial channel stop register 1	ST1L	ST1
F0165H		—			—	
F0166H	Same as RL78/G1A (64-pin products)	SPS1L	SPS1	Serial clock select register 1	SPS1L	SPS1
F0167H		—			—	
F0168H	Same as RL78/G1A (64-pin products)	SO1		Serial output register 1	SO1	
F0169H						
F016AH	Same as RL78/G1A (64-pin products)	SOE1L	SOE1	Serial output enable register 1	SOE1L	SOE1
F016BH		—			—	
F0174H	Same as RL78/G1A (64-pin products)	SOL1L	SOL1	Serial output level register 1	SOL1L	SOL1
F0175H		—			—	

Note The bit setting is different from that of RL78/G1A (64-pin products).

3. 3. 3 Instruction address addressing

See **3. 3 Instruction Address Addressing** in **RL78/G1A Hardware User's Manual (R01UH0305E)**.

3. 3. 4 Addressing for processing data addresses

See **3. 4 Addressing for Processing Data Addresses** in **RL78/G1A Hardware User's Manual (R01UH0305E)**.

3. 4 Port Functions

In this section, the differences of the functions and registers from RL78/G1A (64-pin products) are described. For details, see **CHAPTER 4 PORT FUNCTIONS** in **RL78/G1A Hardware User's Manual (R01UH0305E)**.

3. 4. 1 Port functions

The RL78/G1E microcontrollers (64-pin products, 80-pin products) are provided with digital I/O ports, which enable variety of control operations. In addition to the function as digital I/O ports, these ports have several alternate functions. For details of the alternate functions, see **CHAPTER 2 PIN FUNCTIONS**.

3. 4. 2 Port configuration

Ports include the following hardware.

Table 3-5. Port Configuration

Item	Configuration
Control registers	Port mode registers (PM0 to PM2, PM4 to PM7, PM14, PM15) Port registers (P0 to P2, P4, P5, P7, P12 to P14) Pull-up resistor option registers (PU0, PU1, PU4, PU5, PU7, PU14) Port input mode registers (PIM0, PIM1) Port output mode registers (POM0, POM1, POM5) Port mode control registers (PMC0, PMC1, PMC3, PMC5, PMC7) A/D port configuration register (ADPC) Peripheral I/O redirection register (PIOR) Global analog input disable register (GAIDIS)
Port	· 64-pin products Total: 24 (CMOS I/O: 20, CMOS input: 3, CMOS output: 1) · 80-pin products Total: 30 (CMOS I/O: 26, CMOS input: 3, CMOS output: 1)
Pull-up resistor	· 64-pin products Total: 16 · 80-pin products Total: 21

For details of each port, also see **4. 2 Port Configuration** in **RL78/G1A Hardware User's Manual (R01UH0305E)**.

(2) 80-pin products

Address: F0076H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
ADPC	0	0	0	0	0	ADPC2	ADPC1	ADPC0

ADPC2	ADPC1	ADPC0	Analog input (A)/digital I/O (D) switching				
			ANI4/P24	ANI3/P23	ANI2/P22	ANI1/P21	ANI0/P20
0	0	0	A	A	A	A	A
0	0	1	D	D	D	D	D
0	1	0	D	D	D	D	A
0	1	1	D	D	D	A	A
1	0	0	D	D	A	A	A
1	0	1	D	A	A	A	A
Other than above			Setting prohibited				

Cautions 1. Be sure to clear bits 3 to 7 to "0".

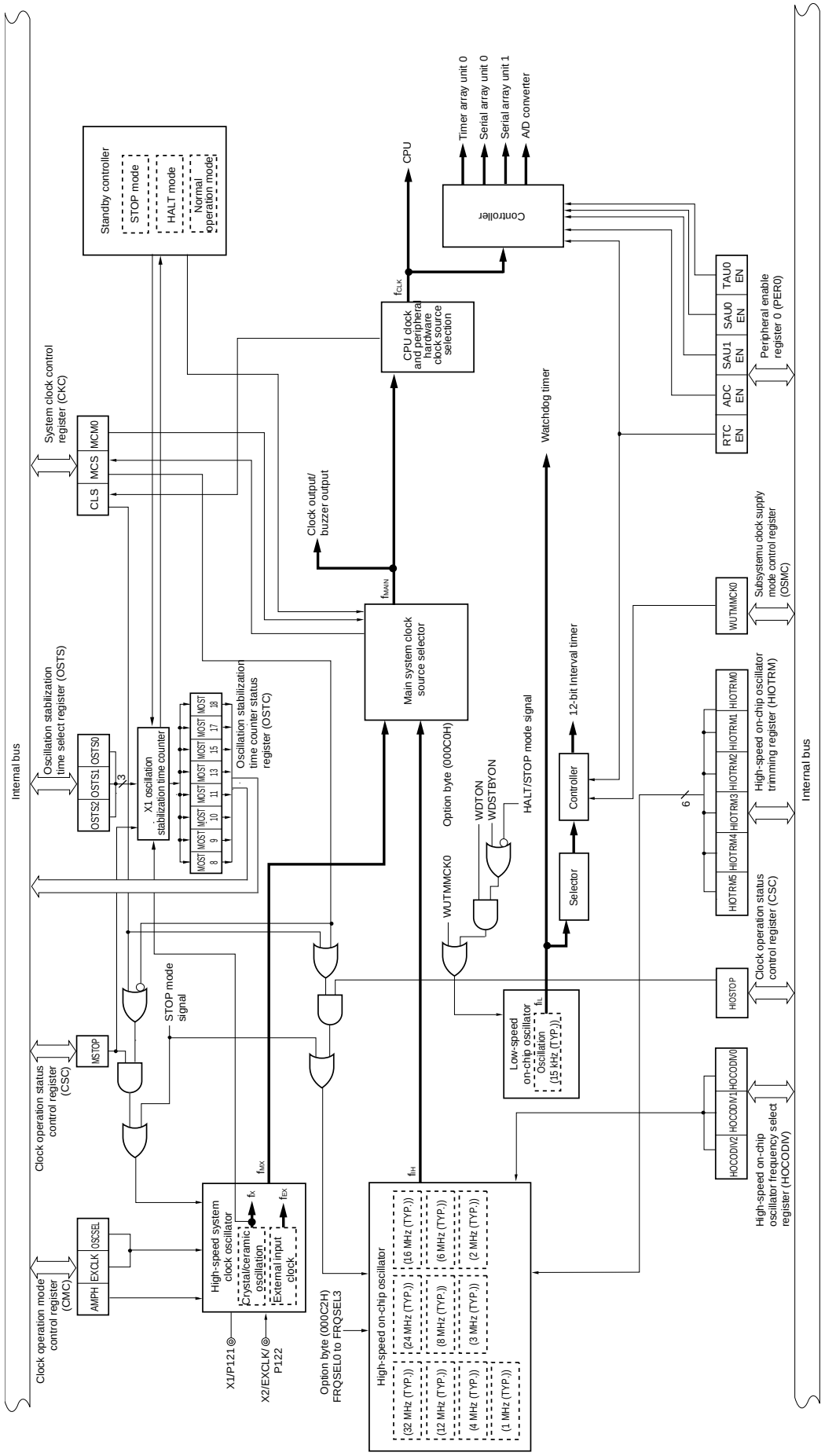
2. Set the channel used for A/D conversion to the input mode by using port mode register 2 (PM2).

3. Do not set the pin set by the ADPC register as digital I/O by the analog input channel specification register (ADS).

4. When using AV_{REFP} and AV_{REFM}, specify ANI0 and ANI1 as the analog input channels and specify input mode by using the port mode register.

Figure 3-1. Block Diagram of Clock Generator

<R>



(**Remark** is listed on the next page)

Remark f_X: X1 clock oscillation frequency
f_{IH}: High-speed on-chip oscillator clock frequency
f_{EX}: External main system clock frequency
f_{MX}: High-speed system clock frequency
f_{MAIN}: Main system clock frequency
f_{CLK}: CPU/peripheral hardware clock frequency
f_{IL}: Low-speed on-chip oscillator clock frequency

3. 6. 2. 1 Timer count register mn (TCRmn)

The bit setting is same as that of RL78/G1A (64-pin products). For details, see **6. 2. 1 Timer count register mn (TCRmn)** in **RL78/G1A Hardware User's Manual (R01UH0305E)**.

3. 6. 2. 2 Timer data register mn (TDRmn)

The bit setting is same as that of RL78/G1A (64-pin products). For details, see **6. 2. 2 Timer data register mn (TDRmn)** in **RL78/G1A Hardware User's Manual (R01UH0305E)**.

- Format of Timer Mode Register mn (TMRmn) (2/4)

Address: F0190H, F0191H (TMR00) - F019EH, F019FH (TMR07) After reset: 0000H R/W

Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TMRmn (n = 2, 4, 6)	CKS mn1	CKS mn0	0	CCS mn	MASTER mn	STS mn2	STS mn1	STS mn0	CIS mn1	CIS mn0	0	0	MD mn3	MD mn2	MD mn1	MD mn0

Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TMRmn (n = 1, 3)	CKS mn1	CKS mn0	0	CCS mn	SPLIT mn	STS mn2	STS mn1	STS mn0	CIS mn1	CIS mn0	0	0	MD mn3	MD mn2	MD mn1	MD mn0

Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TMRmn (n = 0, 5, 7)	CKS mn1	CKS mn0	0	CCS mn	0[Note]	STS mn2	STS mn1	STS mn0	CIS mn1	CIS mn0	0	0	MD mn3	MD mn2	MD mn1	MD mn0

Bit 11 of TMRmn (n = 2, 4, 6)

MASTER mn	Selection between using channel n independently or simultaneously with another channel (as a slave or master)
0	Operates in independent channel operation function or as slave channel in simultaneous channel operation function.
1	Operates as master channel in simultaneous channel operation function.
Only the channel 2, 4, 6 can be set as a master channel (MASTERmn = 1). Be sure to use channel 0, 5, 7 are fixed to 0 (Regardless of the bit setting, channel 0 operates as master, because it is the highest channel). Clear the MASTERmn bit to 0 for a channel that is used with the independent channel operation function.	

Bit 11 of TMRmn (n = 1, 3)

SPLITmn	Selection of 8 or 16-bit timer operation for channels 1 and 3
0	Operates as 16-bit timer. (Operates in independent channel operation function or as slave channel in simultaneous channel operation function.)
1	Operates as 8-bit timer.

STS mn2	STS mn1	STS mn0	Setting of start trigger or capture trigger of channel n
0	0	0	Only software trigger start is valid (other trigger sources are unselected).
0	0	1	Valid edge of the TImn pin input is used as both the start trigger and capture trigger.
0	1	0	Both the edges of the TImn pin input are used as a start trigger and a capture trigger.
1	0	0	Interrupt signal of the master channel is used (when the channel is used as a slave channel with the simultaneous channel operation function).
Other than above			Setting prohibited

<R> **Note** Bit 11 is fixed at 0 of read only, write is ignored.

Remark m: Unit number (m = 0), n: Channel number (n = 0 to 7 (however, timer input pin (TImn), timer output pin (TOmn): n = 0, 4, 7))

Table 3-13. Interrupt Source List (3/3)

Interrupt Type	Default Priority[Note 1]	Interrupt Source		Internal/External	Vector Table Address	Basic Configuration Type[Note 2]	RL78/G1E	
		Name	Trigger				64-pin	80-pin
Maskable	29	INTTM05	End of timer channel 5 count or capture	Internal	0044H	(A)	√	√
	30	INTTM06	End of timer channel 6 count or capture		0046H		√	√
	31	INTTM07	End of timer channel 7 count or capture		0048H		√	√
	32	INTP6	Pin input edge detection	External	004AH	(B)	–	√
	33	INTP7			004CH		–	–
	34	INTP8			004EH		–	–
	35	INTP9			0050H		–	–
	36	INTP10			0052H		–	–
	37	INTP11			0054H		–	–
<R>	38	INTMD	End of division operation/Overflow of multiplyaccumulation result occurs	Internal	005EH	(A)	√	√
	39	INTFL	Reserved[Note 3]		0062H		√	√
Software	–	BRK	Execution of BRK instruction	–	007EH	(D)	√	√
Reset	–	RESET	$\overline{\text{RESET}}$ pin input	–	0000H	–	√	√
		POR	Power-on-reset				√	√
		LVD	Voltage detection[Note 4]				√	√
		WDT	Overflow of watchdog timer				√	√
		TRAP	Execution of illegal instruction[Note 5]				√	√
		IAW	Illegal-memory access				√	√
		RAMTOP	RAM parity error				√	√

Notes 1. The default priority determines the sequence of interrupts if two or more maskable interrupts occur simultaneously. Zero indicates the highest priority and 39 indicates the lowest priority.

2. Basic configuration types (A) to (D) correspond to (A) to (D) in Figure 3-13.

<R> **3.** Be used at the flash self programming library or the data flash library.

4. When bit 7 (LVIMD) of the voltage detection level register (LVIS) is set to 1.

5. When the instruction code in FFH is executed.
Reset by the illegal instruction execution not issued by emulation with the in-circuit emulator or on-chip debug emulator.

3. 26 On-chip Debug Function

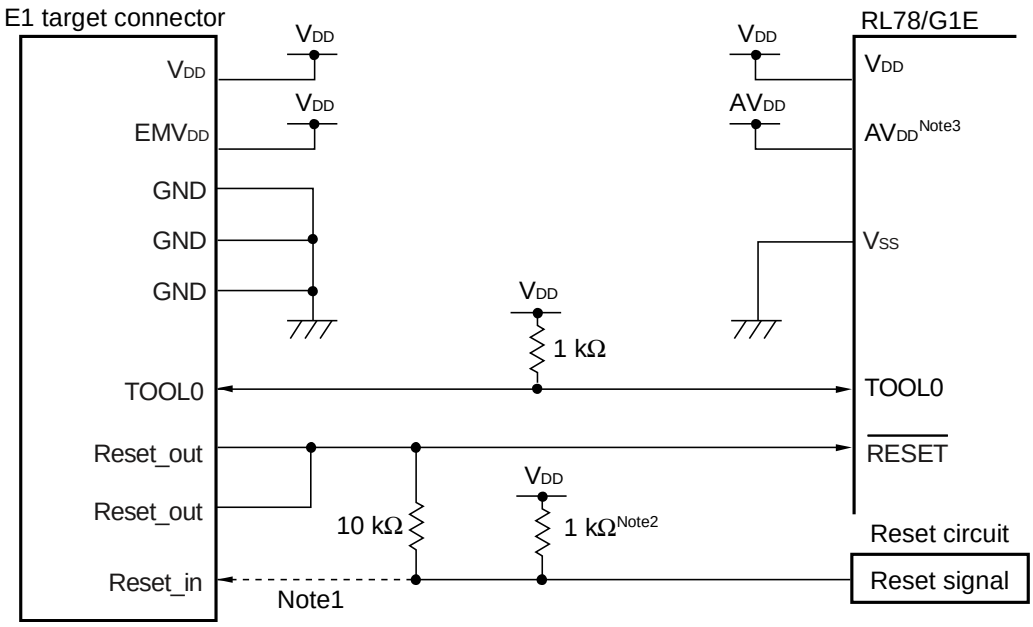
3. 26. 1 Connecting E1 on-chip debugging emulator to RL78/G1E

The RL78/G1A uses the V_{DD}, $\overline{RESET}$, TOOL0, and V_{SS} pins to communicate with the host machine via an E1 on-chip debugging emulator. Serial communication is performed by using a single-line UART that uses the TOOL0 pin.

Caution The RL78/G1E has an on-chip debug function, which is provided for development and evaluation. Do not use the on-chip debug function in products designated for mass production, because the guaranteed number of rewritable times of the flash memory may be exceeded when this function is used, and product reliability therefore cannot be guaranteed. Renesas Electronics is not liable for problems occurring when the on-chip debug function is used.

Figure 3-16. Connection Example of E1 On-chip Debugging Emulator and RL78/G1E

<R>



Notes 1. Connecting the dotted line is not necessary during serial flash programming..

2. If the reset circuit on the target system does not have a buffer and generates a reset signal only with resistors and capacitors, this pull-up resistor is not necessary.

3. $AV_{DD} \leq 3.6$ V.

Cautions 1. This circuit diagram is assumed that the reset signal outputs from an N-ch open drain buffer (output resistor: 100 Ω or less).

2. For the details of $\overline{ARESET}$ pin, see 2. 5. 31 $\overline{ARESET}$.

(9) Power control register 1 (PC1)

This register is used to enable or disable operation of the configurable amplifiers and the D/A converters.

Use this register to stop unused functions to reduce power consumption and noise.

When using one of configurable amplifier channels Ch1 to Ch3, be sure to set the control bit that corresponds to the channel (bits 0 to 2) to 1.

Reset signal input clears this register to 00H.

Address: 11H After reset: 00H R/W

	7	6	5	4	3	2	1	0
PC1	DAC4OF	DAC3OF	DAC2OF	DAC1OF	0	AMP3OF	AMP2OF	AMP1OF

AMP3OF	Operation of configurable amplifier Ch3
0	Stop operation of configurable amplifier Ch3.
1	Enable operation of configurable amplifier Ch3.

AMP2OF	Operation of configurable amplifier Ch2
0	Stop operation of configurable amplifier Ch2.
1	Enable operation of configurable amplifier Ch2.

AMP1OF	Operation of configurable amplifier Ch1
0	Stop operation of configurable amplifier Ch1.
1	Enable operation of configurable amplifier Ch1.

Caution Be sure to clear bit 3 to "0".

4. 5. 3 Registers controlling the high-pass filter

<R> The high-pass filter is controlled by the following 2 registers:

- MPX setting register 3 (MPX3)
- Power control register 2 (PC2)

(1) MPX setting register 3 (MPX3)

This register is used to control MPX7, MPX9, MPX10, and MPX11.

<R> When selecting the signal to be input to the filter circuits, use bits 5 and 4. When switching the order in which signals are processed by the low-pass and high-pass filters, use bit 3.

- 80-pin products

Address: 05H After reset: 00H R/W

	7	6	5	4	3	2	1	0
MPX3	0	0	SCF2	SCF1	SCF0	MPX72	MPX71	MPX70

<R>

SCF2	SCF1	Source of input to filter circuits
0	0	SC_IN pin
0	1	MPX7 output signal
1	0	Gain adjustment amplifier output signal
1	1	Setting prohibited

SCF0	Specification of the order of filter signal processing
0	The MPX9 output signal passes the low-pass filter and then is input to the high-pass filter.
1	The MPX9 output signal passes the high-pass filter and then is input to the low-pass filter.

Remark Bits 7 and 6 are fixed at 0 of read only.

4. 9. 2 SPI communication

The SPI transmits and receives data in 16-bit units. Data can be transmitted and received when $\overline{CS}$ is low. Data is transmitted one bit at a time in synchronization with the falling edge of the serial clock, and is received one bit at a time in synchronization with the rising edge of the serial clock. When the R/W bit is 1, data is written to the SPI control register in accordance with the address/data setting after the 16th rising edge of $\overline{SCLK}$ has been detected following the fall of $\overline{CS}$, and the operation specified by the data is executed. When the R/W bit is 0, the data is output from the register in accordance with the address/data setting in synchronization with the 9th and later falling edges of $\overline{SCLK}$ following the fall of $\overline{CS}$.

Figure 4-5. SPI Communication Timing

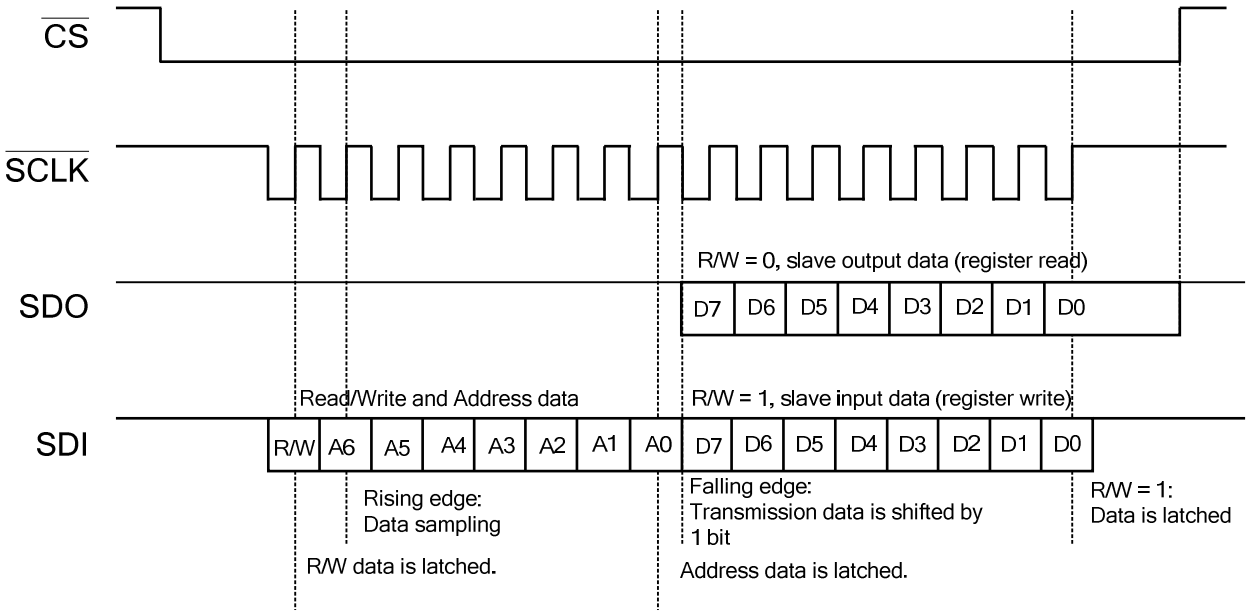


Table 4-14. Pin Statuses after Analog Reset

Pin Name	External Reset from $\overline{\text{ARESET}}$ Pin	Internal Reset by Reset Control Register (RC)
SC_IN	Hi-Z	Hi-Z
CLK_SYNCH	Pull-down input	Pull-down input
SYNCH_OUT	Hi-Z	Hi-Z
GAINAMP_OUT	Hi-Z	Hi-Z
GAINAMP_IN	Hi-Z	Hi-Z
MPXIN61	Hi-Z	Hi-Z
MPXIN51	Hi-Z	Hi-Z
MPXIN60	Hi-Z	Hi-Z
MPXIN50	Hi-Z	Hi-Z
AMP3_OUT	Hi-Z	Hi-Z
DAC3_OUT/VREFIN3	Pull-down input	Pull-down input
AMP2_OUT	Hi-Z	Hi-Z
AMP1_OUT	Hi-Z	Hi-Z
DAC2_OUT/VREFIN2	Pull-down input	Pull-down input
DAC1_OUT/VREFIN1	Pull-down input	Pull-down input
MPXIN41	Hi-Z	Hi-Z
MPXIN31	Hi-Z	Hi-Z
MPXIN40	Hi-Z	Hi-Z
MPXIN30	Hi-Z	Hi-Z
MPXIN21	Hi-Z	Hi-Z
MPXIN11	Hi-Z	Hi-Z
MPXIN20	Hi-Z	Hi-Z
MPXIN10	Hi-Z	Hi-Z
BGR_OUT	Pull down	Pull down
LDO_OUT	Pull down	Pull down
TEMP_OUT	Pull down	Pull down
$\overline{\text{SCLK}}$	Hi-Z	Pull-up input
SDO	Hi-Z (open drain)	Hi-Z (open drain)
SDI	Hi-Z	Pull-up input
$\overline{\text{CS}}$	Hi-Z	Pull-up input
<R> DAC4_OUT/VREFIN4	Pull-down input	Pull-down input
HPF_OUT	Hi-Z	Hi-Z
CLK_HPF	Pull-down input	Pull-down input
CLK_LPF	Pull-down input	Pull-down input
LPF_OUT	Hi-Z	Hi-Z

<R> **(3) Communication between devices at same potenntial (CSI mode) (master mode, SCKp ... internal clock output)**

(T_A = –40 to +85°C, 1.6 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions	HS Note 1		LS Note 2		LV Note 3		Unit
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
SCKp cycle time	t_{KCY1}	2.7 V ≤ V_{DD} ≤ 5.5 V t_{KCY1} ≥ 4/f_{CLK}	125		500		1000		ns
		2.4 V ≤ V_{DD} ≤ 5.5 V t_{KCY1} ≥ 4/f_{CLK}	250		500		1000		ns
		1.8 V ≤ V_{DD} ≤ 5.5 V t_{KCY1} ≥ 4/f_{CLK}	500		500		1000		ns
		1.7 V ≤ V_{DD} ≤ 5.5 V t_{KCY1} ≥ 4/f_{CLK}	1000		1000		1000		ns
		1.6 V ≤ V_{DD} ≤ 5.5 V t_{KCY1} ≥ 4/f_{CLK}	–		1000		1000		ns
SCKp high-level width low-level width	t_{KH1}, t_{KL1}	4.0 V ≤ V_{DD} ≤ 5.5 V	t_{KCY1}/2 -12		t_{KCY1}/2 -50		t_{KCY1}/2 -50		ns
		2.7 V ≤ V_{DD} ≤ 5.5 V	t_{KCY1}/2 -18		t_{KCY1}/2 -50		t_{KCY1}/2 -50		ns
		2.4 V ≤ V_{DD} ≤ 5.5 V	t_{KCY1}/2 -38		t_{KCY1}/2 -50		t_{KCY1}/2 -50		ns
		1.8 V ≤ V_{DD} ≤ 5.5 V	t_{KCY1}/2 -50		t_{KCY1}/2 -50		t_{KCY1}/2 -50		ns
		1.7 V ≤ V_{DD} ≤ 5.5 V	t_{KCY1}/2 -100		t_{KCY1}/2 -100		t_{KCY1}/2 -100		ns
		1.6 V ≤ V_{DD} ≤ 5.5 V	–		t_{KCY1}/2 -100		t_{KCY1}/2 -100		ns
<R> Slp setup time (to SCKp↑) Note 4	t_{SIK1}	4.0 V ≤ V_{DD} ≤ 5.5 V	44		110		110		ns
		2.7 V ≤ V_{DD} ≤ 5.5 V	44		110		110		ns
		2.4 V ≤ V_{DD} ≤ 5.5 V	75		110		110		ns
		1.8 V ≤ V_{DD} ≤ 5.5 V	110		110		110		ns
		1.7 V ≤ V_{DD} ≤ 5.5 V	220		220		220		ns
		1.6 V ≤ V_{DD} ≤ 5.5 V	–		220		220		ns
Slp hold time (from SCKp↑) Note 4	t_{KSI1}	1.7 V ≤ V_{DD} ≤ 5.5 V	19		19		19		ns
		1.6 V ≤ V_{DD} ≤ 5.5 V	–		19		19		
Slp hold time (from SCKp↑) Note 5	t_{KSO1}	1.7 V ≤ V_{DD} ≤ 5.5 V C = 30 pF Note 6		25		25		25	ns
		1.6 V ≤ V_{DD} ≤ 5.5 V C = 30 pF Note 6		–		25		25	

(**Notes Caution** and **Remark** are listed on the next page.)

<R> **(6) Communication between devices at different potential (1.8 V, 2.5 V or 3 V) (UART mode) (output from dedicated baud rate generator) (2/2)**

(T_A = –40 to +85°C, 1.8 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V) (2/2)

Parameter	Symbol	Conditions		HS Note 1		LS Note 2		LV Note 3		Unit
				MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Transfer rate		Transmission	4.0V ≤ V_{DD} ≤ 5.5V, 2.7V ≤ Vb ≤ 4.0V		**Note 4**		**Note 4**		**Note 4**	bps
			Theoretical value of the maximum transfer rate: Cb = 50 pF, Rb = 1.4 kΩ, Vb = 2.7 V		2.8 Note 5		2.8 Note 5		2.8 Note 5	Mbps
			2.7V ≤ V_{DD} < 4.0V, 2.3V ≤ Vb ≤ 2.7V		**Note 7**		**Note 7**		**Note 7**	bps
			Theoretical value of the maximum transfer rate: Cb = 50 pF, Rb = 2.7 kΩ, Vb = 2.3 V		1.2 Note 8		1.2 Note 8		1.2 Note 8	Mbps
			1.8V ≤ V_{DD} < 3.3V, 1.6V ≤ Vb ≤ 2.0V Note 5		**Note 9**		**Note 9**		**Note 9**	bps
			Theoretical value of the maximum transfer rate: Cb = 50 pF, Rb = 5.5 kΩ, Vb = 1.6 V		0.43 Note 10		0.43 Note 10		0.43 Note 10	Mbps

Notes 1. HS is condition of HS (high-speed main) mode.

2. LS is condition of LS (low-speed main) mode.

3. LV is condition of LV (low-voltage main) mode.

4. The smaller value derived by using f_{MCK}/6 or the following expression is the valid maximum transfer rate.
Expression for calculating the transfer rate when 4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ Vb ≤ 4.0 V

$$\text{Maximum transfer rate} = \frac{1}{\{-Cb \times Rb \times \ln(1 - \frac{2.2}{Vb})\} \times 3} \text{ [bps]}$$

$$\text{Baud rate error (theoretical value)} = \frac{\frac{1}{\text{Transfer rate} \times 2} - \{-Cb \times Rb \times \ln(1 - \frac{2.2}{Vb})\}}{(\frac{1}{\text{Transfer rate}}) \times \text{Number of transferred bits}} \times 100 \text{ [\%]}$$

* This value is the theoretical value of the relative difference between the transmission and reception sides.

(Other **Notes** and **Caution** are listed on the next page.)

5. 3. 3. 2 Gain adjustment amplifier characteristics

(1) 64-pin products

(–40°C ≤ T_A ≤ 85°C, AV_{DD1} = AV_{DD2} = AV_{DD3} = DV_{DD} = 5.0 V, VREFIN4 = 1.7 V, GAINOF = 1, DAC4OF = 0)

Parameter	Symbol	Conditions	Ratings			Unit
			MIN	TYP	MAX	
Current consumption	IccA		–	530	1,300	μA
Input voltage	VINL		AGND2 - 0.1	–	–	V
	VINH		–	–	AV_{DD1} - 0.05	V
Output voltage	VOUTL1	IOL = -100 μA	–	AGND2 + 0.02	AGND2 + 0.05	V
	VOUTH1	IOH = 100 μA	AV_{DD1} - 0.05	AV_{DD1} - 0.02	–	V
Gain bandwidth	GBW2	CL = 30 pF, GC4 = 11H (40 dB)	–	0.86	–	MHz
Input conversion offset voltage	VOFF	GC4 = 00H (6 dB), T_A = 25°C, GAINAMP_IN = 2.5 V	-30	–	30	mV
Input conversion offset voltage temperature coefficient	VOTC2	CLK_SYNCH = L, GAINAMP_OUT pin	–	±18	–	μV/°C
Slew rate	SR	CL = 30 pF	–	0.9	–	V/μs
Equivalent input noise	En_Gain	f = 1 kHz, GC4 = 11H (40 dB)	–	700	–	nV/√ Hz
Power supply rejection ratio	PSRR2	f = 1 kHz, GC4 = 00H (6 dB)	–	45	–	dB
Gain setting error	GAIN_Accu1	T_A = 25°C	-0.6	–	0.6	dB
	GAIN_Accu2	T_A = –40 to 85°C	-1.0	–	1.0	dB

5. 3. 3. 5 High-pass filter characteristics

($-40°C \le T_A \le 85°C$, $AV_{DD1} = AV_{DD2} = AV_{DD3} = AV_{DD4} = DV_{DD} = 5.0$ V, HPFOF = 1)

Parameter	Symbol	Conditions	Ratings			Unit
			MIN.	TYP.	MAX.	
Current consumption	IccA		–	800	1800	μA
Input voltage	V_{ILHPF}		AGND4 +0.2	–	–	V
	V_{IHHPF}		–	–	AV_{DD3} - 1.5	V
<R> Output voltage	V_{OLHPF}	IOL = –200 μA	–	AGND4 +0.22	AGND4 +0.25	V
	V_{OHHPF}	IOH = 200 μA	AV_{DD3} -1.55	AV_{DD3} -1.52	–	V
Cutoff frequency	fc1	f_{CLK_HPF} = 2 kHz	–	8	–	Hz
	fc2	f_{CLK_HPF} = 200 kHz	–	800	–	Hz
CLK_HPF low-level input voltage	V_{ILCLK_HPF}				$0.3 \times AV_{DD3}$	V
CLK_HPF high-level input voltage	V_{IHCLK_HPF}		$0.7 \times AV_{DD3}$			V
CLK_HPF Input frequency	f_{CLK_HPF}		2	–	200	kHz
CLK_HPF Input low-level-width Input high-level-width	t_{ILW_HPF} t_{IHW_HPF}		200	–	–	ns

Clock Timing