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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	RL78
Core Size	16-Bit
Speed	32MHz
Connectivity	CSI, I²C, LINbus, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	26
Program Memory Size	48KB (48K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	3K x 8
Voltage - Supply (Vcc/Vdd)	1.6V ~ 5.5V
Data Converters	A/D 17x8/12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	80-LQFP
Supplier Device Package	80-LFQFP (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f10fmdafb-x0

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2. 5. 3 Port 2 (P20 to P24)

(1) Port mode

P20 to P24 function as an I/O port. P20 to P24 can be set to input or output port in 1-bit units using port mode register 2 (PM2).

(2) Control mode

P20 to P24 function as A/D converter analog input, and reference voltage input.

(a) ANI0 to ANI4

These are the analog input pins of A/D converter.

(b) AV_{REFP}

This is a pin that inputs the A/D converter reference potential (+ side).

(c) AV_{REFM}

This is a pin that inputs the A/D converter reference potential (– side).

(d) KR5 to KR7

These are the key interrupt input pins.

Table 3-2. List of Differences in Special Function Registers (SFRs) (4/4)

Address	RL78/G1E (80-pin products)			RL78/G1A (64-pin products)		
	SFRs Name	Symbol		SFRs Name	Symbol	
FFFB0H	Same as RL78/G1A (64-pin products)	DSA0		DMA SFR address register 0	DSA0	
FFFB1H	Same as RL78/G1A (64-pin products)	DSA1		DMA SFR address register 1	DSA1	
FFFB2H	Same as RL78/G1A (64-pin products)	DRA0L	DRA0	DMA RAM address register 0L	DRA0L	DRA0
FFFB3H	Same as RL78/G1A (64-pin products)	DRA0H		DMA RAM address register 0H	DRA0H	
FFFB4H	Same as RL78/G1A (64-pin products)	DRA1L	DRA1	DMA RAM address register 1L	DRA1L	DRA1
FFFB5H	Same as RL78/G1A (64-pin products)	DRA1H		DMA RAM address register 1H	DRA1H	
FFFB6H	Same as RL78/G1A (64-pin products)	DBC0L	DBC0	DMA byte count register 0L	DBC0L	DBC0
FFFB7H	Same as RL78/G1A (64-pin products)	DBC0H		DMA byte count register 0H	DBC0H	
FFFB8H	Same as RL78/G1A (64-pin products)	DBC1L	DBC1	DMA byte count register 1L	DBC1L	DBC1
FFFB9H	Same as RL78/G1A (64-pin products)	DBC1H		DMA byte count register 1H	DBC1H	
FFFBAH	Same as RL78/G1A (64-pin products)	DMC0		DMA mode control register 0	DMC0	
FFFBBH	Same as RL78/G1A (64-pin products)	DMC1		DMA mode control register 1	DMC1	
FFFBCH	Same as RL78/G1A (64-pin products)	DRC0		DMA operation control register 0	DRC0	
FFFBDH	Same as RL78/G1A (64-pin products)	DRC1		DMA operation control register 1	DRC1	
FFFD0H	Interrupt mask flag register 2L Note	IF2L	IF2	Interrupt mask flag register 2L	IF2L	IF2
FFFD1H	Interrupt mask flag register 2H Note	IF2H		Interrupt mask flag register 2H	IF2H	
FFFD4H	Interrupt mask flag register 0L Note	MK2L	MK2	Interrupt mask flag register 0L	MK2L	MK2
FFFD5H	Interrupt mask flag register 2H Note	MK2H		Interrupt mask flag register 2H	MK2H	
FFFD8H	Priority specification flag register 02L Note	PR02L	PR02	Priority specification flag register 02L	PR02L	PR02
FFFD9H	Priority specification flag register 02H Note	PR02H		Priority specification flag register 02H	PR02H	
FFFDCH	Priority specification flag register 12L Note	PR12L	PR12	Priority specification flag register 12L	PR12L	PR12
FFFDDH	Priority specification flag register 12H Note	PR12H		Priority specification flag register 12H	PR12H	
FFFE0H	Interrupt mask flag register 0L Note	IF0L	IF0	Interrupt mask flag register 0L	IF0L	IF0
FFFE1H	Interrupt mask flag register 0H Note	IF0H		Interrupt mask flag register 0H	IF0H	
FFFE2H	Interrupt mask flag register 1L Note	IF1L	IF1	Interrupt mask flag register 1L	IF1L	IF1
FFFE3H	Interrupt mask flag register 1H Note	IF1H		Interrupt mask flag register 1H	IF1H	
FFFE4H	Interrupt mask flag register 0L Note	MK0L	MK0	Interrupt mask flag register 0L	MK0L	MK0
FFFE5H	Interrupt mask flag register 0H Note	MK0H		Interrupt mask flag register 0H	MK0H	
FFFE6H	Interrupt mask flag register 1L Note	MK1L	MK1	Interrupt mask flag register 1L	MK1L	MK1
FFFE7H	Interrupt mask flag register 1H Note	MK1H		Interrupt mask flag register 1H	MK1H	
FFFE8H	Priority specification flag register 00L Note	PR00L	PR00	Priority specification flag register 00L	PR00L	PR00
FFFE9H	Priority specification flag register 00H Note	PR00H		Priority specification flag register 00H	PR00H	
FFFEAH	Priority specification flag register 01L Note	PR01L	PR01	Priority specification flag register 01L	PR01L	PR01
FFFEBH	Priority specification flag register 01H Note	PR01H		Priority specification flag register 01H	PR01H	
FFFECH	Priority specification flag register 10L Note	PR10L	PR10	Priority specification flag register 10L	PR10L	PR10
FFFEDH	Priority specification flag register 10H Note	PR10H		Priority specification flag register 10H	PR10H	
FFFEEH	Priority specification flag register 11L Note	PR11L	PR11	Priority specification flag register 11L	PR11L	PR11
FFFEFH	Priority specification flag register 11H Note	PR11H		Priority specification flag register 11H	PR11H	
FFFF0H FFFF1H	Same as RL78/G1A (64-pin products)	MDAL		Multiplication/division data register A (L)	MDAL	
FFFF2H FFFF3H	Same as RL78/G1A (64-pin products)	MDAH		Multiplication/division data register A (H)	MDAH	
FFFF4H FFFF5H	Same as RL78/G1A (64-pin products)	MDBH		Multiplication/division data register B (L)	MDBH	
FFFF6H FFFF7H	Same as RL78/G1A (64-pin products)	MDBL		Multiplication/division data register B (H)	MDBL	
FFFFEH	Same as RL78/G1A (64-pin products)	PMC		Processor mode control register	PMC	

Note The bit setting is different from that of RL78/G1A (64-pin products).

Table 3-3. List of Differences in Expanded Special Function Registers (2nd SFRs) (2/6)

Address	RL78/G1E (64-pin products)			RL78/G1A (64-pin products)		
	2nd SFRs Name	Symbol		2nd SFRs Name	Symbol	
F0073H	Same as RL78/G1A (64-pin products)	ISC		Input switch control register	ISC	
F0074H	Timer input select register 0 Note	TIS0		Timer input select register 0	TIS0	
F0076H	A/D port configuration register Note	ADPC		A/D port configuration register	ADPC	
F0077H	Peripheral I/O redirection register Note	PIOR		Peripheral I/O redirection register	PIOR	
F0078H	Same as RL78/G1A (64-pin products)	IAWCTL		Invalid memory access detection control register	IAWCTL	
F007CH	Same as RL78/G1A (64-pin products)	GAIDIS		Global analog input disable register	GAIDIS	
F007DH				Global digital input disable register	GDIDIS	
F0090H	Same as RL78/G1A (64-pin products)	DFLCTL		Data flash control register	DFLCTL	
F00A0H	Same as RL78/G1A (64-pin products)	HIOTRM		High-speed on-chip oscillator trimming register	HIOTRM	
F00A8H	Same as RL78/G1A (64-pin products)	HOCODIV		High-speed on-chip oscillator frequency select register	HOCODIV	
F00E0H	Same as RL78/G1A (64-pin products)	MDCL		Multiplication/division data register C (L)	MDCL	
F00E2H	Same as RL78/G1A (64-pin products)	MDCH		Multiplication/division data register C (H)	MDCH	
F00E8H	Same as RL78/G1A (64-pin products)	MDUC		Multiplication/division control register	MDUC	
F00F0H	Peripheral enable register 0 Note	PER0		Peripheral enable register 0	PER0	
<R> F00F3H	Subsystem clock supply mode control register Note	OSMC		Subsystem clock supply mode control register	OSMC	
F00F5H	Same as RL78/G1A (64-pin products)	RPECTL		RAM parity error control register	RPECTL	
F00FEH	Same as RL78/G1A (64-pin products)	BCDADJ		BCD adjust result register	BCDADJ	
F0100H	Same as RL78/G1A (64-pin products)	SSR00L	SSR00	Serial status register 00	SSR00L	SSR00
F0101H		—			—	
F0102H	Same as RL78/G1A (64-pin products)	SSR01L	SSR01	Serial status register 01	SSR01L	SSR01
F0103H		—			—	
F0104H	Same as RL78/G1A (64-pin products)	SSR02L	SSR02	Serial status register 02	SSR02L	SSR02
F0105H		—			—	
F0106H	Same as RL78/G1A (64-pin products)	SSR03L	SSR03	Serial status register 03	SSR03L	SSR03
F0107H		—			—	
F0108H	Same as RL78/G1A (64-pin products)	SIR00L	SIR00	Serial flag clear trigger register 00	SIR00L	SIR00
F0109H		—			—	
F010AH	Same as RL78/G1A (64-pin products)	SIR01L	SIR01	Serial flag clear trigger register 01	SIR01L	SIR01
F010BH		—			—	
F010CH	Same as RL78/G1A (64-pin products)	SIR02L	SIR02	Serial flag clear trigger register 02	SIR02L	SIR02
F010DH		—			—	
F010EH	Same as RL78/G1A (64-pin products)	SIR03L	SIR03	Serial flag clear trigger register 03	SIR03L	SIR03
F010FH		—			—	

Note The bit setting is different from that of RL78/G1A (64-pin products).

Caution Do not write data to the registers which is in the row with painted gray.

3. 4. 3. 5 Port output mode register (POMxx)

(1) 64-pin products

Symbol	7	6	5	4	3	2	1	0	Address	After Reset	R/W
POM0	0	0	0	0	POM03	POM02	0	0	F0050H	00H	R/W
POM1	0	0	0	POM14	POM13	POM12	POM11	POM10	F0051H	00H	R/W

<R> **Caution Be sure to clear bits 0, 1 and 4 to 7 of the POM0 register, and bits 5 to 7 of the POM1 register to "0".**

<R> **(2) 80-pin products**

Symbol	7	6	5	4	3	2	1	0	Address	After Reset	R/W
POM0	0	0	0	POM04	POM03	POM02	0	0	F0050H	00H	R/W
POM1	0	0	POM15	POM14	POM13	POM12	POM11	POM10	F0051H	00H	R/W
POM5	0	0	0	0	0	0	0	POM50	F0055H	00H	R/W

Caution Be sure to clear bits 0, 1 and 5 to 7 of the POM0 register, bits 6 and 7 of the POM1 register, and bits 1 to 7 of the POM5 register to "0".

3. 4. 3. 6 Port mode control register (PMCxx)

<R> **(1) 64-pin products**

Symbol	7	6	5	4	3	2	1	0	Address	After Reset	R/W
PMC0	1	1	1	1	PMC03	PMC02	1	1	F0060H	FFH	R/W
PMC1	1	1	1	PMC14	PMC13	PMC12	PMC11	PMC10	F0061H	FFH	R/W
PMC4	1	1	1	1	1	1	PMC41	1	F0064H	FFH	R/W
PMC7	1	1	1	1	1	1	1	PMC70	F0067H	FFH	R/W

Caution Be sure to set bits 0, 1 and 4 to 7 of the PMC0 register, bits 5 to 7 of the PMC1 register, bits 0 and 2 to 7 of the PMC4 register, and bits 1 to 7 of the PMC7 register to "0".

<R> **(2) 80-pin products**

Symbol	7	6	5	4	3	2	1	0	Address	After Reset	R/W
PMC0	1	1	1	1	PMC03	PMC02	1	1	F0060H	FFH	R/W
PMC1	1	1	PMC15	PMC14	PMC13	PMC12	PMC11	PMC10	F0061H	FFH	R/W
PMC4	1	1	1	1	1	1	PMC41	1	F0064H	FFH	R/W
PMC5	1	1	1	1	1	1	PMC51	PMC50	F0065H	FFH	R/W
PMC7	1	1	1	1	1	1	1	PMC70	F0067H	FFH	R/W

Caution Be sure to set bits 0, 1 and 4 to 7 of the PMC0 register, bits 6 and 7 of the PMC1 register, bits 0 and 2 to 7 of the PMC4 register, bits 2 to 7 of the PMC5 register, and bits 1 to 7 of the PMC7 register to "0".

<R> **(2) Setting procedure when using output ports of UART0 to UART2, CSI00, CSI10, and CSI20 functions in N-ch open-drain output mode**

In case of UART0: P12
In case of UART1: P02
In case of UART2: P13
In case of CSI00: P10, P12
In case of CSI10: P02, P04
In case of CSI20: P13, P15

<1> Using an external resistor, pull up externally the output pin to be used to the power supply of the target device (on-chip pull-up resistor cannot be used).
<2> After reset release, the port mode changes to the input mode (Hi-Z).
<3> Set the output latch of the corresponding port to 1.
<4> Set the corresponding bit of the POM0 and POM1 registers to 1 to set the N-ch open drain output (V_{DD} withstand voltage) mode.
<5> Enable the operation of the serial array unit and set the mode to the UART/CSI mode.
<6> Set the output mode by manipulating the PM0 and PM1 registers. At this time, the output data is high level, so the pin is in the Hi-Z state.

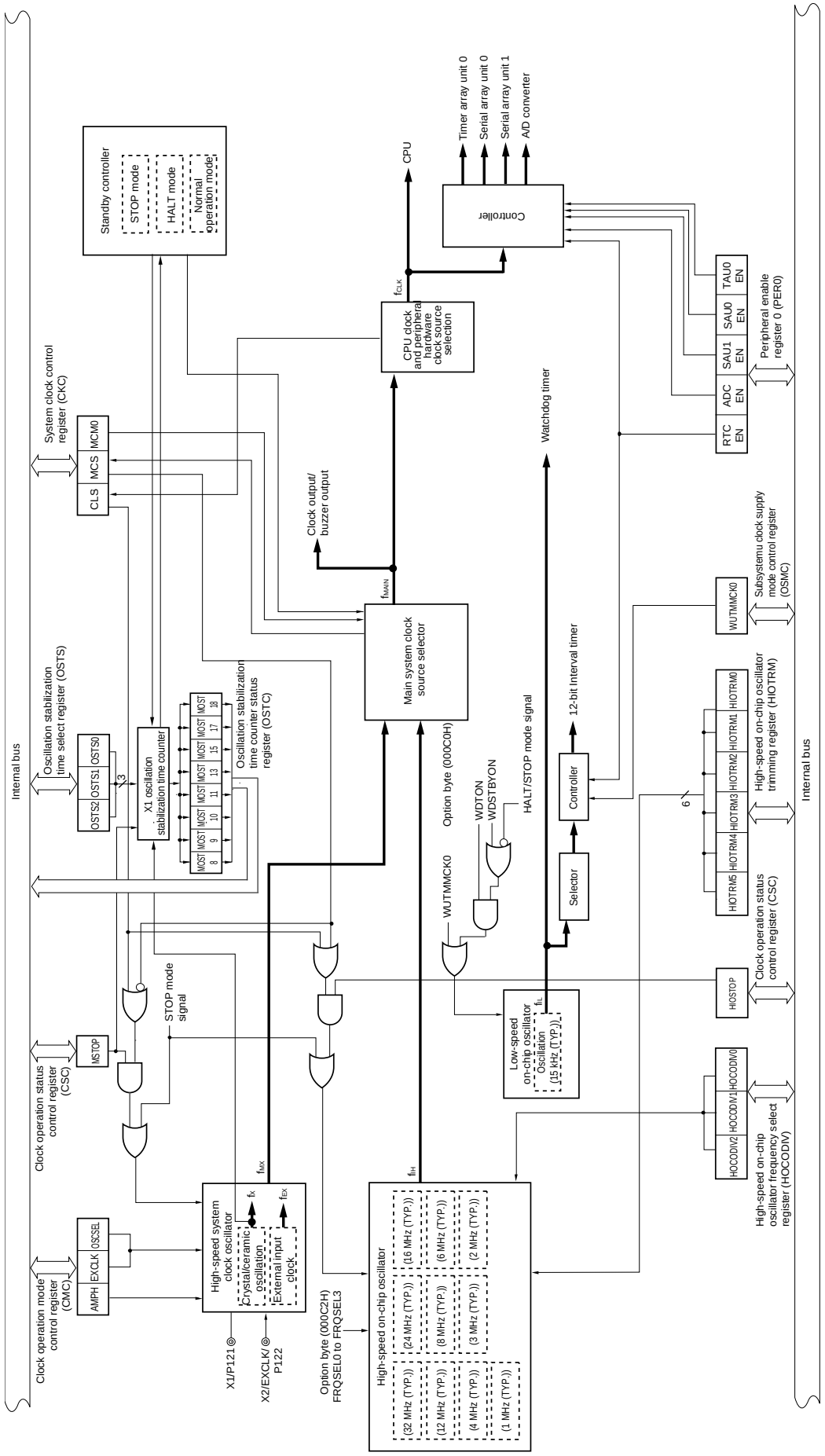
<R> **(3) Setting procedure when using I/O ports of IIC00, IIC10, and IIC20 functions with a different potential (1.8 V ,2.5 V or 3V)**

In case of IIC00: P10, P11
In case of IIC10: P03, P04
In case of IIC20: P14, P15

<1> Using an external resistor, pull up externally the input pin to be used to the power supply of the target device (on-chip pull-up resistor cannot be used).
<2> After reset release, the port mode is the input mode (Hi-Z).
<3> Set the output latch of the corresponding port to 1.
<4> Set the corresponding bit of the POM0 and POM1 registers to 1 to set the N-ch open drain output (V_{DD} tolerance) mode.
<5> Set the corresponding bit of the PIM0 and PIM1 registers to 1 to switch to the TTL input buffer. For V_{IH} and V_{IL}, refer to the DC characteristics when the TTL input buffer is selected.
<6> Enable the operation of the serial array unit and set the mode to the simplified I^2C mode.
<7> Set the corresponding bit of the PM0 and PM1 registers to the output mode (data I/O is possible in the output mode).
At this time, the output data is high level, so the pin is in the Hi-Z state.

Figure 3-1. Block Diagram of Clock Generator

<R>



(**Remark** is listed on the next page)

3. 5. 3 Registers controlling clock generator

The bit settings which are different from that of RL78/G1A (64-pin products) are shown below. For details of each register, see **5. 3 Registers Controlling Clock Generator** in **RL78/G1A Hardware User's Manual (R01UH0305E)**.

<R> **3. 5. 3. 1 Clock operation mode control register (CMC)**

Address: FFFA0H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
CMC	EXCLK	OSCSEL	0	0	0	0	0	AMPH

EXCLK	OSCSEL	High-speed system clock pin operation mode	X1/P121 pin	X2/EXCLK/P122 pin
0	0	Input port mode	Input port	
0	1	X1 oscillation mode	Crystal/ceramic resonator connection	
1	0	Input port mode	Input port	
1	1	External clock input mode	Input port	External clock input

AMPH	Control of X1 clock oscillation frequency
0	1 MHz ≤ fx ≤ 10 MHz
1	10 MHz < fx ≤ 20 MHz

Cautions 1. Be sure to clear bits 1 to 3 and 5 to "0".

2. The CMC register can be written only once after reset release, by an 8-bit memory manipulation instruction. When using the CMC register with its initial value (00H), be sure to set the register to 00H after a reset ends in order to prevent malfunction due to a program loop. Such a malfunction becomes unrecoverable when a value other than 00H is mistakenly written.

3. After reset release, set the CMC register before X1 oscillation is started as set by the clock operation status control register (CSC).

4. Be sure to set the AMPH bit to 1 if the X1 clock oscillation frequency exceeds 10 MHz.

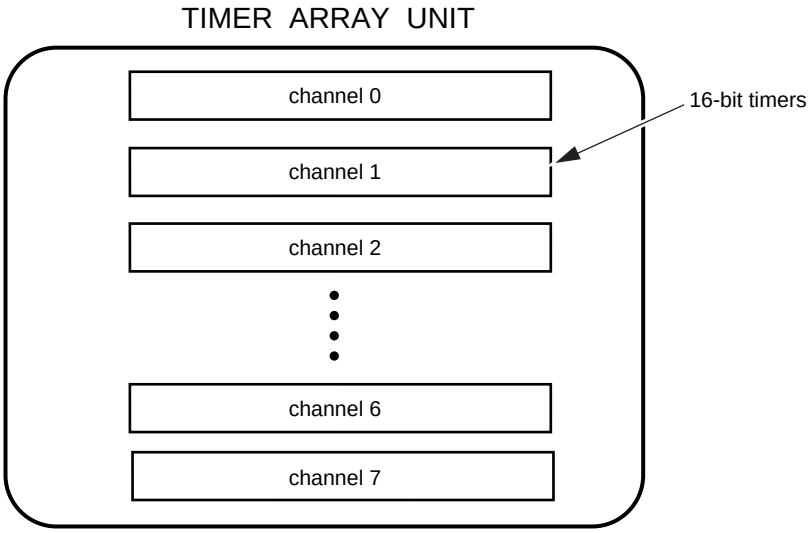
5. Specify the settings for the AMPH, AMPHS1, and AMPHS0 bits while f_{IH} is selected as f_{CLK} after a reset ends (before f_{CLK} is switched to f_{MX}).

6. Although the maximum system clock frequency is 32 MHz, the maximum frequency of the X1 oscillator is 20 MHz.

Remark fx: X1 clock oscillation frequency

The timer array unit has eight 16-bit timers.

Each 16-bit timer is called a channel and can be used as an independent timer. In addition, two or more “channels” can be used to create a high-accuracy timer.



For the details of each function, see the section shown below.

Independent channel operation function	Simultaneous channel operation function
• Interval timer (-> see 3. 6. 8) • Square wave output (-> see 3. 6. 8) • External event counter (-> see 3. 6. 8) • Divider function [Note] (-> see 3. 6. 8) • Input pulse interval measurement (-> see 3. 6. 8) • Measurement of high/low-level width of input signal (-> see 3. 6. 8) • Delay counter (-> see 3. 6. 8)	• One-shot pulse output (-> see 3. 6. 9) • PWM output (-> see 3. 6. 9) • Multiple PWM output (-> see 3. 6. 9)

Note Only channel 0 of unit 0.

It is possible to use the 16-bit timer of channels 1 and 3 of unit 0 as two 8-bit timers (higher and lower). The functions that can use channels 1 and 3 as 8-bit timers are as follows:

- Interval timer (higher/lower 8-bit timer)/square wave output (lower 8-bit timer only)
- External event counter (lower 8-bit timer only)
- Delay counter (lower 8-bit timer only)

Channel 7 of unit 0 can be used to realize LIN-bus communication operating in combination with UART2 of the serial array unit.

3. 12. 3. 5 Higher 7 bits of the serial data register mn (SDRmn)

The bit setting is same as that of RL78/G1A (64-pin products). For details, see **12. 3. 5 Higher 7 bits of the serial data register mn (SDRmn)** in **RL78/G1A Hardware User's Manual (R01UH0305E)**.

3. 12. 3. 6 Serial flag clear trigger register mn (SIRmn)

The bit setting is same as that of RL78/G1A (64-pin products). For details, see **12. 3. 6 Serial flag clear trigger register mn (SIRmn)** in **RL78/G1A Hardware User's Manual (R01UH0305E)**.

3. 12. 3. 7 Serial status register mn (SSRmn)

The bit setting is same as that of RL78/G1A (64-pin products). For details, see **12. 3. 7 Serial status register mn (SSRmn)** in **RL78/G1A Hardware User's Manual (R01UH0305E)**.

3. 12. 3. 8 Serial channel start register m (SSm)

The bit setting is same as that of RL78/G1A (64-pin products). For details, see **12. 3. 8 Serial channel start register m (SSm)** in **RL78/G1A Hardware User's Manual (R01UH0305E)**.

3. 12. 3. 9 Serial channel stop register m (STm)

The bit setting is same as that of RL78/G1A (64-pin products). For details, see **12. 3. 9 Serial channel stop register m (STm)** in **RL78/G1A Hardware User's Manual (R01UH0305E)**.

3. 12. 3. 10 Serial channel enable status register m (SEm)

The bit setting is same as that of RL78/G1A (64-pin products). For details, see **12. 3. 10 Serial channel enable status register m (SEm)** in **RL78/G1A Hardware User's Manual (R01UH0305E)**.

3. 12. 3. 11 Serial output enable register m (SOEm)

The bit setting is same as that of RL78/G1A (64-pin products). For details, see **12. 3. 11 Serial output enable register m (SOEm)** in **RL78/G1A Hardware User's Manual (R01UH0305E)**.

3. 12. 3. 12 Serial output register m (SOm)

The bit setting is same as that of RL78/G1A (64-pin products). For details, see **12. 3. 12 Serial output register m (SOm)** in **RL78/G1A Hardware User's Manual (R01UH0305E)**.

Table 3-13. Interrupt Source List (3/3)

Interrupt Type	Default Priority[Note 1]	Interrupt Source		Internal/External	Vector Table Address	Basic Configuration Type[Note 2]	RL78/G1E	
		Name	Trigger				64-pin	80-pin
Maskable	29	INTTM05	End of timer channel 5 count or capture	Internal	0044H	(A)	√	√
	30	INTTM06	End of timer channel 6 count or capture		0046H		√	√
	31	INTTM07	End of timer channel 7 count or capture		0048H		√	√
	32	INTP6	Pin input edge detection	External	004AH	(B)	–	√
	33	INTP7			004CH		–	–
	34	INTP8			004EH		–	–
	35	INTP9			0050H		–	–
	36	INTP10			0052H		–	–
	37	INTP11			0054H		–	–
<R>	38	INTMD	End of division operation/Overflow of multiplyaccumulation result occurs	Internal	005EH	(A)	√	√
	39	INTFL	Reserved[Note 3]		0062H		√	√
Software	–	BRK	Execution of BRK instruction	–	007EH	(D)	√	√
Reset	–	RESET	$\overline{\text{RESET}}$ pin input	–	0000H	–	√	√
		POR	Power-on-reset				√	√
		LVD	Voltage detection[Note 4]				√	√
		WDT	Overflow of watchdog timer				√	√
		TRAP	Execution of illegal instruction[Note 5]				√	√
		IAW	Illegal-memory access				√	√
		RAMTOP	RAM parity error				√	√

Notes 1. The default priority determines the sequence of interrupts if two or more maskable interrupts occur simultaneously. Zero indicates the highest priority and 39 indicates the lowest priority.

2. Basic configuration types (A) to (D) correspond to (A) to (D) in Figure 3-13.

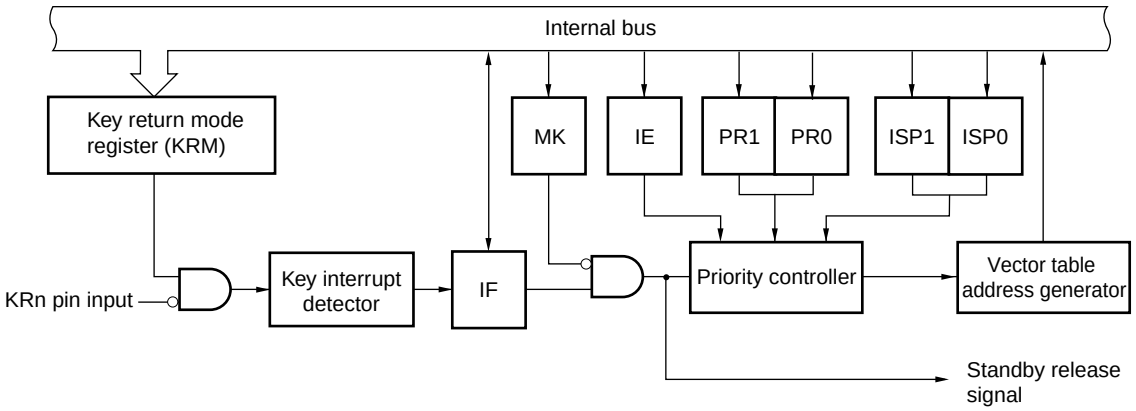
<R> **3.** Be used at the flash self programming library or the data flash library.

4. When bit 7 (LVIMD) of the voltage detection level register (LVIS) is set to 1.

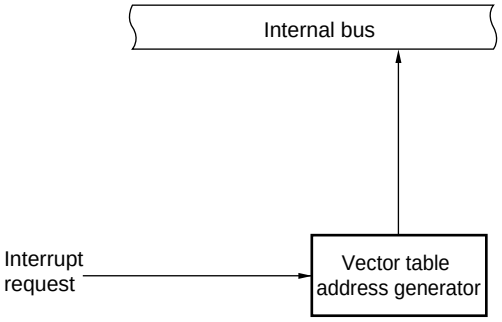
5. When the instruction code in FFH is executed.
Reset by the illegal instruction execution not issued by emulation with the in-circuit emulator or on-chip debug emulator.

Figure 3-13. Basic Configuration of Interrupt Function (2/2)

(c) External maskable interrupt (INTKR)



(d) Software interrupt



IF: Interrupt request flag
IE: Interrupt enable flag
ISP0: In-service priority flag 0
ISP1: In-service priority flag 1
MK: Interrupt mask flag
PR0: Priority specification flag 0
PR1: Priority specification flag 1

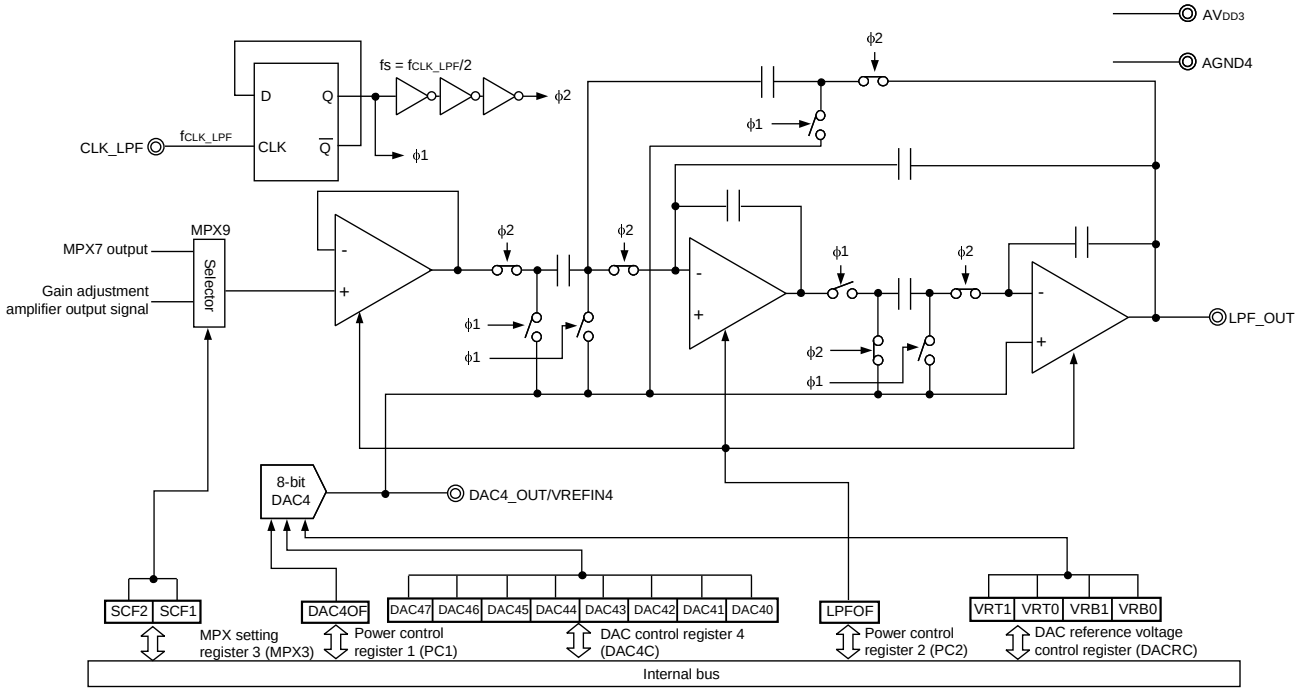
Remark 64-pin products: n = 0 to 6
80-pin products: n = 0 to 7

3. 18 Standby Function

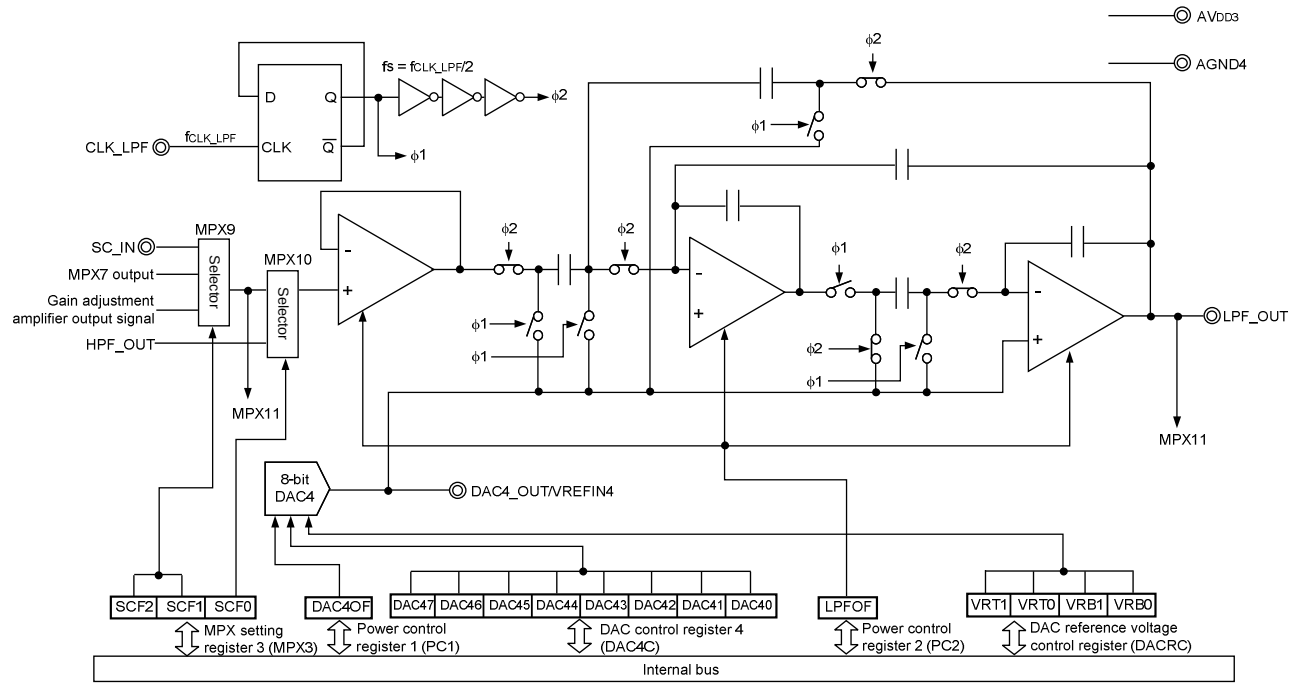
See **CHAPTER 18 STANDBY FUNCTION** in **RL78/G1A Hardware User's Manual (R01UH0305E)**.

4. 4. 2 Block diagram

- **64-pin products**



- **80-pin products**



4. 9 SPI

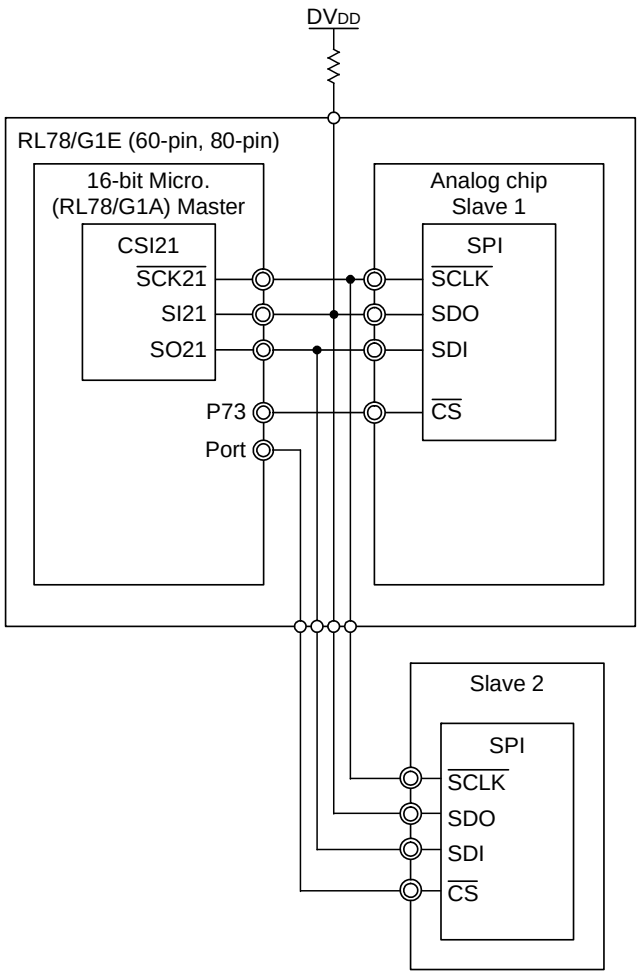
4. 9. 1 Overview of SPI features

The SPI interface is used to allow control from external devices by using clocked communication via four lines: a serial clock line ($\overline{\text{SCLK}}$), two serial data lines (SDI and SDO), and a chip select input line ($\overline{\text{CS}}$).

Data transmission/reception:

- 16-bit data unit
- MSB first

Figure 4-4. SPI Configuration Example



Caution After turning on DV_{DD}, be sure to generate external reset by inputting a reset signal to $\overline{\text{ARESET}}$ pin before starting SPI communication. For details, see 4.10 Analog Reset.

<R> 5. 2. 1. 2 On-chip oscillator characteristics

(T_A = –40 to +85°C, 1.6 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Resonator	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
High-speed on-chip oscillator clock frequency Note 1, 2	f_{IH}			1		32	MHz
High-speed on-chip oscillator clock frequency accuracy		–20 to + 85 °C	1.8 V ≤ V_{DD} ≤ 5.5 V	– 1.0		+ 1.0	%
			1.6 V ≤ V_{DD} ≤ 1.8 V	– 5.0		+ 5.0	%
		–40 to – 20 °C	1.8 V ≤ V_{DD} ≤ 5.5 V	– 1.5		+ 1.5	%
			1.6 V ≤ V_{DD} ≤ 1.8 V	– 5.5		+ 5.5	%
Low-speed on-chip oscillator clock frequency	f_{IL}				15		kHz
Low-speed on-chip oscillator clock frequency accuracy				– 15		+ 15	%

Notes 1. Frequency can be selected in a high-speed on-chip oscillator. Selected by bits 0 to 3 of option byte (000C2H/010C2H) and bits 0 to 2 of HOCODIV register.

2. Indicates only permissible frequency level. Refer to AC Characteristics for instruction execution time.

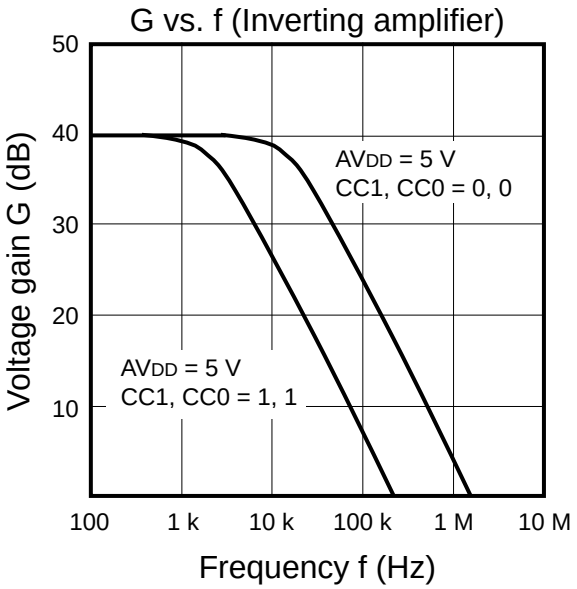
(T_A = –40 to +85°C, 1.6 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V) (3/3)

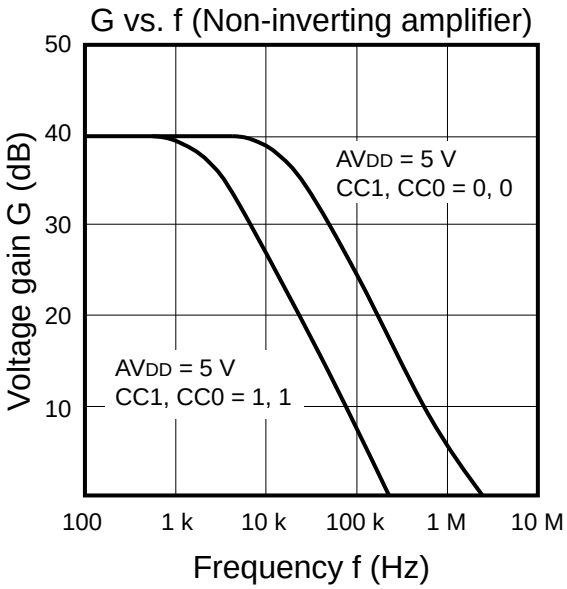
Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
<R> Low-speed on-chip oscillator operating current	I_{FIL} Note 1				0.20		μA
12-bit Interval timer operating current	I_{IT} Note 1, 2, 3				0.02 Note 3		μA
Watchdog timer operating current	I_{WDT} Note 1, 2, 4	f_{IL} = 15 kHz, f_{MAIN} is stopped			0.22		μA
A/D converter operating current	I_{ADC} Note 5, 6	AV_{DD} = 3.0 V, When conversion at maximum speed			420	720	μA
$AV_{REF(+)}$ current	I_{AVREF} Note 7	AV_{DD} = 3.0 V, ADREFP1 = 0, ADREFP0 = 0 Note 6			14.0	25.0	μA
		AV_{REFP} = 3.0 V, ADREFP1 = 0, ADREFP0 = 1 Note 9			14.0	25.0	μA
		ADREFP1 = 1, ADREFP0 = 0 Note 1			14.0	25.0	μA
A/D converter reference voltage current	I_{ADREF} Note 1, 8	V_{DD} = 3.0 V			75.0		μA
Temperature sensor operating current	I_{TMPS} Note 1	V_{DD} = 3.0 V			75.0		μA
LVD operating current	I_{LVD} Note 1, 10				0.08		μA
BGO operating current	I_{BGO} Note 1, 11				2.5	12.2	mA
Selfprogramming operating current	I_{FSP} Note 1, 12				2.5	12.2	mA
SNOOZE operating current	I_{SNOZ}	A/D converter operation (AV_{DD} = 3.0 V)	The mode is performed Note 1, 13		0.50	0.60	mA
			During A/D conversion Note 1		0.60	0.75	mA
			During A/D conversion Note 6		420	720	μA
		CSI/UART operation Note 1			0.70	0.84	mA

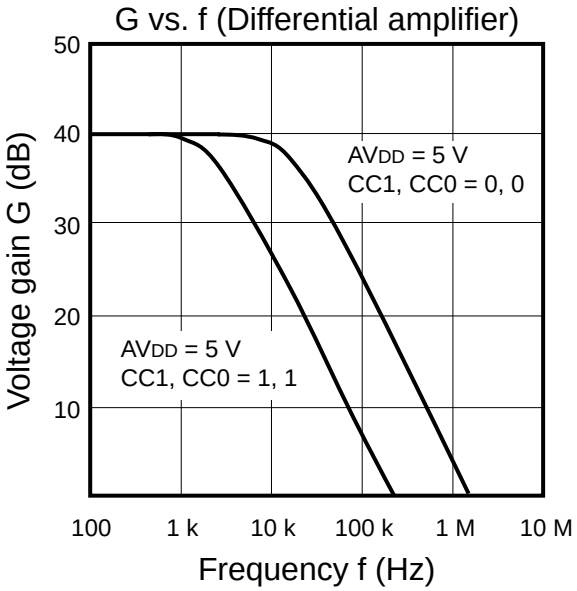
(**Notes** and **Remarks** are listed on the next page.)

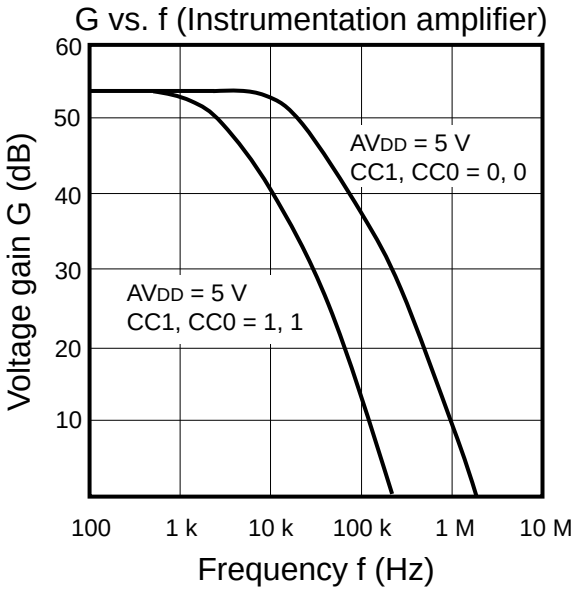
APPENDIX A CHARACTERISTICS CURVE (T_A = 25°C, TYP.) (REFERENCE VALUE)

• Configurable amplifier

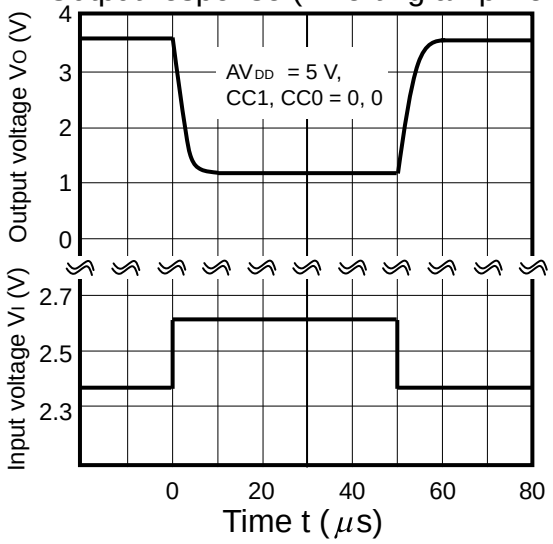




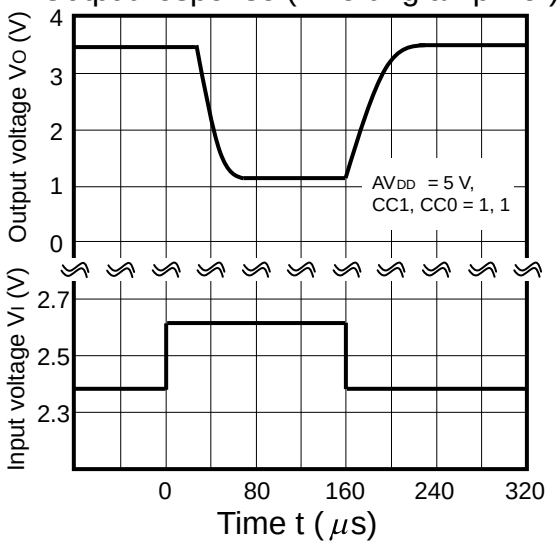




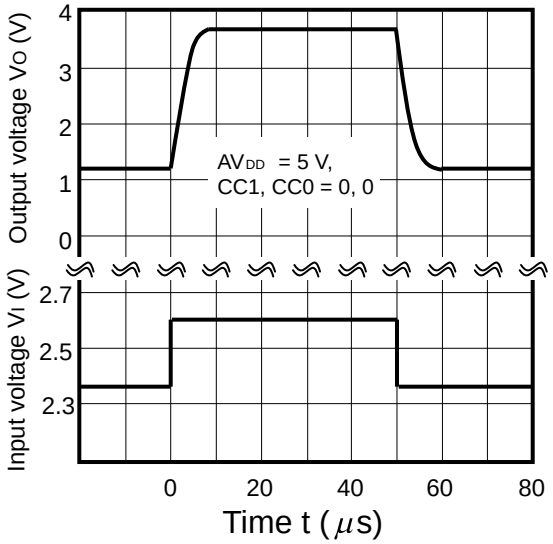
Output response (Inverting amplifier)



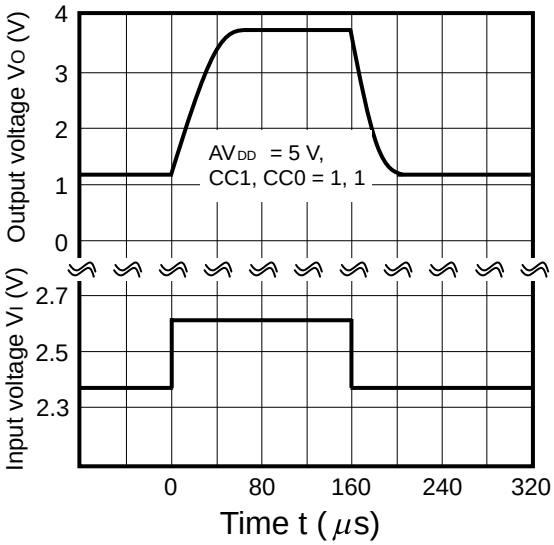
Output response (Inverting amplifier)



Output response (Non-inverting amplifier)



Output response (Non-inverting amplifier)



(4/6)

Edition	Description	Chapter
Rev.1.00	Modification of the description in **5. 2. 8 Timing specs for switching flash memory programming modes**	**CHAPTER 5 ELECTRICAL SPECIFICATIONS**
	Addition of the specification depending on the products in **5. 3. 3. 2 Gain adjustment amplifier characteristics**	
	Addition of the specification for “CLK_SYNCH input voltage” in **5. 3. 3. 2 Gain adjustment amplifier characteristics (2) 80-pin products**	
	Error correction of the description and addition of the specification for “CLK_SYNCH input voltage” in **5. 3. 3. 4 Low-pass filter characteristics**	
	Error correction of the description and addition of the specification for “CLK_SYNCH input voltage” in **5. 3. 3. 5 High-pass filter characteristics**	
Rev.0.04	Change of the name for CS from “Slave Select” to “Chip Select”	Whole pages
	Deletion of the word “interface” from the name of SPI	
	Error correction of the figures in **1. 4 Pin Configuration (Top View)**	**CHAPTER 1 OUTLINE**
	Error correction of the description (deletion of “SCLA0”, “SCLA1”) in **1. 4. 3 Pin identification (Microcontroller Block)**	
	Error correction of the figures in **1. 5 Block Diagram**	
	Error correction of the function names and modification of the description for the function in **2. 2 Pin Functions in Analog Block**	**CHAPTER 2 PIN FUNCTIONS**
	Error correction of the description for the pin of ANI30 (D/A converter -> A/D converter) in **2. 3. 4 P40 to P42 (port 4)**	
	Modification of the description in **2. 3. 43 I.C**	
	Addition of “Remarks” on the tables in **3. 1 Differences in Functions between RL78/G1E and RL78/G1A**	**CHAPTER 3 MICROCONTROLLER FUNCTION**
	Modification of the description on the tables (deletion of the same registers as RL78/G1A) in **3. 2 Differences in (Expanded) Special-Function Registers between RL78/G1E and RL78/G1A**	
	Modification of the description and change of the sequence flow of the setting procedure (2) in **3. 3. 3 Connecting to an external device with different potential (1.8 V, 2.5 V, 3 V)**	
	Addition of **3. 4. 4 Resonator and Oscillator Constants**	
	Error correction of the description on **Table 3-14.**	
	Addition of **3. 13 Safety Functions**	
	Modification of the gain setting of non-inverting amplifier in **5. 1 Overview of Configurable Amplifier Features** and in **5. 3 Registers Controlling the Configurable Amplifiers**	**CHAPTER 5 CONFIGURABLE AMPLIFIERS**
	Modification of the description in **8. 1 Overview of Low-Pass Filter Features**	**CHAPTER 8 LOW-PASS FILTER**
	Modification of the description in **9. 1 Overview of High-Pass Filter Features**	**CHAPTER 8 HIGH-PASS FILTER**
	Addition of **Note** in **11. 3 Registers Controlling the Variable Output Voltage Regulator**	**CHAPTER 11 VARIABLE OUTPUT VOLTAGE REGULATOR**