Renesas Electronics America Inc - R5F10FMDDFB#V0 Datasheet

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	RL78
Core Size	16-Bit
Speed	32MHz
Connectivity	CSI, I²C, LINbus, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	26
Program Memory Size	48KB (48K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	3K x 8
Voltage - Supply (Vcc/Vdd)	1.6V ~ 5.5V
Data Converters	A/D 17x8/12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	80-LQFP
Supplier Device Package	80-LFQFP (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f10fmddfb-v0

How to Use This Manual

Readers

This manual is intended for user engineers who wish to understand the functions of the RL78/G1E and design and develop application systems and programs for these devices.
The target products are as follows.

- 64-pin: R5F10FLx (x = C, D, E)
- 80-pin: R5F10FMx (x = C, D, E)

Purpose

This manual is intended to give users an understanding of the functions described in the **Organization** below.

Organization

The RL78/G1E manual is separated into three parts: this manual, RL78/G1A user's manual, and the RL78 family software user's manual.

RL78/G1E User's Manual (This Manual)	**RL78/G1A Hardware User's Manual**	**RL78 family Software User's Manual**
• Pin functions • Internal block functions • On-chip peripheral functions • Electrical specifications	• Pin functions • Internal block functions • Interrupts • Other on-chip peripheral functions • Electrical specifications	• CPU functions • Instruction set • Explanation of each instruction

○ Analog Block

AV_{DD1}	Power supply for configurable amplifiers	AMP1_OUT, AMP2_OUT, AMP3_OUT	Configurable amplifier output
AV_{DD2}	Power supply for variable output voltage regulator and reference voltage generator	DAC1_OUT, DAC2_OUT, DAC3_OUT, DAC4_OUT	D/A converter output
AV_{DD3}	Power supply for low-pass filter and high-pass filter		
AGND1	Ground for configurable amplifiers	VREFIN1,	
AGND2	Ground for gain adjustment amplifier	VREFIN2,	
AGND3	Ground for variable output voltage regulator and reference voltage generator	VREFIN3	Reference voltage input for configurable amplifier
		VREFIN4	Reference voltage input for Gain adjustment amplifier, low-pass filter, and high-pass filter
AGND4	Ground for low-pass filter and high-pass filter		
MPXIN10,	Multiplexer input	$\overline{SCLK}$	Serial clock input
MPXIN11,		SDO	Serial data output
MPXIN20,		SDI	Serial data input
MPXIN21,		$\overline{CS}$	Chip select input
MPXIN30,		TEMP_OUT	Temperature sensor output
MPXIN31,		$\overline{ARESET}$	Reset for analog block
MPXIN40,		DV_{DD}	Power supply for SPI
MPXIN41,		DGND	Ground for SPI
MPXIN50,		HPF_OUT	High-pass filter output
MPXIN51,		CLK_HPF	Pin for inputting high-pass filter control clock
MPXIN60,			
MPXIN61		CLK_LPF	Pin for inputting low-pass filter control clock
SC_IN	Input for filter signal processing		
CLK_SYNCH	Synchronous detector control clock input	LPF_OUT	Low-pass filter output
		BGR_OUT	Reference voltage generator output
SYNCH_OUT	Synchronous detector output	LDO_OUT	Variable output voltage regulator
GAINAMP_IN	Gain adjustment amplifier input	I.C	Internal connect
GAINAMP_OUT	Gain adjustment amplifier output		

3. 6. 3. 9 Timer output enable register m (TOEm)

Address: F01BAH, F01BBH (TOE0) After reset: 0000H R/W

Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TOEm	0	0	0	0	0	0	0	0	TOEm7	0	0	TOEm4	0	0	0	TOEm0

TOEmn	Timer output enable/disable of channel n
0	The TOmn operation stopped by count operation (timer channel output bit). Writing to the TOmn bit is enabled. The TOmn pin functions as data output, and it outputs the level set to the TOmn bit. The output level of the TOmn pin can be manipulated by software.
1	The TOmn operation enabled by count operation (timer channel output bit). Writing to the TOmn bit is disabled (writing is ignored). The TOmn pin functions as timer output, and the TOEmn bit is set or reset depending on the timer operation. The TOmn pin outputs the square-wave or PWM depending on the timer operation.

Caution Be sure to clear bits 15 to 8, 6, 5, 3 to 1 to “0”.

Remark m: Unit number (m = 0), n: Channel number (n = 0 to 7 (however, timer input pin (TImn), timer output pin (TOmn): n = 0, 4, 7))

3. 6. 3. 10 Timer output register m (TOm)

Address: F01B8H, F01B9H (TO0) After reset: 0000H R/W

Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TOm	0	0	0	0	0	0	0	0	TOm7	0	0	TOm4	0	0	0	TOm0

TOmn	Timer output of channel n
0	Timer output value is “0”.
1	Timer output value is “1”.

Caution Be sure to clear bits 15 to 8, 6, 5, 3 to 1 to “0”.

Remark m: Unit number (m = 0), n: Channel number (n = 0 to 7 (however, timer input pin (TImn), timer output pin (TOmn): n = 0, 4, 7))

Address: FFF31H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
ADS	ADISS	0	0	ADS4	ADS3	ADS2	ADS1	ADS0

• Select mode (80-pin products, ADMD = 0)

ADISS	ADS4	ADS3	ADS2	ADS1	ADS0	Selected channel	Input source
0	0	0	0	0	0	ANI0	P20/ANI0/AVREFP pin
0	0	0	0	0	1	ANI1	P21/ANI1/AVREFM pin
0	0	0	0	1	0	ANI2	P22/ANI2 pin
0	0	0	0	1	1	ANI3	P23/ANI3 pin
0	0	0	1	0	0	ANI4	P24/ANI4 pin
0	0	0	1	0	1	Setting prohibited	
0	0	0	1	1	0	Setting prohibited	
0	0	0	1	1	1	Setting prohibited	
0	0	1	0	0	0	Setting prohibited	
0	0	1	0	0	1	Setting prohibited	
0	0	1	0	1	0	Setting prohibited	
0	0	1	0	1	1	Setting prohibited	
0	0	1	1	0	0	Setting prohibited	
0	0	1	1	0	1	Setting prohibited	
0	0	1	1	1	0	Setting prohibited	
0	0	1	1	1	1	Setting prohibited	
0	1	0	0	0	0	ANI16	P03/ANI16 pin
0	1	0	0	0	1	ANI17	P02/ANI17 pin
0	1	0	0	1	0	ANI18	P10/ANI18 pin
0	1	0	0	1	1	Setting prohibited	
0	1	0	1	0	0	ANI20	P11/ANI20 pin
0	1	0	1	0	1	ANI21	P12/ANI21 pin
0	1	0	1	1	0	ANI22	P13/ANI22 pin
0	1	0	1	1	1	ANI23	P14/ANI23 pin
0	1	1	0	0	0	ANI24	P15/ANI24 pin
0	1	1	0	0	1	ANI25	P51/ANI25 pin
0	1	1	0	1	0	ANI26	P50/ANI26 pin
0	1	1	0	1	1	Setting prohibited	
0	1	1	1	0	0	ANI28	P70/ANI28 pin
0	1	1	1	0	1	Setting prohibited	
0	1	1	1	1	0	ANI30	P41/ANI30 pin
0	1	1	1	1	1	Setting prohibited	
1	0	0	0	0	0	–	Temperature sensor output[Note]
1	0	0	0	0	1	–	Internal reference voltage output (1.45 V)[Note]
Other than above						Setting prohibited	

Note This setting can be used only in HS (high-speed main) mode.

<R> **3. 12. 3 Registers controlling serial array unit**

The bit settings which are different from that of RL78/G1A (64-pin products) are shown below. For details of each register, see **12. 3 Registers Controlling Serial Array Unit** in **RL78/G1A Hardware User's Manual (R01UH0305E)**.

3. 12. 3. 1 Peripheral enable register 0 (PER0)

Address: F00F0H After reset: 00H R/W

Symbol	<7>	6	<5>	4	<3>	<2>	1	<0>
PER0	RTCEN	0	ADCEN	0	SAU1EN	SAU0EN	0	TAU0EN

SAU1EN	Control of serial array unit 1 input clock supply
0	Stops input clock supply. • SFR used by the serial array unit 1 cannot be written. • The serial array unit 1 is in the reset status.
1	Enables input clock supply. • SFR used by the serial array unit 1 can be read/written.

<R>

SAU0EN	Control of serial array unit 0 input clock supply
0	Stops input clock supply. • SFR used by the serial array unit 0 cannot be written. • The serial array unit 0 is in the reset status.
1	Enables input clock supply. • SFR used by the serial array unit 0 can be read/written.

<R>

Caution Be sure to clear bits 1, 4, and 6 to "0".

3. 12. 3. 2 Serial clock select register m (SPSm)

The bit setting is same as that of RL78/G1A (64-pin products). For details, see **12. 3. 2 Serial clock select register m (SPSm)** in **RL78/G1A Hardware User's Manual (R01UH0305E)**.

3. 13 Serial Interface IICA

Serial interface IICA is not provided in RL78/G1E (64-pin products, 80-pin products).

3. 16 Interrupt Functions

The interrupt function switches the program execution to other processing. When the branch processing is finished, the program returns to the interrupted processing. The number of interrupt sources differs, depending on the product.

		64-pin products	80-pin products
Maskable interrupts	External	2	5
	Internal	25	

3. 16. 1 Interrupt function types

The following two types of interrupt functions are used.

(1) Maskable interrupts

These interrupts undergo mask control. Maskable interrupts can be divided into four priority groups by setting the priority specification flag registers (PR00L, PR00H, PR01L, PR01H, PR02L, PR02H, PR10L, PR10H, PR11L, PR11H, PR12L, PR12H).

Multiple interrupt servicing can be applied to low-priority interrupts when high-priority interrupts are generated. If two or more interrupt requests, each having the same priority, are simultaneously generated, then they are processed according to the default priority of vectored interrupt servicing. Default priority, see **Table 3-13**.

A standby release signal is generated and STOP, HALT, and SNOOZE modes are released.

External interrupt requests and internal interrupt requests are provided as maskable interrupts.

(2) Software interrupt

This is a vectored interrupt generated by executing the BRK instruction. It is acknowledged even when interrupts are disabled. The software interrupt does not undergo interrupt priority control.

3. 16. 2 Interrupt sources and configuration

Interrupt sources include maskable interrupts and software interrupts. In addition, they also have up to seven reset sources (see **Table 3-13**). The vector codes that store the program start address when branching due to the generation of a reset or various interrupt requests are two bytes each, so interrupts jump to a 64 K address of 00000H to 0FFFFH.

3. 19 Reset Function

See **CHAPTER 19 RESET FUNCTION** in **RL78/G1A Hardware User's Manual (R01UH0305E)**.

<R> The reset and internal interrupt signals are generated in each mode as follows.

Interrupt & reset mode (LVIMDS1, LVIMDS0 = 1, 0)	Reset mode (LVIMDS1, LVIMDS0 = 1, 1)	Interrupt mode (LVIMDS1, LVIMDS0 = 0, 1)
Generates an interrupt request signal by detecting $V_{DD} < V_{LVDH}$ when the operating voltage falls, and an internal reset by detecting $V_{DD} < V_{LVDL}$. Releases an internal reset by detecting $V_{DD} \geq V_{LVDH}$.	Releases an internal reset by detecting $V_{DD} \geq V_{LVD}$. Generates an interrupt request signal by detecting $V_{DD} < V_{LVD}$.	Releases an internal reset by detecting $V_{DD} \geq V_{LVD}$ at power on after the first release of the POR. Generates an interrupt request signal by detecting $V_{DD} < V_{LVD}$ or $V_{DD} \geq V_{LVD}$ at power on after the second release of the POR.

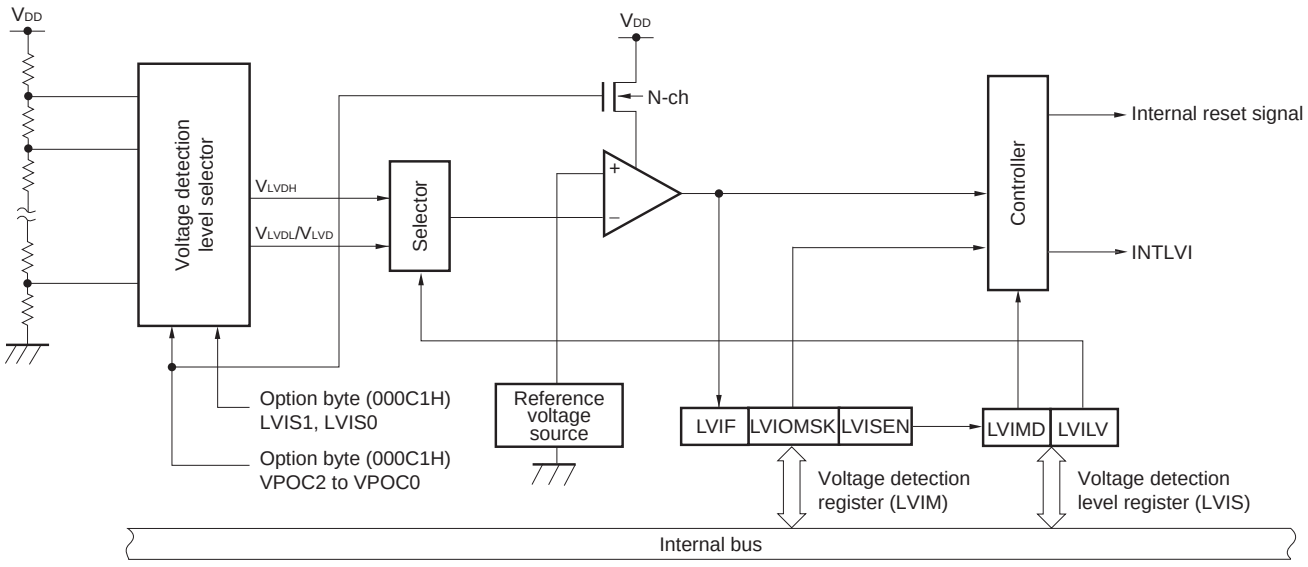
While the voltage detector is operating, whether the supply voltage or the input voltage from an external input pin is more than or less than the detection level can be checked by reading the voltage detection flag (LVIF: bit 0 of the voltage detection register (LVIM)).

Bit 0 (LVIRF) of the reset control flag register (RESF) is set to 1 if reset occurs. For details of the RESF register, see **3. 19 Reset Function**.

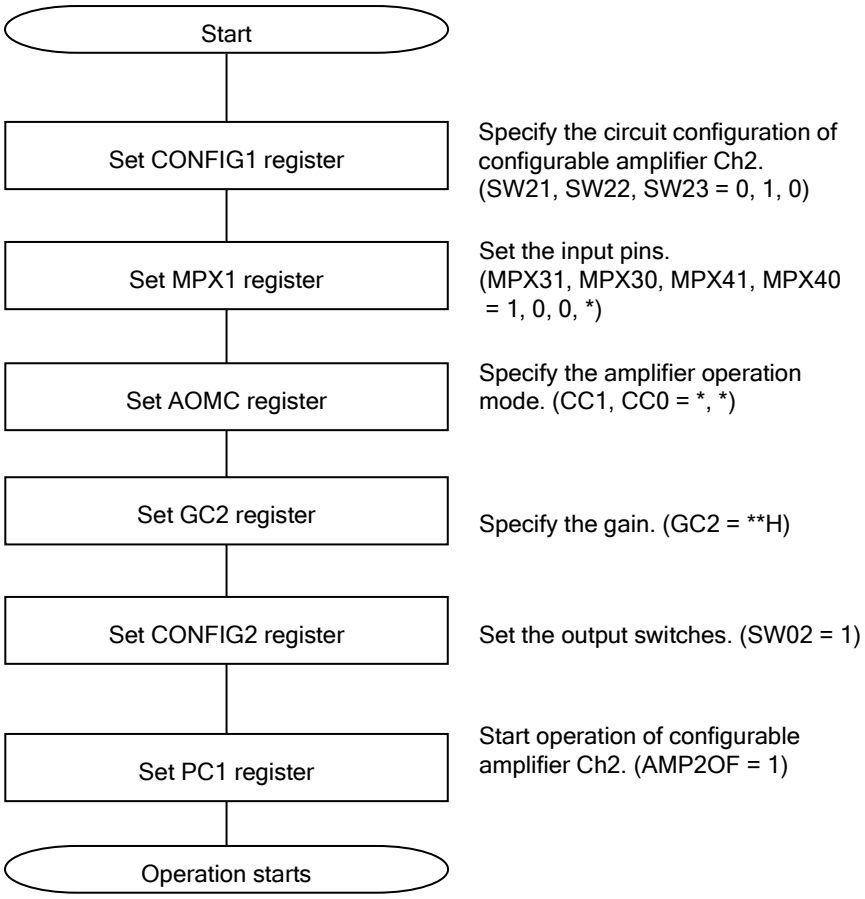
3. 21. 2 Configuration of voltage detector

The block diagram of the voltage detector is shown in Figure 3-15.

<R> **Figure 3-15. Block Diagram of Voltage Detector**

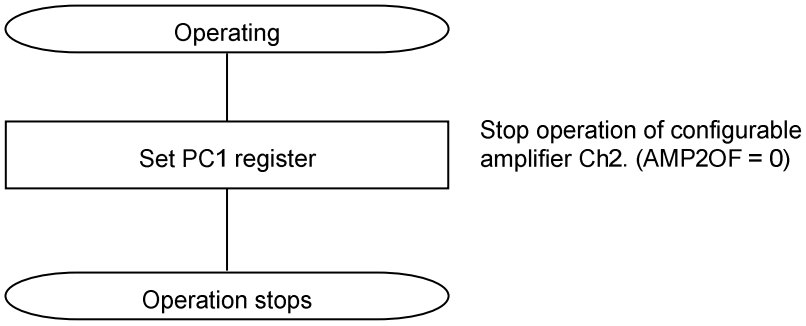


Example of procedure for starting configurable amplifier Ch2 (non-inverting amplifier)

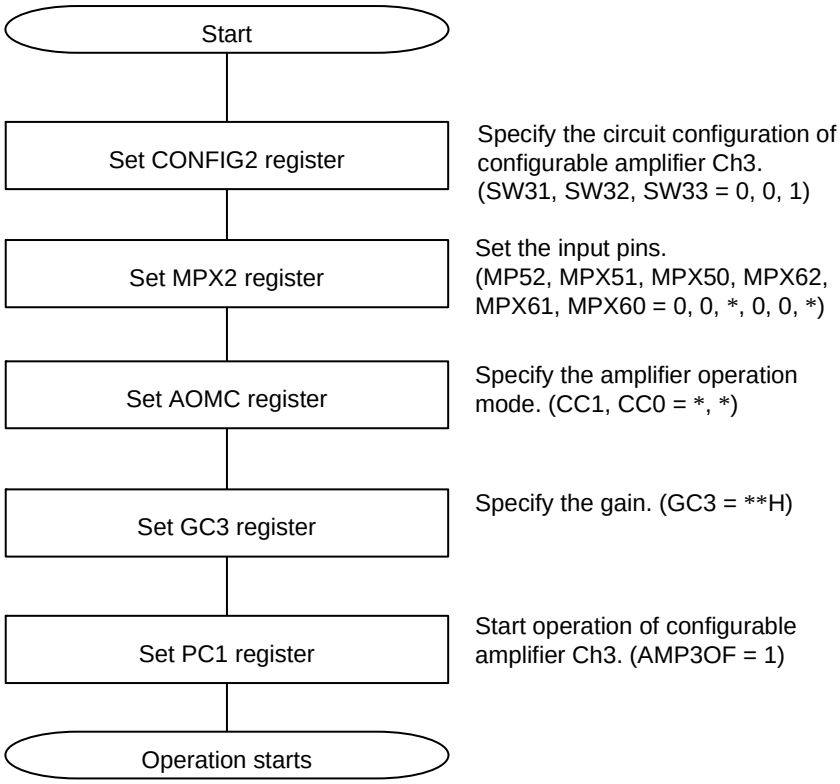


Remark *: don't care

Example of procedure for stopping configurable amplifier Ch2 (non-inverting amplifier)

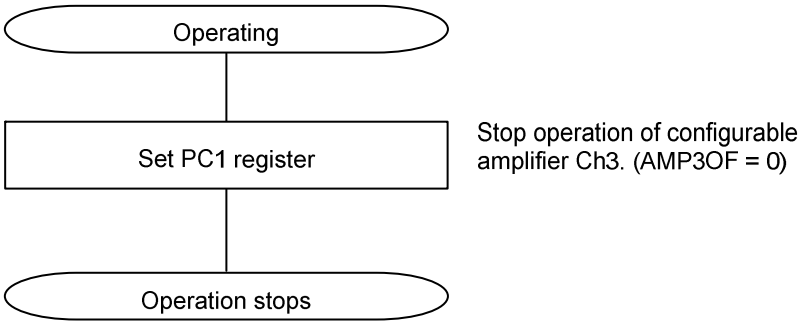


Example of procedure for starting configurable amplifier Ch3 (differential amplifier)



Remark *: don't care

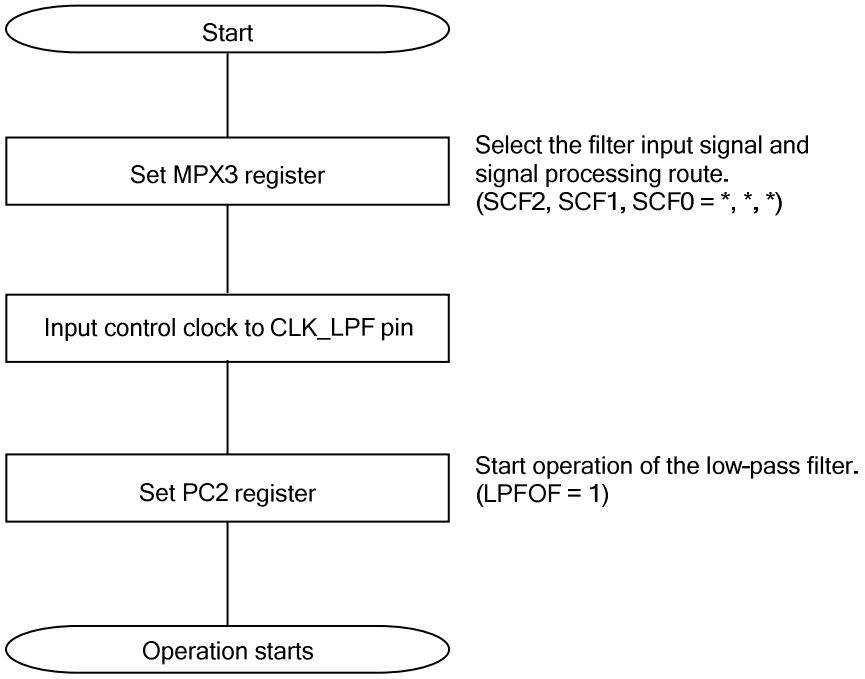
Example of procedure for stopping configurable amplifier Ch3 (differential amplifier)



4. 4. 4 Procedure for operating the low-pass filter

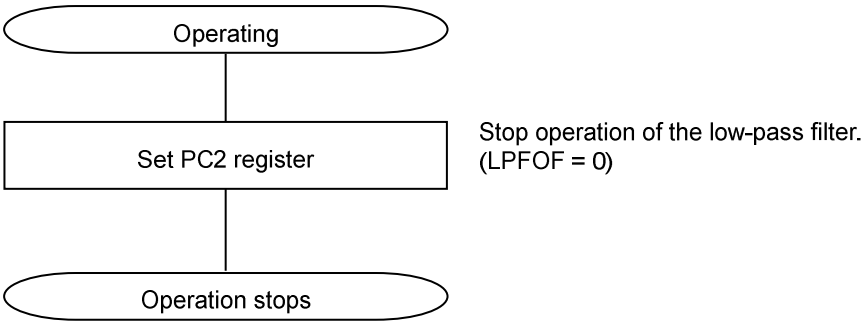
Follow the procedures below to start and stop the low-pass filter.

Example of procedure for starting the low-pass filter



Remark *: don't care

Example of procedure for stopping the low-pass filter



4 .6 Temperature Sensor

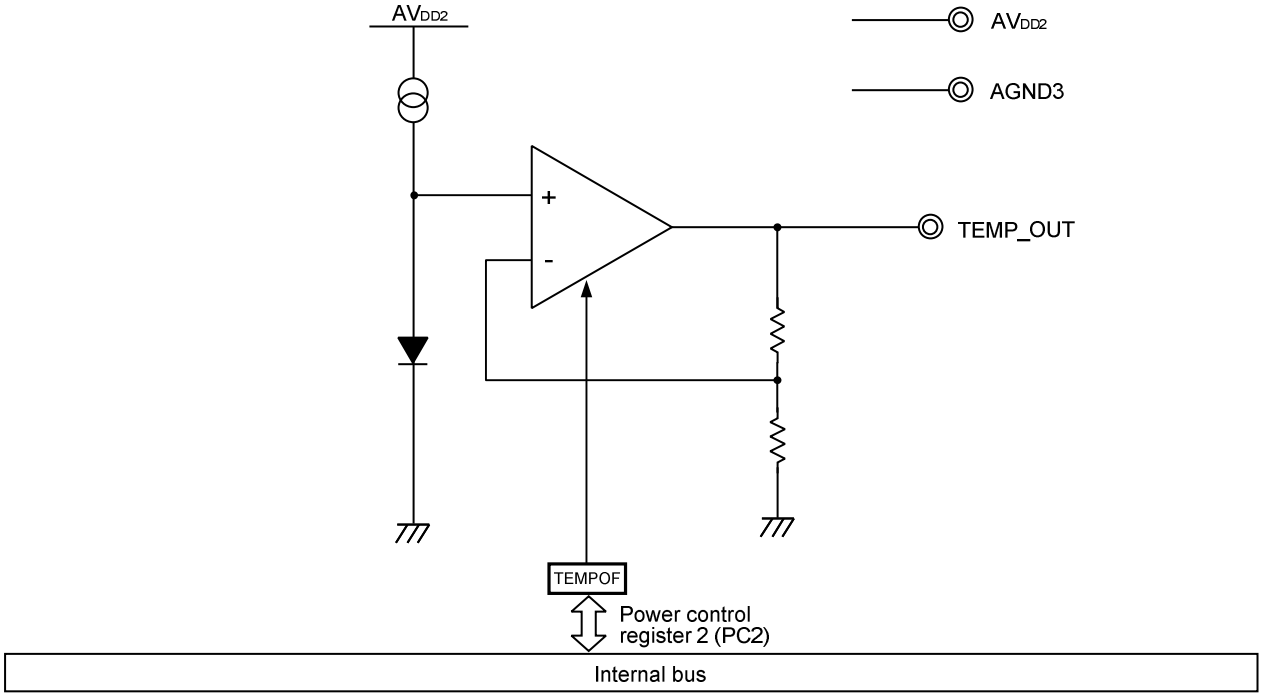
The RL78/G1E (64-pin products, 80-pin products) has one on-chip temperature sensor channel.

4. 6. 1 Overview of temperature sensor features

The features of temperature sensor are described below.

- Output voltage temperature coefficient: –5 mV/°C (Typ.)
- Includes a power-off function.

4. 6. 2 Block diagram



4. 7. 3 Registers controlling the variable output voltage regulator

The variable output voltage regulator is controlled by the following 2 registers:

- LDO control register (LDOC)
- Power control register 2 (PC2)

(1) LDO control register (LDOC)

This register is used to specify the output voltage of the variable output voltage regulator.

Reset signal input sets this register to 0DH.

Address: 0BH After reset: 0DH R/W

	7	6	5	4	3	2	1	0
LDOC	0	0	0	0	LDO3	LDO2	LDO1	LDO0

LDO3	LDO2	LDO1	LDO0	Output Voltage of Variable Output Voltage Regulator (Typ.)
0	0	0	0	2.0 V
0	0	0	1	2.1 V
0	0	1	0	2.2 V
0	0	1	1	2.3 V
0	1	0	0	2.4 V
0	1	0	1	2.5 V
0	1	1	0	2.6 V
0	1	1	1	2.7 V
1	0	0	0	2.8 V
1	0	0	1	2.9 V
1	0	1	0	3.0 V
1	0	1	1	3.1 V
1	1	0	0	3.2 V
1	1	0	1	3.3 V Note
Other than above				Setting prohibited

Note Output voltage of 3.3 V is available when the power supply voltage is more than 4 V.

<R> **Remark** Bits 7 to 4 are fixed at 0 of read only.

4. 9 SPI

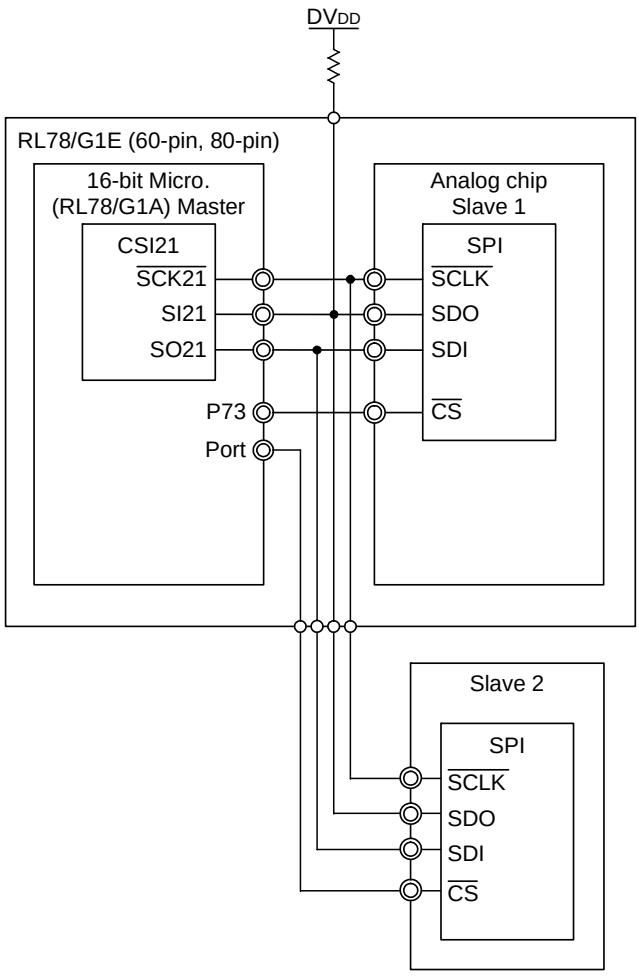
4. 9. 1 Overview of SPI features

The SPI interface is used to allow control from external devices by using clocked communication via four lines: a serial clock line ($\overline{\text{SCLK}}$), two serial data lines (SDI and SDO), and a chip select input line ($\overline{\text{CS}}$).

Data transmission/reception:

- 16-bit data unit
- MSB first

Figure 4-4. SPI Configuration Example



Caution After turning on DV_{DD}, be sure to generate external reset by inputting a reset signal to $\overline{\text{ARESET}}$ pin before starting SPI communication. For details, see 4.10 Analog Reset.

Table 4-12. Statuses during Analog Reset

Function Block	External Reset from $\overline{\text{ARESET}}$ Pin	Internal Reset by Reset Control Register (RC)
Configurable amplifier	Operation stops.	
Gain adjustment amplifier	Operation stops.	
D/A converter	Operation stops.	
Low-pass filter	Operation stops.	
High-pass filter Note	Operation stops.	
Temperature sensor	Operation stops.	
Variable output voltage regulator	Operation stops.	
Reference voltage generator	Operation stops.	
SPI	Operation stops.	Operation enabled.

Note 80-pin products only.

Table 4-13. Statuses of SPI Control Registers after Analog Reset Is Acknowledged

Address	SPI Control Register	Status After a Reset Is Acknowledged	
		External Reset	Internal Reset
00H	Configuration register 1 (CONFIG1)	00H	00H
01H	Configuration register 2 (CONFIG2)	00H	00H
03H	MPX setting register 1 (MPX1)	00H	00H
04H	MPX setting register 2 (MPX2)	00H	00H
05H	MPX setting register 3 (MPX3)	00H	00H
06H	Gain control register 1 (GC1)	00H	00H
07H	Gain control register 2 (GC2)	00H	00H
08H	Gain control register 3 (GC3)	00H	00H
09H	AMP operation mode control register (AOMC)	00H	00H
0AH	Gain control register 4 (GC4)	00H	00H
0BH	LDO control register (LDOC)	0DH	0DH
0CH	DAC reference voltage control register (DACRC)	00H	00H
0DH	DAC control register 1 (DAC1C)	80H	80H
0EH	DAC control register 2 (DAC2C)	80H	80H
0FH	DAC control register 3 (DAC3C)	80H	80H
10H	DAC control register 4 (DAC4C)	80H	80H
11H	Power control register 1 (PC1)	00H	00H
12H	Power control register 2 (PC2)	00H	00H
13H	Reset control register (RC)	00H	01H Note

<R> **Note** The reset control register is not initialized by generating internal reset of the reset control register, but it can be done to 00H by generating external reset from $\overline{\text{ARESET}}$ pin or writing 0 to the RESET bit of the reset control register (RC)..

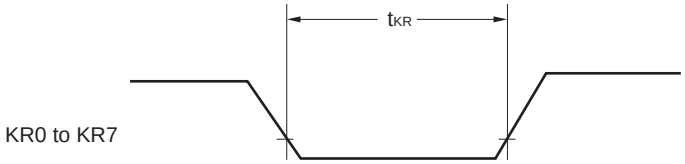
<R> **5. 1. 3 Absolute maximum ratings (common to microcontroller block and analog block)**

Absolute maximum ratings

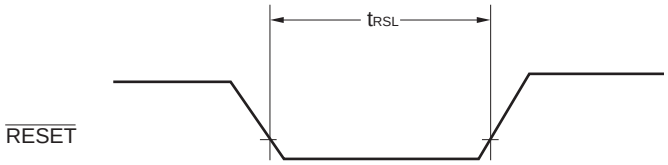
Parameter	Symbol	Conditions	Ratings	Unit
Operating ambient temperature	T_A	In normal operation mode	–40 to +85	°C
		In flash memory programming mode	–40 to +85	°C
Storage temperature	T_{stg}		–40 to +150	°C

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

Key Interrupt Input Timing



$\overline{\text{RESET}}$ Input Timing



<R> **(4) Communication between devices at same potential (CSI mode)**
(slave mode, SCKp ... External clock input) (2/2)

(T_A = –40 to +85°C, 1.6 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V) (2/2)

Parameter	Symbol	Conditions		HS Note 1		LS Note 2		LV Note 3		Unit
				MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
SIp setup time (to SCKp↑) Note 4	t_{SIK2}	2.7 V ≤ V_{DD} ≤ 5.5 V		1/f_{MCK} +20		1/f_{MCK} +30		1/f_{MCK} +30		ns
		1.8 V ≤ V_{DD} ≤ 5.5 V		1/f_{MCK} +30		1/f_{MCK} +30		1/f_{MCK} +30		ns
		1.7 V ≤ V_{DD} ≤ 5.5 V		1/f_{MCK} +40		1/f_{MCK} +40		1/f_{MCK} +40		ns
		1.6 V ≤ V_{DD} ≤ 5.5 V		–		1/f_{MCK} +40		1/f_{MCK} +40		ns
SIp hold time (from SCKp↑) Note 4	t_{KSI2}	1.8 V ≤ V_{DD} ≤ 5.5 V		1/f_{MCK} +31		1/f_{MCK} +31		1/f_{MCK} +31		ns
		1.7 V ≤ V_{DD} ≤ 5.5 V		1/f_{MCK} +250		1/f_{MCK} +250		1/f_{MCK} +250		ns
		1.6 V ≤ V_{DD} ≤ 5.5 V		–		1/f_{MCK} +250		1/f_{MCK} +250		ns
Delay time from SCKp↓ to SOp output Note 5	t_{KSO2}	C = 30 pF Note 6	2.7V ≤ V_{DD} ≤ 5.5V		2/f_{MCK} +44		2/f_{MCK} +110		2/f_{MCK} +110	ns
			2.4V ≤ V_{DD} ≤ 5.5V		2/f_{MCK} +75		2/f_{MCK} +110		2/f_{MCK} +110	ns
			1.8V ≤ V_{DD} ≤ 5.5V		2/f_{MCK} +110		2/f_{MCK} +110		2/f_{MCK} +110	ns
			1.7V ≤ V_{DD} ≤ 5.5V		2/f_{MCK} +220		2/f_{MCK} +220		2/f_{MCK} +220	ns
			1.6V ≤ V_{DD} ≤ 5.5V		–		2/f_{MCK} +220		2/f_{MCK} +220	ns

Notes 1. HS is condition of HS (high-speed main) mode.

2. LS is condition of LS (low-speed main) mode.

3. LV is condition of LV (low-voltage main) mode.

4. This indicates the time when DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. When DAPmn = 0 and CKPmn = 1 or DAPmn = 1 and CKPmn = 0, this specification refers to SCKp↓.

5. This indicates the time when DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. When DAPmn = 0 and CKPmn = 1 or DAPmn = 1 and CKPmn = 0, this specification refers to SCKp↑.

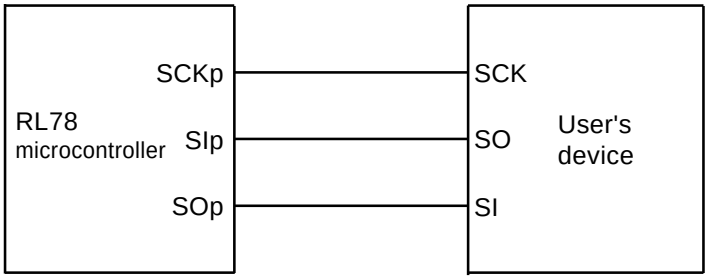
6. C is the load capacitance of the SOp output line.

Caution Select the normal input buffer for the SIp pin and SCKp pin and the normal output mode for the SOp pin by using port input mode register g (PIMg) and port output mode register g (POMg).

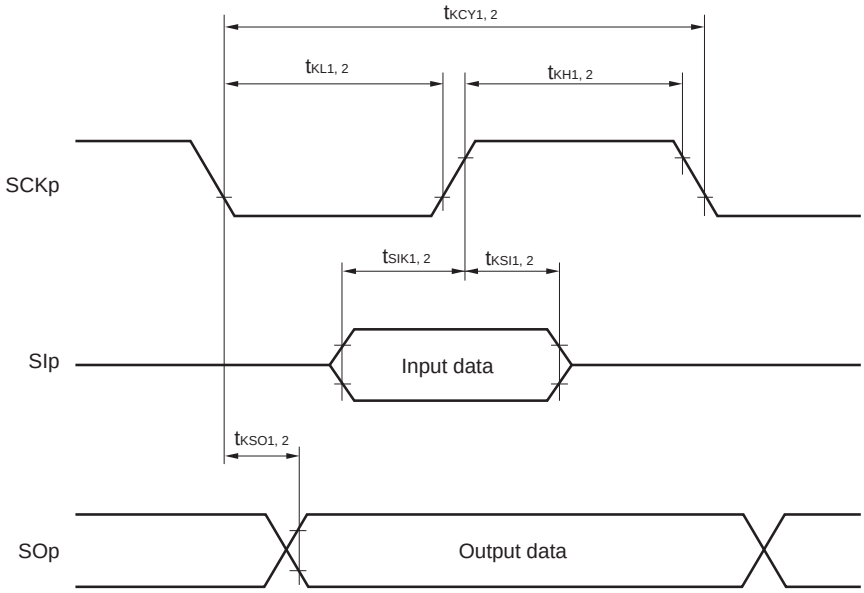
Remarks 1. p: CSI number (p = 00, 10, 20, 21), m: Unit number (m = 0, 1), n: Channel number (n = 0 to 2), g: PIM and POM numbers (g = 0, 1)

2. f_{MCK}: Serial array unit operating clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn).
m: Unit number, n: Channel number (mn = 00 to 03, 10, 11))

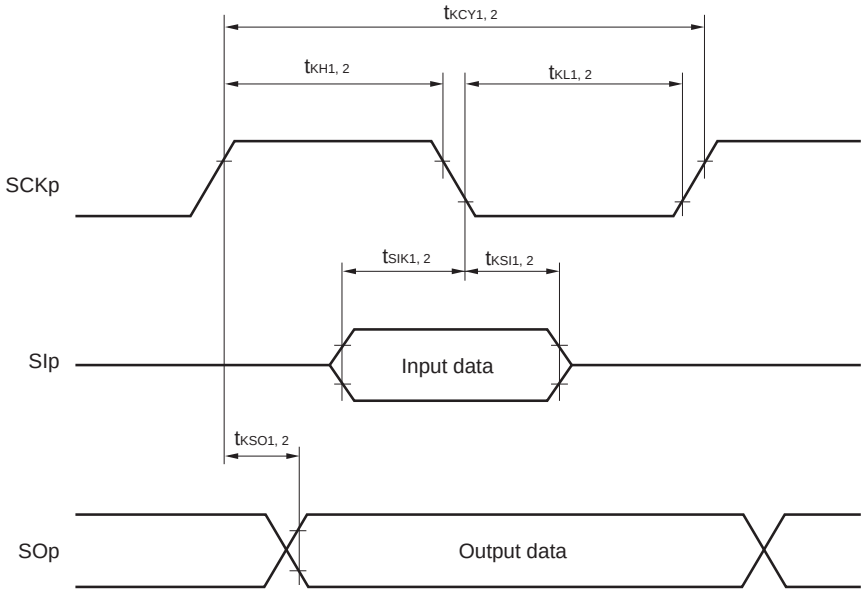
CSI mode connection diagram (during communication between devices with the same voltage)



CSI mode serial transfer timing (during communication between devices with the same voltage)
(when DAPmn = 0 and CKPmn = 0 or DAPmn = 1 and CKPmn = 1)



CSI mode serial transfer timing (during communication between devices with the same voltage)
(when DAPmn = 0 and CKPmn = 1 or DAPmn = 1 and CKPmn = 0)



Remarks 1. p: CSI number (p = 00, 10, 20, 21)

2. m: Unit number, n: Channel number (mn = 00 to 03, 10, 11)