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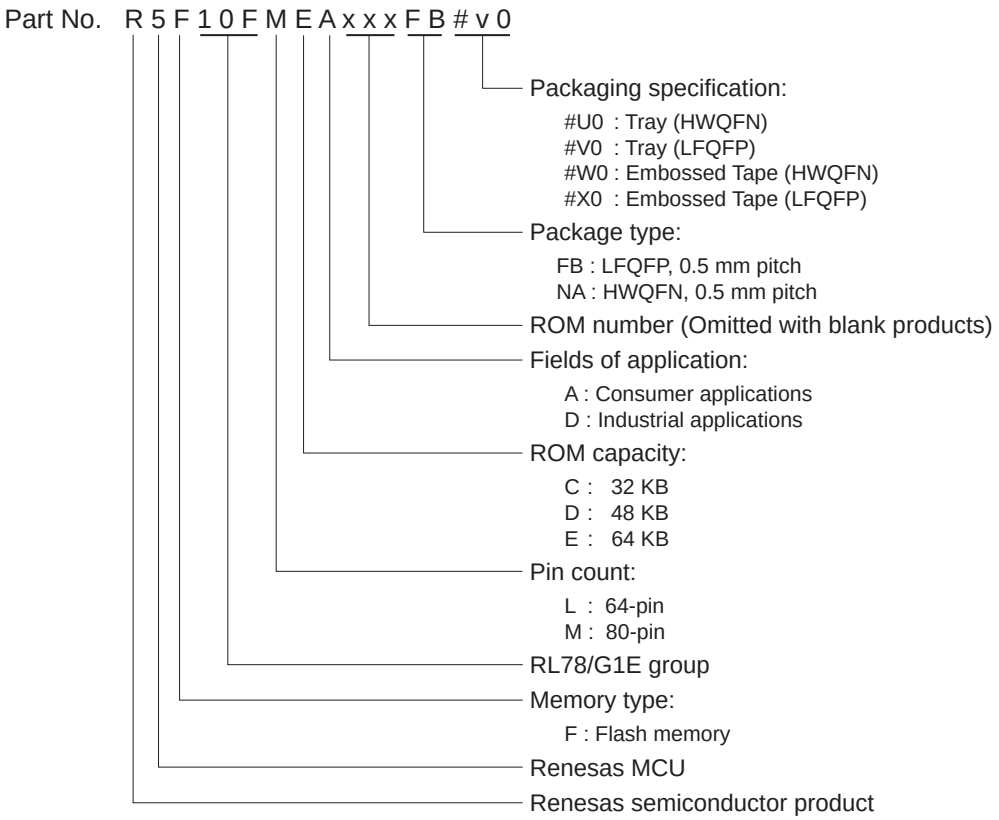
Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	RL78
Core Size	16-Bit
Speed	32MHz
Connectivity	CSI, I²C, LINbus, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	26
Program Memory Size	48KB (48K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	3K x 8
Voltage - Supply (Vcc/Vdd)	1.6V ~ 5.5V
Data Converters	A/D 17x8/12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	80-LQFP
Supplier Device Package	80-LFQFP (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f10fmddfb-x0

CONTENTS

1. 2 List of Part Numbers

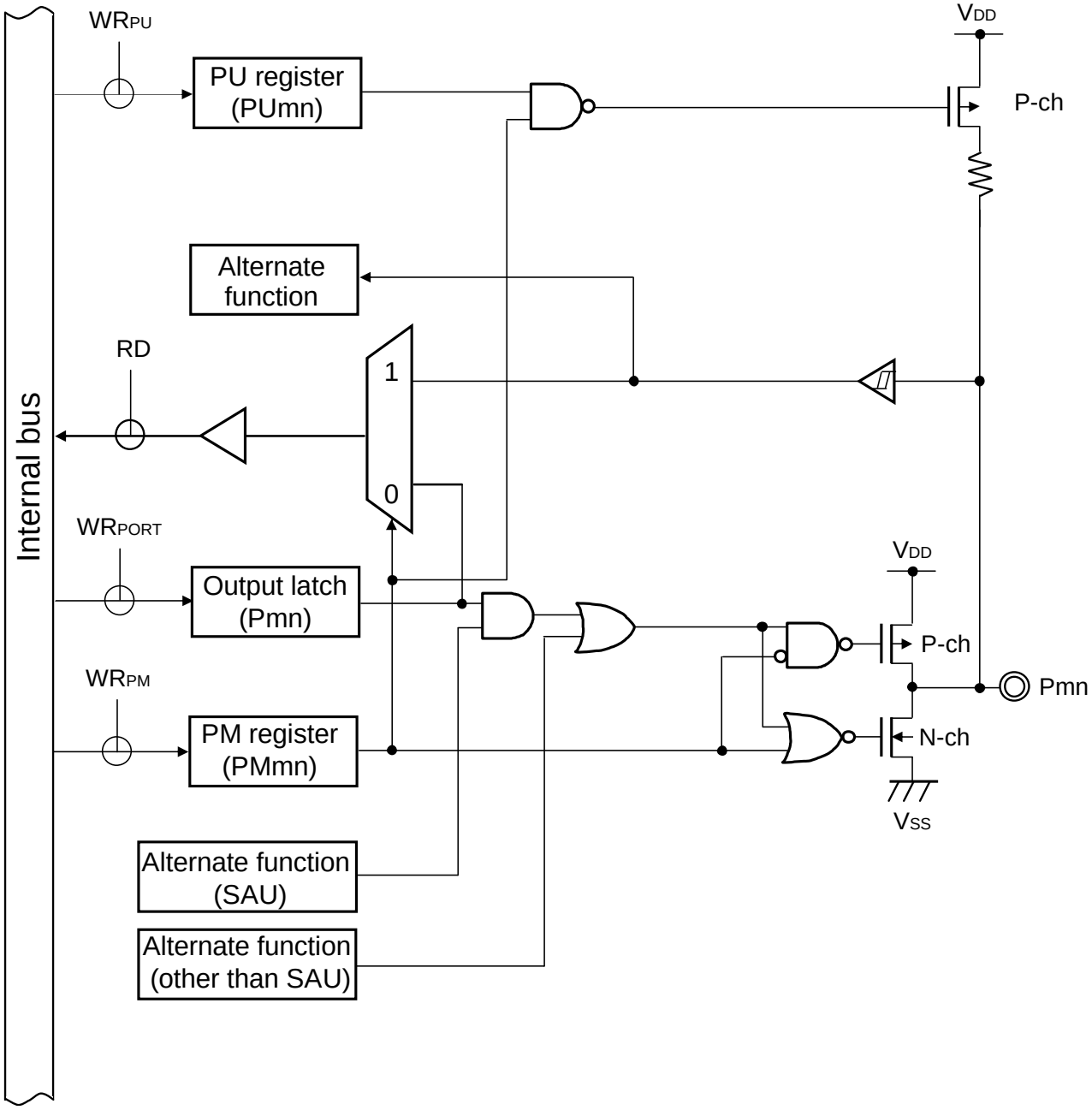


<R>

Pin count	Package	Data Flash	Part Number
64 pins	64-pin plastic HWQFN (fine pitch) (9 × 9)	Mounted	R5F10FLCANA#U0, R5F10FLCANA#W0, R5F10FLDANA#U0, R5F10FLDANA#W0, R5F10FLEANA#U0, R5F10FLEANA#W0, R5F10FLCDNA#U0, R5F10FLCDNA#W0, R5F10FLDDNA#U0, R5F10FLDDNA#W0, R5F10FLEDNA#U0, R5F10FLEDNA#W0
80 pins	80-pin plastic LFQFP (12 × 12)	Mounted	R5F10FMCAFB#V0, R5F10FMCAFB#X0, R5F10FMDAFB#V0, R5F10FMDAFB#X0, R5F10FMEAFB#V0, R5F10FMEAFB#X0, R5F10FMCDFB#V0, R5F10FMCDFB#X0, R5F10FMDDFB#V0, R5F10FMDDFB#X0, R5F10FMEDFB#V0, R5F10FMEDFB#X0

Caution The part number above is valid as of when this manual was issued. For the latest part number, see the web page of the target product on the Renesas Electronics website.

<R> **Figure 2-6. Pin Block Diagram for Pin Type 7-1-1**



Remarks 1. For alternate functions, see **2. 1. 1 Port functions**.

2. SAU: Serial array unit

3. 3. 2. 5 Expanded special function registers (2nd SFRs)

The differences in expanded special function registers (2nd SFRs) between RL78/G1E (64-pin products, 80-pin products) and RL78/G1A (64-pin products) are shown in the tables below.

(1) 64-pin products

Table 3-3. List of Differences in Expanded Special Function Registers (2nd SFRs) (1/6)

Address	RL78/G1E (64-pin products)		RL78/G1A (64-pin products)	
	2nd SFRs Name	Symbol	2nd SFRs Name	Symbol
F0010H	Same as RL78/G1A (64-pin products)	ADM2	A/D converter mode register 2	ADM2
F0011H	Same as RL78/G1A (64-pin products)	ADUL	Conversion result comparison upper limit setting register	ADUL
F0012H	Same as RL78/G1A (64-pin products)	ADLL	Conversion result comparison lower limit setting register	ADLL
F0013H	Same as RL78/G1A (64-pin products)	ADTES	A/D test register	ADTES
F0030H	Pull-up resistor option register 0 Note	PU0	Pull-up resistor option register 0	PU0
F0031H	Pull-up resistor option register 1 Note	PU1	Pull-up resistor option register 1	PU1
F0033H			Pull-up resistor option register 3	PU3
F0034H	Pull-up resistor option register 4 Note	PU4	Pull-up resistor option register 4	PU4
F0035H			Pull-up resistor option register 5	PU5
F0037H	Pull-up resistor option register 7 Note	PU7	Pull-up resistor option register 7	PU7
F003CH			Pull-up resistor option register 12	PU12
F003EH			Pull-up resistor option register 14	PU14
F0040H	Port input mode register 0 Note	PIM0	Port input mode register 0	PIM0
F0041H	Port input mode register 1 Note	PIM1	Port input mode register 1	PIM1
F0050H	Port output mode register 0 Note	POM0	Port output mode register 0	POM0
F0051H	Port output mode register 1 Note	POM1	Port output mode register 1	POM1
F0055H			Port output mode register 5	POM5
F0057H			Port output mode register 7	POM7
F0060H	Same as RL78/G1A (64-pin products)	PMC0	Port mode control register 0	PMC0
F0061H	Port mode control register 1 Note	PMC1	Port mode control register 1	PMC1
F0063H			Port mode control register 3	PMC3
F0064H	Same as RL78/G1A (64-pin products)	PMC4	Port mode control register 4	PMC4
F0065H			Port mode control register 5	PMC5
F0067H	Same as RL78/G1A (64-pin products)	PMC7	Port mode control register 7	PMC7
F006CH			Port mode control register 12	PMC12
F0070H	Same as RL78/G1A (64-pin products)	NFEN0	Noise filter enable register 0	NFEN0
F0071H	Noise filter enable register 1 Note	NFEN1	Noise filter enable register 1	NFEN1

Note The bit setting is different from that of RL78/G1A (64-pin products).

Caution Do not write data to the registers which is in the row with painted gray.

Table 3-3. List of Differences in Expanded Special Function Registers (2nd SFRs) (2/6)

Address	RL78/G1E (64-pin products)			RL78/G1A (64-pin products)		
	2nd SFRs Name	Symbol		2nd SFRs Name	Symbol	
F0073H	Same as RL78/G1A (64-pin products)	ISC		Input switch control register	ISC	
F0074H	Timer input select register 0 Note	TIS0		Timer input select register 0	TIS0	
F0076H	A/D port configuration register Note	ADPC		A/D port configuration register	ADPC	
F0077H	Peripheral I/O redirection register Note	PIOR		Peripheral I/O redirection register	PIOR	
F0078H	Same as RL78/G1A (64-pin products)	IAWCTL		Invalid memory access detection control register	IAWCTL	
F007CH	Same as RL78/G1A (64-pin products)	GAIDIS		Global analog input disable register	GAIDIS	
F007DH				Global digital input disable register	GDIDIS	
F0090H	Same as RL78/G1A (64-pin products)	DFLCTL		Data flash control register	DFLCTL	
F00A0H	Same as RL78/G1A (64-pin products)	HIOTRM		High-speed on-chip oscillator trimming register	HIOTRM	
F00A8H	Same as RL78/G1A (64-pin products)	HOCODIV		High-speed on-chip oscillator frequency select register	HOCODIV	
F00E0H	Same as RL78/G1A (64-pin products)	MDCL		Multiplication/division data register C (L)	MDCL	
F00E2H	Same as RL78/G1A (64-pin products)	MDCH		Multiplication/division data register C (H)	MDCH	
F00E8H	Same as RL78/G1A (64-pin products)	MDUC		Multiplication/division control register	MDUC	
F00F0H	Peripheral enable register 0 Note	PER0		Peripheral enable register 0	PER0	
<R> F00F3H	Subsystem clock supply mode control register Note	OSMC		Subsystem clock supply mode control register	OSMC	
F00F5H	Same as RL78/G1A (64-pin products)	RPECTL		RAM parity error control register	RPECTL	
F00FEH	Same as RL78/G1A (64-pin products)	BCDADJ		BCD adjust result register	BCDADJ	
F0100H	Same as RL78/G1A (64-pin products)	SSR00L	SSR00	Serial status register 00	SSR00L	SSR00
F0101H		—			—	
F0102H	Same as RL78/G1A (64-pin products)	SSR01L	SSR01	Serial status register 01	SSR01L	SSR01
F0103H		—			—	
F0104H	Same as RL78/G1A (64-pin products)	SSR02L	SSR02	Serial status register 02	SSR02L	SSR02
F0105H		—			—	
F0106H	Same as RL78/G1A (64-pin products)	SSR03L	SSR03	Serial status register 03	SSR03L	SSR03
F0107H		—			—	
F0108H	Same as RL78/G1A (64-pin products)	SIR00L	SIR00	Serial flag clear trigger register 00	SIR00L	SIR00
F0109H		—			—	
F010AH	Same as RL78/G1A (64-pin products)	SIR01L	SIR01	Serial flag clear trigger register 01	SIR01L	SIR01
F010BH		—			—	
F010CH	Same as RL78/G1A (64-pin products)	SIR02L	SIR02	Serial flag clear trigger register 02	SIR02L	SIR02
F010DH		—			—	
F010EH	Same as RL78/G1A (64-pin products)	SIR03L	SIR03	Serial flag clear trigger register 03	SIR03L	SIR03
F010FH		—			—	

Note The bit setting is different from that of RL78/G1A (64-pin products).

Caution Do not write data to the registers which is in the row with painted gray.

3. 6. 3. 3 Timer mode register mn (TMRmn)

- Format of Timer Mode Register mn (TMRmn) (1/4)

Address: F0190H, F0191H (TMR00) - F019EH, F019FH (TMR07) After reset: 0000H R/W

Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TMRmn (n = 2, 4, 6)	CKS mn1	CKS mn0	0	CCS mn	MAS TER mn	STS mn2	STS mn1	STS mn0	CIS mn1	CIS mn0	0	0	MD mn3	MD mn2	MD mn1	MD mn0

Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TMRmn (n = 1, 3)	CKS mn1	CKS mn0	0	CCS mn	SPLIT mn	STS mn2	STS mn1	STS mn0	CIS mn1	CIS mn0	0	0	MD mn3	MD mn2	MD mn1	MD mn0

Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TMRmn (n = 0, 5, 7)	CKS mn1	CKS mn0	0	CCS mn	0Note	STS mn2	STS mn1	STS mn0	CIS mn1	CIS mn0	0	0	MD mn3	MD mn2	MD mn1	MD mn0

CKSmn1	CKSmn0	Selection of operation clock (f_{MCK}) of channel n
0	0	Operation clock CKm0 set by timer clock select register m (TPSm)
0	1	Operation clock CKm2 set by timer clock select register m (TPSm)
1	0	Operation clock CKm1 set by timer clock select register m (TPSm)
1	1	Operation clock CKm3 set by timer clock select register m (TPSm)
Operation clock (f_{MCK}) is used by the edge detector. A count clock (f_{TCLK}) and a sampling clock are generated depending on the setting of the CCSmn bit. The operation clocks CKm2 and CKm3 can only be selected for channels 1 and 3.		

CCSmn	Selection of count clock (f_{TCLK}) of channel n
0	Operation clock (f_{MCK}) specified by the CKSmn0 and CKSmn1 bits
1	Valid edge of input signal input from the TImn pin When channel 5 is used, the valid edge of the input signal selected by the TIS0
Count clock (f_{TCLK}) is used for the timer/counter, output controller, and interrupt controller.	

<R> **Note** Bit 11 is fixed at 0 of read only, write is ignored.

Cautions 1. Be sure to clear bits 13, 5, and 4 to "0".

2. The timer array unit must be stopped (TTm = 00FFH) if the clock selected for f_{CLK} is changed (by changing the value of the system clock control register (CKC)), even if the operating clock specified by using the CKSmn0 and CKSmn1 bits (f_{MCK}) or the valid edge of the signal input from the TImn pin is selected as the count clock (f_{TCLK}).

Remark m: Unit number (m = 0), n: Channel number (n = 0 to 7 (however, timer input pin (TImn), timer output pin (TOmn): n = 0, 4, 7))

3. 11. 3. 3 A/D converter mode register 1 (ADM1)

Address: FFF32H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
ADM1	ADTMD1	ADTMD0	ADSCM	0	0	0	ADTRS1	ADTRS0

<R>

ADTMD1	ADTMD0	Selection of the A/D conversion trigger mode
0	×	Software trigger mode
1	0	Hardware trigger no-wait mode
1	1	Hardware trigger wait mode

ADSCM	Specification of the A/D conversion mode
0	Sequential conversion mode
1	One-shot conversion mode

ADTRS1	ADTRS0	Selection of the hardware trigger signal
0	0	End of timer channel 1 count or capture interrupt signal (INTTM01)
0	1	Setting prohibited
1	0	Setting prohibited
1	1	Interval timer interrupt signal (INTIT)

Cautions 1. Rewrite the value of the ADM1 register while conversion is stopped (ADCS = 0, ADCE = 0).

<R>

2. To complete A/D conversion, specify at least the following time as the hardware trigger interval:
Hardware trigger no wait mode: 2 f_{CLK} clock + A/D conversion time
Hardware trigger wait mode: 2 f_{CLK} clock + A/D power supply stabilization wait time +A/D conversion time

3. In modes other than SNOOZE mode, input of the next INTRTC or INTIT will not be recognized as a valid hardware trigger for up to four f_{CLK} cycles after the first INTRTC or INTIT is input.

Remarks 1. ×: don't care

2. f_{CLK}: CPU/peripheral hardware clock frequency

- Setting of serial communication operation setting register mn (SCRmn) (2/2)

<R> Address: F0118H, F0119H (SCR00) - F011EH, F011FH (SCR03), After reset: 0087H R/W
F0158H, F0159H (SCR10), F015AH, F015BH (SCR11)

Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SCRmn	TXE mn	RXE mn	DAP mn	CKP mn	0	EOC mn	PTC mn1	PTC mn0	DIR mn	0	SLC mn1 Note 1	SLC mn0	0	1	DLS mn1 Note 2	DLS mn0

PTCmn1	PTCmn0	Setting of parity bit in UART mode	
		Transmission	Reception
0	0	Does not output the parity bit.	Receives without parity
0	1	Outputs 0 parity Note 3.	No parity judgment
1	0	Outputs even parity.	Judged as even parity.
1	1	Outputs odd parity.	Judges as odd parity.
Be sure to set PTCmn1, PTCmn0 = 0, 0 in the CSI mode and simplified I^2C mode.			

DIRmn	Selection of data transfer sequence in CSI and UART modes
0	Inputs/outputs data with MSB first.
1	Inputs/outputs data with LSB first.
Be sure to clear DIRmn = 0 in the simplified I^2C mode.	

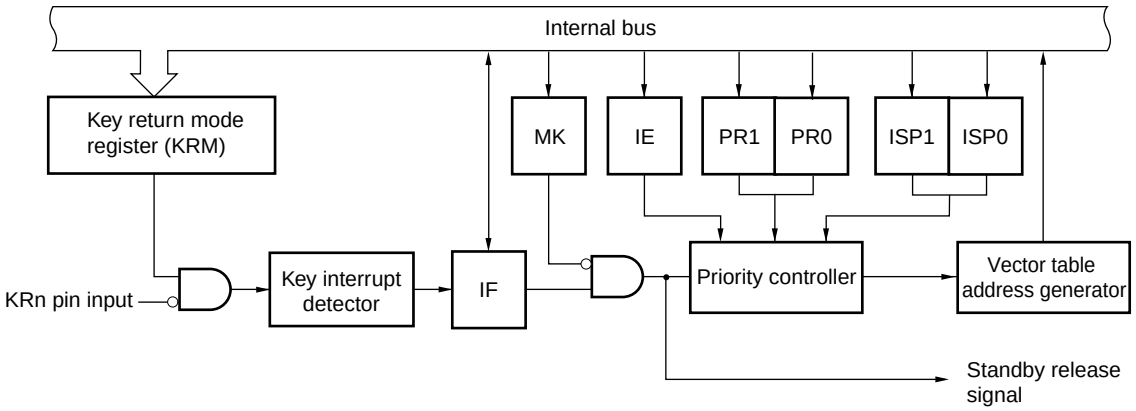
SLCmn1 Note 1	SLCmn0	Setting of stop bit in UART mode
0	0	No stop bit
0	1	Stop bit length = 1 bit
1	0	Stop bit length = 2 bits (mn = 00, 02, 10 only)
1	1	Setting prohibited
When the transfer end interrupt is selected, the interrupt is generated when all stop bits have been completely transferred. Set 1 bit (SLCmn1, SLCmn0 = 0, 1) during UART reception and in the simplified I^2C mode. Set no stop bit (SLCmn1, SLCmn0 = 0, 0) in the CSI mode.		

DLSmn1 Note 2	DLSmn0	Setting of data length in CSI and UART modes
0	1	9-bit data length (stored in bits 0 to 8 of the SDRmn register) (settable in UART mode only)
1	0	7-bit data length (stored in bits 0 to 6 of the SDRmn register)
1	1	8-bit data length (stored in bits 0 to 7 of the SDRmn register)
Other than above		Setting prohibited
Be sure to set DLSmn1, DLSmn0 = 1, 1 in the simplified I^2C mode.		

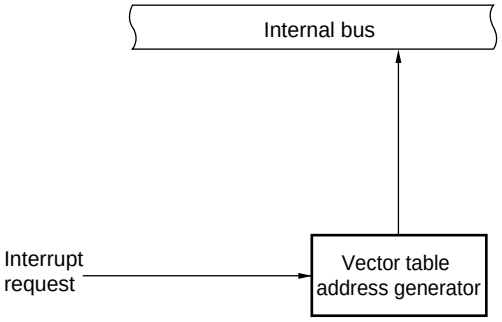
(**Notes**, **Caution** and **Remark** are on the next page.)

Figure 3-13. Basic Configuration of Interrupt Function (2/2)

(c) External maskable interrupt (INTKR)



(d) Software interrupt



IF: Interrupt request flag
IE: Interrupt enable flag
ISP0: In-service priority flag 0
ISP1: In-service priority flag 1
MK: Interrupt mask flag
PR0: Priority specification flag 0
PR1: Priority specification flag 1

Remark 64-pin products: n = 0 to 6
80-pin products: n = 0 to 7

Table 3-14. Flags Corresponding to Interrupt Request Sources (4/4)

Interrupt Source	Interrupt Request Flag	Register	Interrupt Mask Flag	Register	Priority Specification Flag	Register	RL78/G1E 64-pin	RL78/G1E 80-pin
INTTM05	TMIF05	IF2L	TMMK05	MK2L	TMPR005, TMPR105	PR02L, PR12L	√	√
INTTM06	TMIF06		TMMK06		TMPR006, TMPR106		√	√
INTTM07	TMIF07		TMMK07		TMPR007, TMPR107		√	√
INTP6	PIF6		PMK6		PPR06, PPR16		–	√
INTP7	PIF7		PMK7		PPR07, PPR17		–	–
INTP8	PIF8		PMK8		PPR08, PPR18		–	–
INTP9	PIF9		PMK9		PPR09, PPR19		–	–
INTP10	PIF10		PMK10		PPR010, PPR110		–	–
INTP11	PIF11	IF2H	PMK11	MK2H	PPR011, PPR111	PR02H, PR12H	–	–
INTMD	MDIF		MDMK		MDPR0, MDPR1		√	√
INTFL	FLIF		FLMK		FLPR0, FLPR1		√	√

The bit settings which are different from that of RL78/G1A (64-pin products) are shown on the next page. For details of each register, see **16. 3 Registers Controlling Interrupt Functions** in **RL78/G1A Hardware User's Manual (R01UH0305E)**.

Address: FFFD8H After reset: FFH R/W

Symbol	7	6	5	4	<3>	<2>	<1>	<0>
PR02L	1	1	1	1	PPR06	TMPR007	TMPR006	TMPR005

Address: FFFDCH After reset: FFH R/W

Symbol	7	6	5	4	<3>	<2>	<1>	<0>
PR12L	1	1	1	1	PPR16	TMPR107	TMPR106	TMPR105

Address: FFFD9H After reset: FFH R/W

Symbol	<7>	6	<5>	4	3	2	1	0
PR02H	FLPR0	1	MDPR0	1	1	1	1	1

Address: FFFDDH After reset: FFH R/W

Symbol	<7>	6	<5>	4	3	2	1	0
PR12H	FLPR1	1	MDPR1	1	1	1	1	1

Cautions 1. Be sure to set bits 5 to 7 of the PR00L register to “1”.

2. Be sure to set bits 5 to 7 of the PR10L register to “1”.

3. Be sure to set bit 3 of the PR01L register to “1”.

4. Be sure to set bit 3 of the PR11L register to “1”.

5. Be sure to set bits 1 and 4 to 6 of the PR01H register to “1”.

6. Be sure to set bits 1 and 4 to 6 of the PR11H register to “1”.

7. Be sure to set bits 4 to 7 of the PR02L register to “1”.

8. Be sure to set bits 4 to 7 of the PR12L register to “1”.

9. Be sure to set bits 4 to 7 of the PR02H register to “1”.

10. Be sure to set bits 0 to 4 and 6 of the PR12H register to “1”.

3. 17 Key Interrupt Function

The number of key interrupt input channels differs, depending on the product.

	64-pin products	80-pin products
Key interrupt input channels	4 ch (7 ch)	4 ch (8 ch)

Remarks 1. Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR).

2. Most of the following descriptions in this section use the case of 80-pin products as an example.

3. 17. 1 Functions of key interrupt

A key interrupt (INTKR) can be generated by inputting a rising/falling edge to the key interrupt input pins (KR0 to KR7).

There are two ways to identify the channel(s) to which a valid edge has been input:

- Identify the channel(s) (KR0 to KR7) by using the port input level.
- Identify the channel(s) (KR0 to KR5) by using the key interrupt flag.

Table 3-16. Assignment of Key Interrupt Detection Pins

Key Interrupt Pins	Key return mode register (KRM0)	Key return flag register (KRF)
KR0	KRM00	KRF0
KR1	KRM01	KRF1
KR2	KRM02	KRF2
KR3	KRM03	KRF3
KR4	KRM04	KRF4
KR5	KRM05	KRF5
KR6	KRM06	–
KR7	KRM07	–

Remark KR0 to KR3 (KR0 to KR6): 64-pin products
KR0 to KR3 (KR0 to KR7): 80-pin products
Functions in parentheses can be assigned via settings in the peripheral I/O redirection register (PIOR)

3. 17. 2 Configuration of key interrupt

The key interrupt includes the following hardware.

Table 3-17. Configuration of Key Interrupt

Item	Configuration
Control register	Key interrupt control register (KRCTL)
	Key interrupt mode control register 0 (KRM0)
	Key interrupt flag register (KRF)
	Port mode registers 0, 1, 2, 7 (PM0, PM1, PM2, PM7)
	Peripheral I/O redirection register (PIOR)

3. 20 Power-On-Reset Circuit

See **CHAPTER 20 POWER-ON-RESET CIRCUIT** in **RL78/G1A Hardware User's Manual (R01UH0305E)**.

3. 21. 3 Registers controlling voltage detector

The bit settings which are different from that of RL78/G1A (64-pin products) are shown below. For details of each register, see **21. 3 Registers Controlling Voltage Detector** in **RL78/G1A Hardware User's Manual (R01UH0305E)**.

3. 21. 3. 1 Voltage detection register (LVIM)

The bit setting is same as that of RL78/G1A (64-pin products). For details, see **21. 3. 1 Voltage detection register (LVIM)** in **RL78/G1A Hardware User's Manual (R01UH0305E)**.

3. 21. 3. 2 Voltage detection level register (LVIS)

The bit setting is same as that of RL78/G1A (64-pin products). For details, see **21. 3. 2 Voltage detection level register (LVIS)** in **RL78/G1A Hardware User's Manual (R01UH0305E)**.

5. 1. 2 Absolute maximum ratings of analog block

Absolute maximum ratings (T_A = 25°C)

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage	AV_{DDA}	AV_{DD1}, AV_{DD2}, AV_{DD3}	–0.3 to +6.0	V
	DV_{DD}	DV_{DD}	–0.3 to +6.0	V
	AGND	AGND1, AGND2, AGND3, AGND4	–0.3 to +0.3	V
	DGND	DGND	–0.3 to +0.3	V
Input voltage	V_{I1}	MPXIN10, MPXIN11, MPXIN20, MPXIN21, MPXIN30, MPXIN31, MPXIN40, MPXIN41, MPXIN50, MPXIN51, MPXIN60, MPXIN61, SC_IN, CLK_SYNCH, VREFIN1, VREFIN2, VREFIN3, VREFIN4, CLK_LPF, CLK_HPF, $\overline{\text{RESET}}$	–0.3 to AV_{DDA} + 0.3[Note]	V
	V_{I2}	$\overline{\text{SCLK}}$, SDI, $\overline{\text{CS}}$	–0.3 to DV_{DD} + 0.3[Note]	V
Output voltage	V_{O1}	LDO_OUT, BGR_OUT, AMP1_OUT, AMP2_OUT, AMP3_OUT, GAINAMP_OUT, SYNCH_OUT, LPF_OUT, HPF_OUT, DAC1_OUT, DAC2_OUT, DAC3_OUT, DAC4_OUT, TEMP_OUT	–0.3 to AV_{DDA} + 0.3[Note]	V
	V_{O2}	SDO	–0.3 to DV_{DD} + 0.3[Note]	V
Output current	I_{O1}	AMP1_OUT, AMP2_OUT, AMP3_OUT, GAINAMP_OUT, SYNCH_OUT LPF_OUT, HPF_OUT DAC1_OUT, DAC2_OUT, DAC3_OUT, DAC4_OUT, TEMP_OUT	1	mA
	I_{O2}	SDO	–10	mA
	I_{LDOOUT}	LDO_OUT	15	mA

Note Must be 6.0 V or lower.

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

<R> (3) When reference voltage (+) = AV_{DD} (ADREFP1 = 0, ADREFP0 = 0), reference voltage (–) = AV_{SS} (ADREFM = 0), target for conversion: ANI0 to ANI4 (ANI pins that use AV_{DD} as their power source)

(T_A = –40 to +85°C, 1.6 V ≤ V_{DD} ≤ 5.5 V, 1.6 V ≤ AV_{DD} ≤ 3.6 V, AV_{DD} ≤ V_{DD}, V_{SS} = 0 V, AV_{SS} = 0 V, reference voltage (+) = AV_{DD}, reference voltage (–) = AV_{SS} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Resolution	R_{ES}		2.4 V ≤ AV_{DD} ≤ 3.6 V	8		12	bit
			1.8 V ≤ AV_{DD} ≤ 3.6 V	8		10 Note 1	
			1.6 V ≤ AV_{DD} ≤ 3.6 V	8 Note 2			
Overall error Note 3	AINL	12-bit resolution	2.4 V ≤ AV_{DD} ≤ 3.6 V			±7.5	LSB
		10-bit resolution	1.8 V ≤ AV_{DD} ≤ 3.6 V			±5.5	
		8-bit resolution	1.6 V ≤ AV_{DD} ≤ 3.6 V			±3.0	
Conversion time	t_{CONV}	ADTYP = 0, 12-bit resolution	2.4 V ≤ AV_{DD} ≤ 3.6 V	3.375			μs
		ADTYP = 0, 10-bit resolution Note 1	1.8 V ≤ AV_{DD} ≤ 3.6 V	6.75			
		ADTYP = 0, 8-bit resolution Note 2	1.6 V ≤ AV_{DD} ≤ 3.6 V	13.5			
		ADTYP = 1, 8-bit resolution	2.4 V ≤ AV_{DD} ≤ 3.6 V	2.5625			
			1.8 V ≤ AV_{DD} ≤ 3.6 V	5.125			
			1.6 V ≤ AV_{DD} ≤ 3.6 V	10.25			
Zero-scale error Notes 3	EZS	12-bit resolution	2.4 V ≤ AV_{DD} ≤ 3.6 V			±6.0	LSB
		10-bit resolution	1.8 V ≤ AV_{DD} ≤ 3.6 V			±5.0	
		8-bit resolution	1.6 V ≤ AV_{DD} ≤ 3.6 V			±2.5	
Full-scale error Notes 3	EFS	12-bit resolution	2.4 V ≤ AV_{DD} ≤ 3.6 V			±6.0	LSB
		10-bit resolution	1.8 V ≤ AV_{DD} ≤ 3.6 V			±5.0	
		8-bit resolution	1.6 V ≤ AV_{DD} ≤ 3.6 V			±2.5	
Integral linearity error Note 3	ILE	12-bit resolution	2.4 V ≤ AV_{DD} ≤ 3.6 V			±3.0	LSB
		10-bit resolution	1.8 V ≤ AV_{DD} ≤ 3.6 V			±2.0	
		8-bit resolution	1.6 V ≤ AV_{DD} ≤ 3.6 V			±1.5	
Differential linearity error Note 3	DLE	12-bit resolution	2.4 V ≤ AV_{DD} ≤ 3.6 V			±2.0	LSB
		10-bit resolution	1.8 V ≤ AV_{DD} ≤ 3.6 V			±2.0	
		8-bit resolution	1.6 V ≤ AV_{DD} ≤ 3.6 V			±1.5	
Analog input voltage	V_{AIN}			0		AV_{DD}	V

Notes 1. The lower 2 bits of the ADCR register cannot be used.

2. The lower 4 bits of the ADCR register cannot be used.

3. Excludes quantization error (±1/2 LSB).

5. 3. 3. 4 Low-pass filter characteristics

($-40°C \le T_A \le 85°C$, $AV_{DD1} = AV_{DD2} = AV_{DD3} = AV_{DD4} = DV_{DD} = 5.0$ V, LPFOF = 1)

Parameter	Symbol	Conditions	Ratings			Unit
			MIN.	TYP.	MAX.	
Current consumption	IccA		–	800	1800	μA
Input voltage	V_{ILLPF}		AGND4 +0.2	–	–	V
	V_{IHLPF}		–	–	AV_{DD3} -1.5	V
Output voltage	V_{OLLPF}	IOL = –200 μA	–	AGND4 +0.22	AGND4 +0.25	V
	V_{OHLPF}	IOH = 200 μA	AV_{DD3} -1.55	AV_{DD3} -1.52	–	V
Cutoff frequency	fc1	f_{CLK_LPF} = 2 kHz	–	9	–	Hz
	fc2	f_{CLK_LPF} = 1 MHz	–	4.5	–	kHz
CLK_LPF low-level input voltage	V_{ILCLK_LPF}				$0.3 \times AV_{DD3}$	V
CLK_LPF high-level input voltage	V_{IHCLK_LPF}		$0.7 \times AV_{DD3}$			V
CLK_LPF Input frequency	f_{CLK_LPF}		2	–	1000	kHz
<R> CLK_LPF Input low-level-width Input high-level-width	t_{ILW_LPF} t_{IHW_LPF}		200	–	–	ns

Clock Timing