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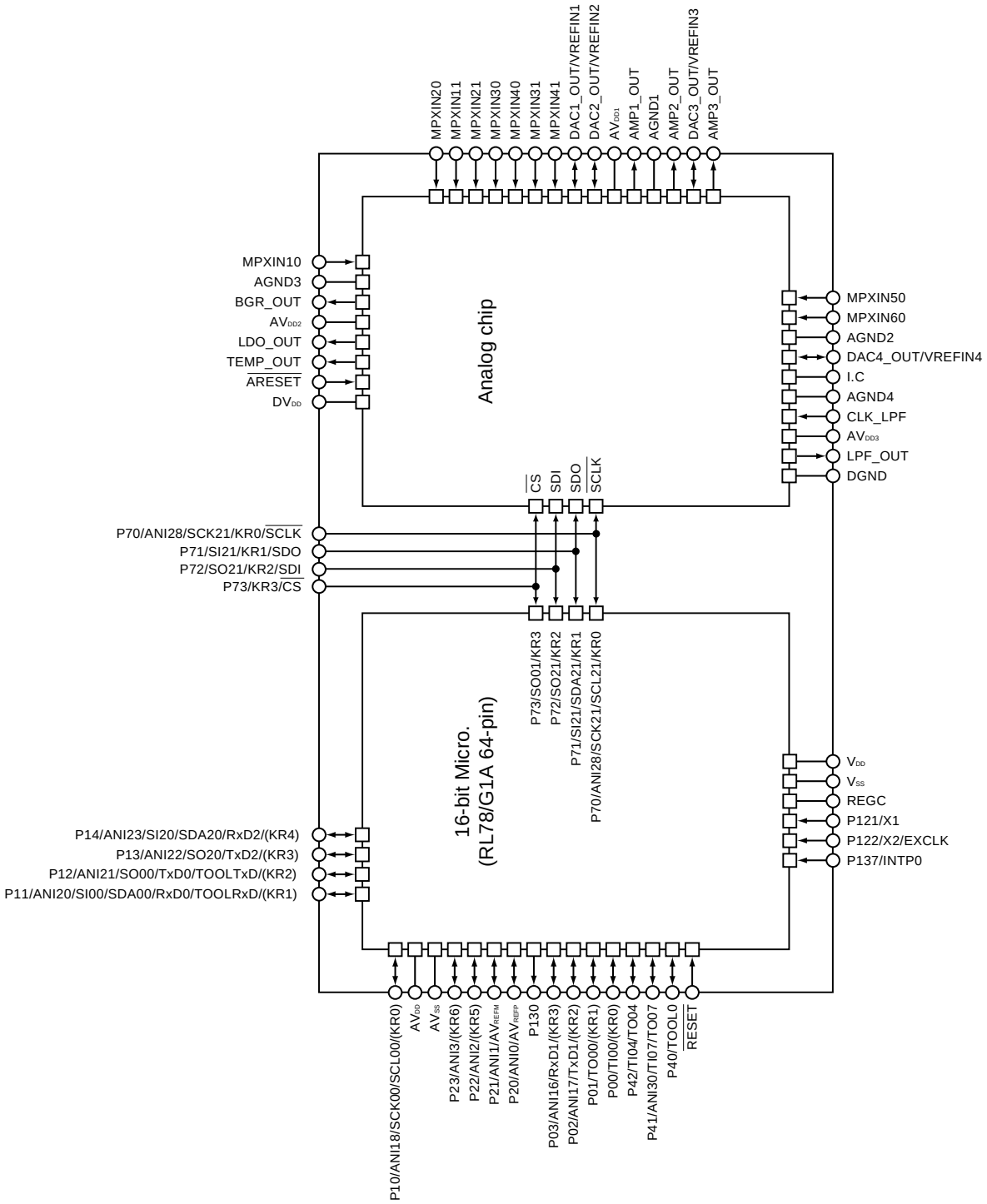
"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	RL78
Core Size	16-Bit
Speed	32MHz
Connectivity	CSI, I²C, LINbus, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	26
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	1.6V ~ 5.5V
Data Converters	A/D 17x8/12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	80-LQFP
Supplier Device Package	80-LFQFP (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f10fmeafb-v0

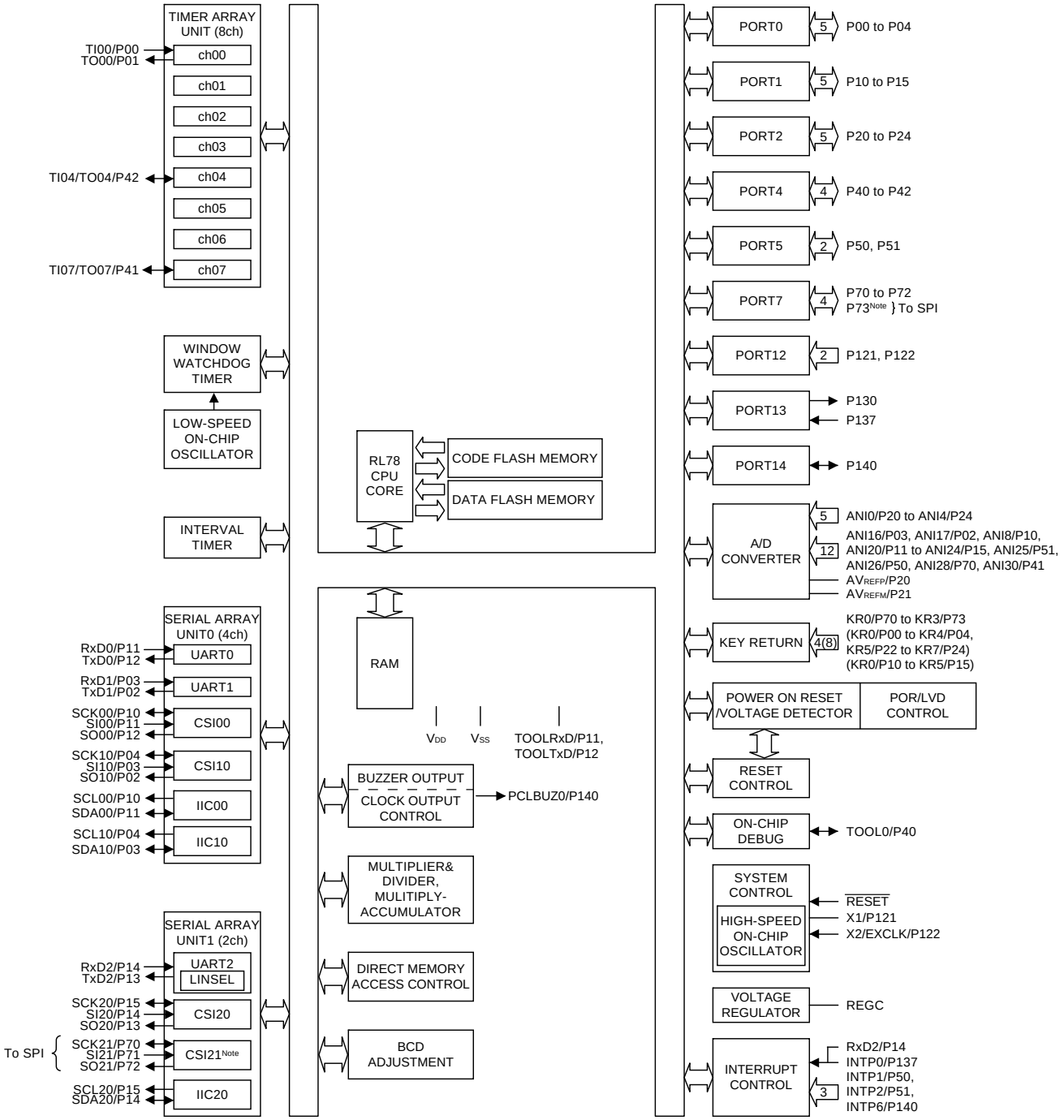
<R> 1. 5 Block Diagram

1. 5. 1 64-pin products



Remark The RL78/G1E (64-pin products) is a multi-chip package (MCP) device that integrates a chip of an analog block and a chip of 16-bit microcontroller block in a single package.

<R> **(1) Block diagram in microcontroller block (80-pin products)**



Note Connected inside the package.

(2) 80-pin products

Table 3-2. List of Differences in Special Function Registers (SFRs) (1/4)

Address	RL78/G1E (80-pin products)			RL78/G1A (64-pin products)		
	SFRs Name	Symbol		SFRs Name	Symbol	
FFF00H	Port register 0 Note	P0		Port register 0	P0	
FFF01H	Port register 1 Note	P1		Port register 1	P1	
FFF02H	Port register 2 Note	P2		Port register 2	P2	
FFF03H				Port register 3	P3	
FFF04H	Port register 4 Note	P4		Port register 4	P4	
FFF05H	Same as RL78/G1A (64-pin products)	P5		Port register 5	P5	
FFF06H				Port register 6	P6	
FFF07H	Port register 7 Note	P7		Port register 7	P7	
FFF0CH	Port register 12 Note	P12		Port register 12	P12	
FFF0DH	Same as RL78/G1A (64-pin products)	P13		Port register 13	P13	
FFF0EH	Port register 14 Note	P14		Port register 14	P14	
FFF0FH				Port register 15	P15	
FFF10H	Same as RL78/G1A (64-pin products)	TXD0/ SIO00	SDR00	Serial data register 00	TXD0/ SIO00	SDR00
FFF11H		—			—	
FFF12H	Same as RL78/G1A (64-pin products)	RXD0/ SIO01	SDR01	Serial data register 01	RXD0/ SIO01	SDR01
FFF13H		—			—	
FFF18H	Same as RL78/G1A (64-pin products)	TDR00		Timer data register 00	TDR00	
FFF19H						
FFF1AH	Same as RL78/G1A (64-pin products)	TDR01L	TDR01	Timer data register 01	TDR01L	TDR01
FFF1BH		TDR01H			TDR01H	
FFF1EH	Same as RL78/G1A (64-pin products)	ADCR		12-bit A/D conversion result register	ADCR	
FFF1FH	Same as RL78/G1A (64-pin)	ADCRH		8-bit A/D conversion result register	ADCRH	
FFF20H	Port mode register 0 Note	PM0		Port mode register 0	PM0	
FFF21H	Port mode register 1 Note	PM1		Port mode register 1	PM1	
FFF22H	Port mode register 2 Note	PM2		Port mode register 2	PM2	
FFF23H				Port mode register 3	PM3	
FFF24H	Port mode register 4 Note	PM4		Port mode register 4	PM4	
FFF25H	Same as RL78/G1A (64-pin products)	PM5		Port mode register 5	PM5	
FFF26H	Port mode register 6 Note	PM6		Port mode register 6	PM6	
FFF27H	Port mode register 7 Note	PM7		Port mode register 7	PM7	
FFF2CH				Port mode register 12	PM12	
FFF2EH	Port mode register 14 Note	PM14		Port mode register 14	PM14	
FFF2FH	Port mode register 15 Note	PM15		Port mode register 15	PM15	
FFF30H	Same as RL78/G1A (64-pin products)	ADM0		A/D converter mode register 0	ADM0	
FFF31H	Analog input channel specification register Note	ADS		Analog input channel specification register	ADS	
FFF32H	A/D converter mode register 1 Note	ADM1		A/D converter mode register 1	ADM1	

Note The bit setting is different from that of RL78/G1A (64-pin products).

Caution Do not write data to the registers which is in the row with painted gray.

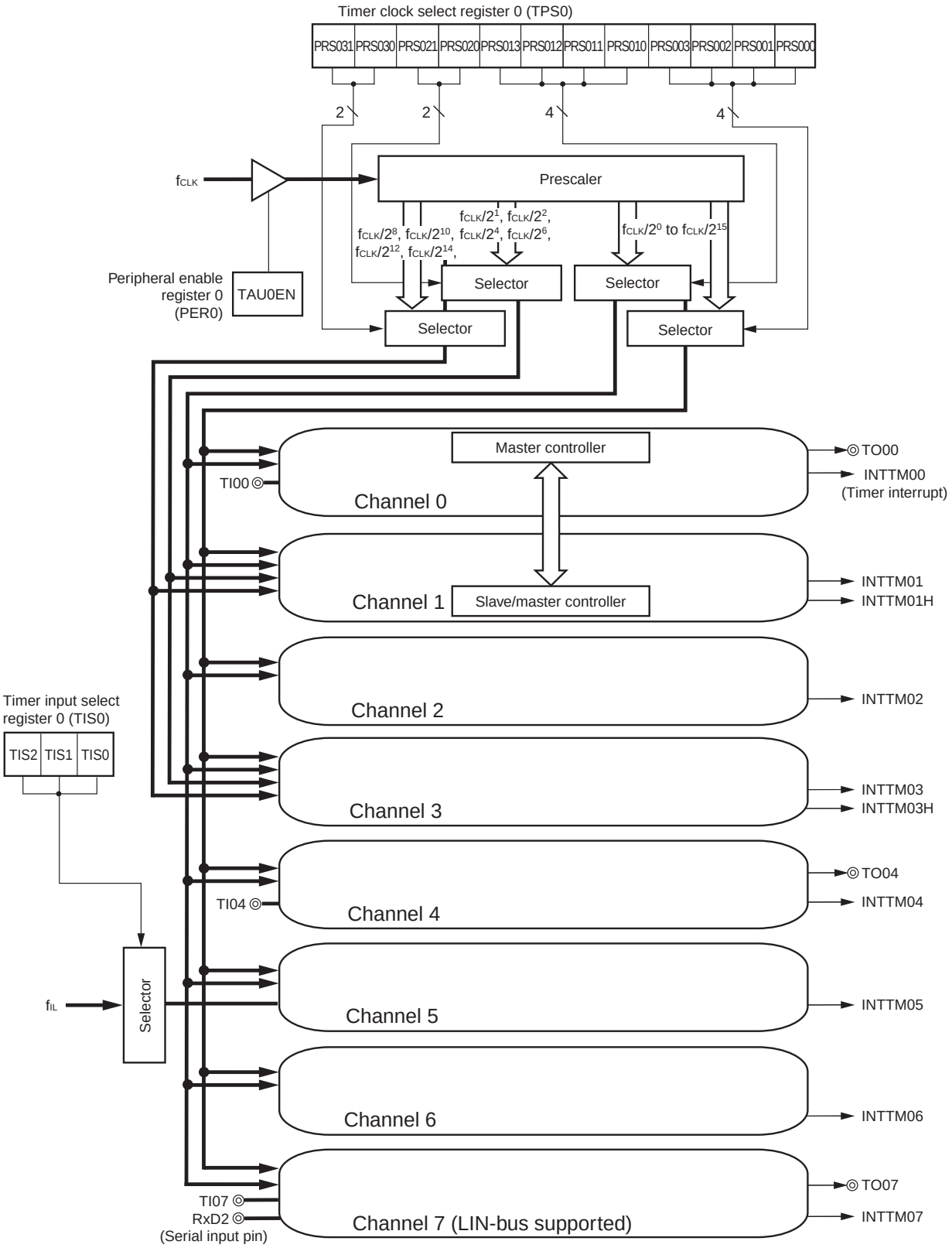
3. 5. 2 Configuration of clock generator

The clock generator includes the following hardware.

Table 3-6. Configuration of Clock Generator

Item	Configuration
Control registers	Clock operation mode control register (CMC) System clock control register (CKC) Clock operation status control register (CSC) Oscillation stabilization time counter status register (OSTC) Oscillation stabilization time select register (OSTS) Peripheral enable register 0 (PER0) <R> Subsystem clock supply mode control register (OSMC) High-speed on-chip oscillator frequency select register (HOCODIV) High-speed on-chip oscillator trimming register (HIOTRM)
Oscillators	X1 oscillator High-speed on-chip oscillator Low-speed on-chip oscillator

Figure 3-3. Entire Configuration of Timer Array Unit 0 (Example: 80-pin products)



Remark f_{IL}: ow-speed on-chip oscillator clock frequency

<R> 3. 12. 3. 17 Registers controlling port functions of serial input/output pins

Using the serial array unit requires setting of the registers that control the port functions multiplexed on the target channel (port mode register (PMxx), port register (Pxx), port input mode register (PIMxx), port output mode register (POMxx), port mode control register (PMCxx)).

For details, see **3. 4. 3. 1 Port mode registers (PMxx)**, **3. 4. 3. 2 Port registers (Pxx)**, **3. 4. 3. 4 Port input mode registers (PIMxx)**, **3. 4. 3. 5 Port output mode registers (POMxx)**, and **3. 4. 3. 6 Port mode control registers (PMCxx)**.

For details of setting example, see **12. 3. 17 Registers controlling port functions of serial Input/output pins** in **RL78/G1A Hardware User's Manual (R01UH0305E)**.

Table 3-14. Flags Corresponding to Interrupt Request Sources (3/4)

Interrupt Source	Interrupt Request Flag	Register	Interrupt Mask Flag	Register	Priority Specification Flag	Register	RL78/G1E 64-pin	RL78/G1E 80-pin
INTST1[Note 1]	STIF1[Note 1]	IF1L	STMK1[Note 1]	MK1L	STPR01, STPR11[Note 1]	PR01L, PR11L	√	√
INTCSI10[Note 1]	CSIIF10[Note 1]		CSIMK10[Note 1]		CSIPR010, CSIPR110[Note 1]		–	√
INTIIC10[Note 1]	IICIF10[Note 1]		IICMK10[Note 1]		IICPR010, IICPR110[Note 1]		–	√
INTSR1[Note 2]	SRIF1[Note 2]		SRMK1[Note 2]		SRPR01, SRPR11[Note 2]		√	√
INTCSI11[Note 2]	CSIIF11[Note 2]		CSIMK11[Note 2]		CSIPR011, CSIPR111[Note 2]		–	–
INTIIC11[Note 2]	IICIF11[Note 2]		IICMK11[Note 2]		IICPR011, IICPR111[Note 2]		–	–
INTSRE1[Note 3]	SREIF1[Note 3]		SREMK1[Note 3]		SREPR01, SREPR11[Note 3]		√	√
INTTM03H[Note 3]	TMIF03H[Note 3]		TMMK03H[Note 3]		TMPR003H, TMPR103H[Note 3]		√	√
INTIICA0	IICAIF0		IICAMK0		IICAPR00, IICAPR10		–	–
INTTM00	TMIF00		TMMK00		TMPR000, TMPR100		√	√
INTTM01	TMIF01		TMMK01		TMPR001, TMPR101		√	√
INTTM02	TMIF02		TMMK02		TMPR002, TMPR102		√	√
INTTM03	TMIF03		TMMK03		TMPR003, TMPR103		√	√
INTAD	ADIF	IF1H	ADMK	MK1H	ADPR0, ADPR1	PR01H, PR11H	√	√
INTRTC	RTCIF		RTCMK		RTCPR0, RTCPR1		–	–
INTIT	ITIF		ITMK		ITPR0, ITPR1		√	√
INTKR	KRIF		KRMK		KRPR0, KRPR1		√	√
INTTM04	TMIF04		TMMK04		TMPR004, TMPR104		√	√

(**Notes** are on the next page.)

3. 16. 3. 2 Interrupt mask flag register (MK0L, MK0H, MK1L, MK1H, MK2L, MK2H)

- 64-pin products

Address: FFFE4H After reset: FFH R/W

Symbol	7	6	5	4	3	<2>	<1>	<0>
MK0L	1	1	1	1	1	PMK0	LVIMK	WDTIMK

Address: FFFE5H After reset: FFH R/W

Symbol	<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>
MK0H	TMMK01H SREMK0	SRMK0	STMK0 CSIMK00 IICMK00	DMAMK1	DMAMK0	SREMK2	SRMK2 CSIMK21	STMK2

Address: FFFE6H After reset: FFH R/W

Symbol	<7>	<6>	<5>	<4>	3	<2>	<1>	<0>
MK1L	TMMK03	TMMK02	TMMK01	TMMK00	1	SREMK1 TMMK03H	SRMK1	STMK1

Address: FFFE7H After reset: FFH R/W

Symbol	<7>	6	5	4	<3>	<2>	1	<0>
MK1H	TMMK04	1	1	1	KRMK	ITMK	1	ADMK

Address: FFFD4H After reset: FFH R/W

Symbol	7	6	5	4	3	<2>	<1>	<0>
MK2L	1	1	1	1	1	TMMK07	TMMK06	TMMK05

Address: FFFD5H After reset: FFH R/W

Symbol	<7>	6	<5>	4	3	2	1	0
MK2H	FLMK	1	MDMK	1	1	1	1	1

Cautions 1. Be sure to set bits 3 to 7 of the MK0L register to “1”.

2. Be sure to set bit 3 of the MK1L register to “1”.

3. Be sure to set bits 1 and 4 to 6 of the MK1H register to “1”.

4. Be sure to set bits 3 to 7 of the MK2L register to “1”.

5. Be sure to set bits 0 to 4 and 6 of the MK2H register to “1”.

3. 17. 2 Configuration of key interrupt

The key interrupt includes the following hardware.

Table 3-17. Configuration of Key Interrupt

Item	Configuration
Control register	Key interrupt control register (KRCTL)
	Key interrupt mode control register 0 (KRM0)
	Key interrupt flag register (KRF)
	Port mode registers 0, 1, 2, 7 (PM0, PM1, PM2, PM7)
	Peripheral I/O redirection register (PIOR)

Format of User Option Byte (000C1H/010C1H) (1/2)

Address: 000C1H/010C1H[Note]

7	6	5	4	3	2	1	0
VPOC2	VPOC1	VPOC0	1	LVIS1	LVIS0	LVIMDS1	LVIMDS0

- LVD setting (interrupt & reset mode)

<R>

Detection voltage			Option byte setting value						
V_{LVDH}		V_{LVDL}	VPOC2	VPOC1	VPOC0	LVIS1	LVIS0	Mode setting	
Rising edge	Falling edge	Falling edge						LVIMDS1	LVIMDS0
3.13	3.06	1.84	0	0	1	0	0	1	0
3.75	3.67	2.45	0	1	0	0	0		
4.06	3.98	2.75	0	1	1	0	0		
–			Value other than above is setting prohibited.						

- LVD setting (reset mode)

<R>

Detection voltage		Option byte setting value						
V_{LVDH}		VPOC2	VPOC1	VPOC0	LVIS1	LVIS0	Mode setting	
Rising edge	Falling edge						LVIMDS1	LVIMDS0
3.13	3.06	0	0	1	0	0	1	1
3.75	3.67	0	1	0	0	0		
4.06	3.98	0	1	1	0	0		
–		Value other than above is setting prohibited.						

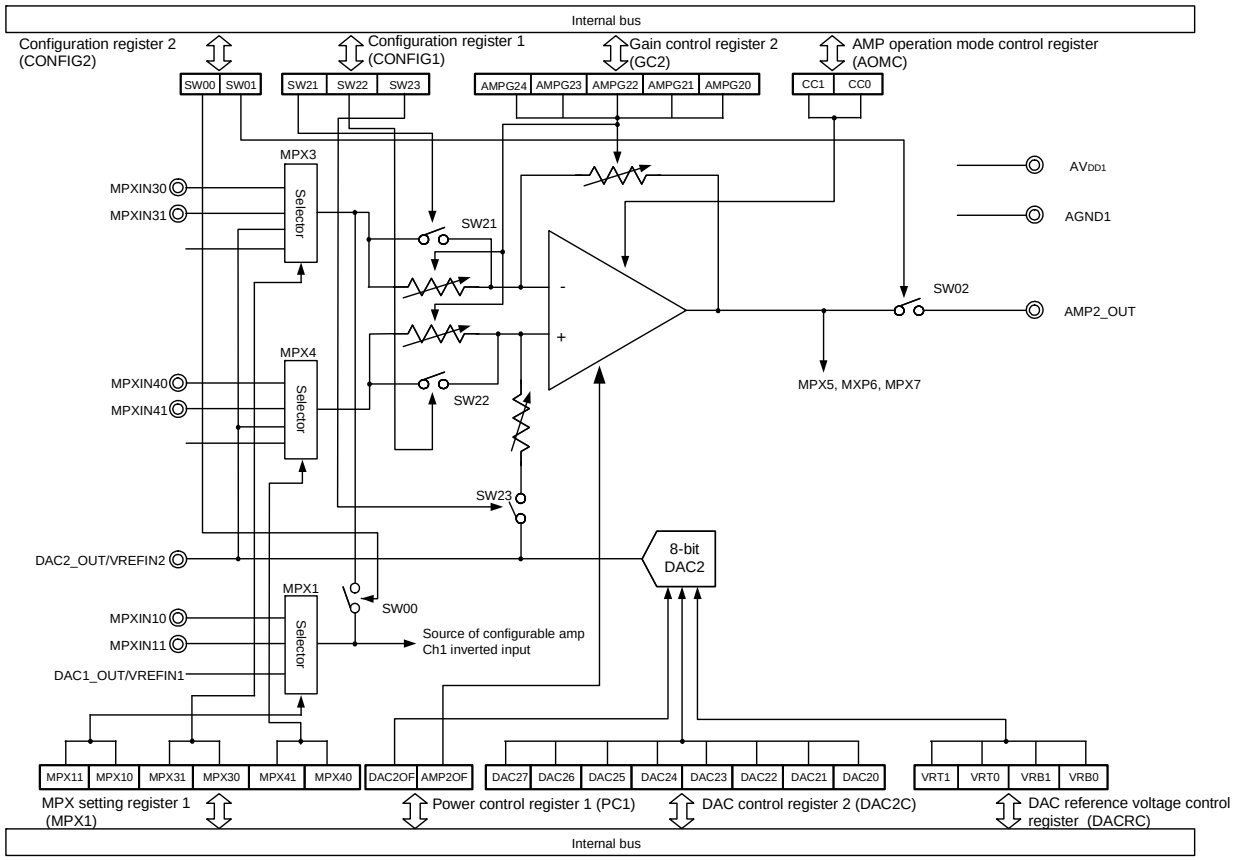
Note Set the same value as 000C1H to 010C1H when the boot swap operation is used because 000C1H is replaced by 010C1H.

<R> **Remarks 1.** For details on the LVD circuit, see **3. 21 Voltage Detector**.

2. The detection voltage is a TYP. value. For details, see **5. 2. 5. 4 LVD circuit characteristics.**

(**Cautions** are listed on the next page.)

Figure 4-2. Block Diagram of Configurable Amplifier Ch2



(7) Gain control register 3 (GC3)

This register is used to specify the gain and feedback resistance of configurable amplifier Ch3.

The value to specify depends on the configuration of configurable amplifier Ch3.

When using configurable amplifiers Ch1 to Ch3 together as an instrumentation amplifier, be sure to set gain control register 1 (GC1) and gain control register 2 (GC2) to 03H, respectively.

Reset signal input clears this register to 00H.

Address: 08H After reset: 00H R/W

	7	6	5	4	3	2	1	0
GC3	0	0	0	AMPG34	AMPG33	AMPG32	AMPG31	AMPG30

Table 4-7. Gain of Configurable Amplifier Ch3 (Non-Inverting Amplifier)

AMPG34	AMPG33	AMPG32	AMPG31	AMPG30	Gain of Configurable Amplifier Ch3 (Typ.)
0	0	0	0	0	9.5 dB
0	0	0	0	1	10.9 dB
0	0	0	1	0	12.4 dB
0	0	0	1	1	14.0 dB
0	0	1	0	0	15.6 dB
0	0	1	0	1	17.3 dB
0	0	1	1	0	19.0 dB
0	0	1	1	1	20.8 dB
0	1	0	0	0	22.7 dB
0	1	0	0	1	24.5 dB
0	1	0	1	0	26.4 dB
0	1	0	1	1	28.3 dB
0	1	1	0	0	30.3 dB
0	1	1	0	1	32.2 dB
0	1	1	1	0	34.2 dB
0	1	1	1	1	36.1 dB
1	0	0	0	0	38.1 dB
1	0	0	0	1	40.1 dB
Other than above					Setting prohibited

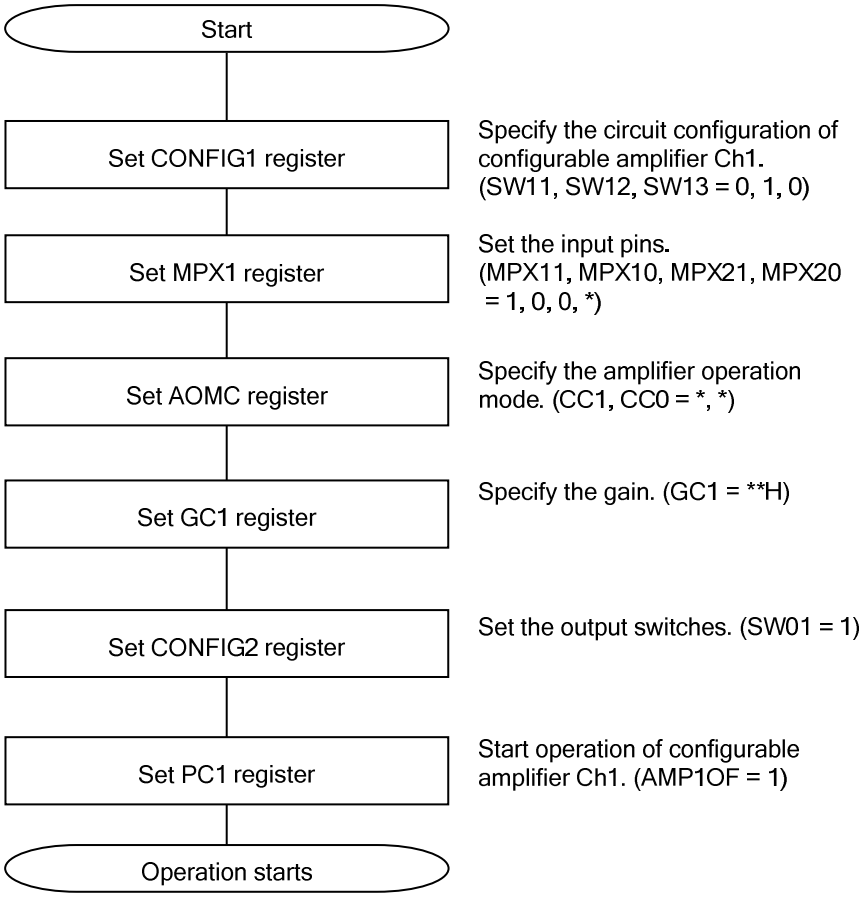
<R> **Remark** Bits 7 to 5 are fixed at 0 of read only.

4. 1. 4 Procedure for operating the configurable amplifiers

(1) Procedure when using the amplifiers as non-inverting amplifiers

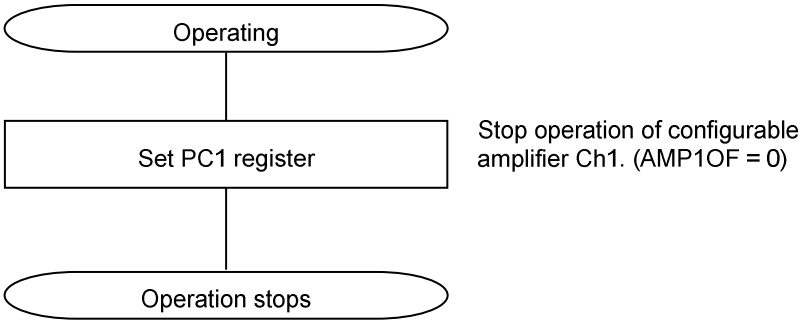
When using the configurable amplifiers as non-inverting amplifiers, follow the procedures below to start and stop the amplifiers.

Example of procedure for starting configurable amplifier Ch1 (non-inverting amplifier)

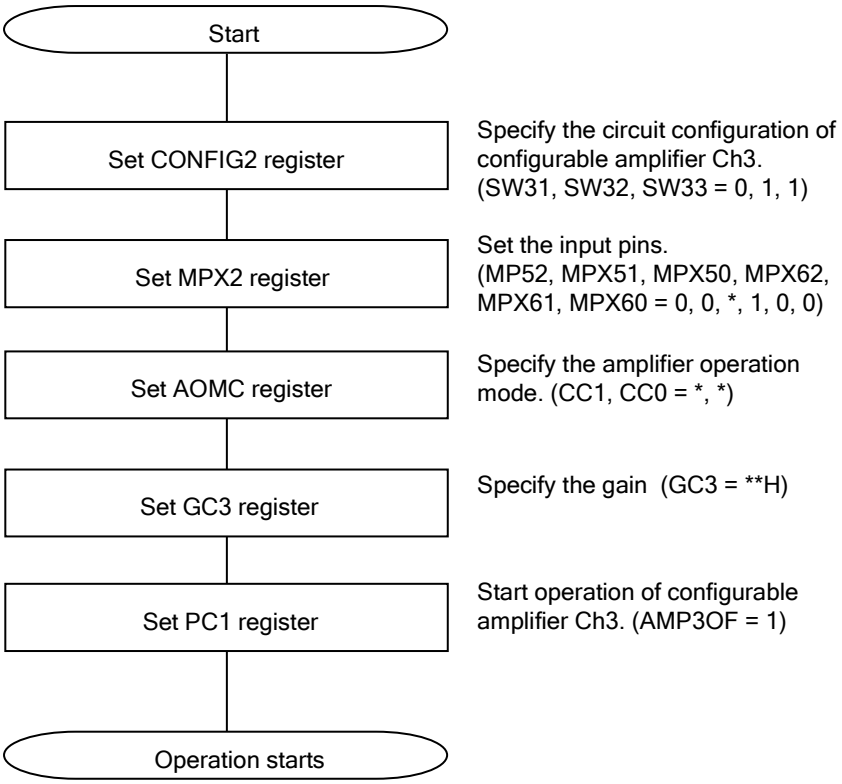


Remark *: don't care

Example of procedure for stopping configurable amplifier Ch1 (non-inverting amplifier)

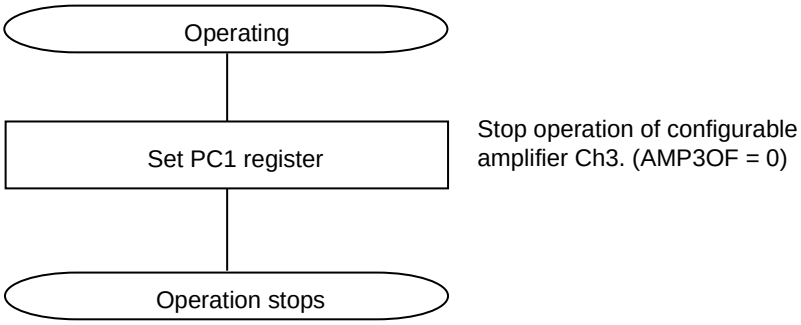


Example of procedure for starting configurable amplifier Ch3 (inverting amplifier)

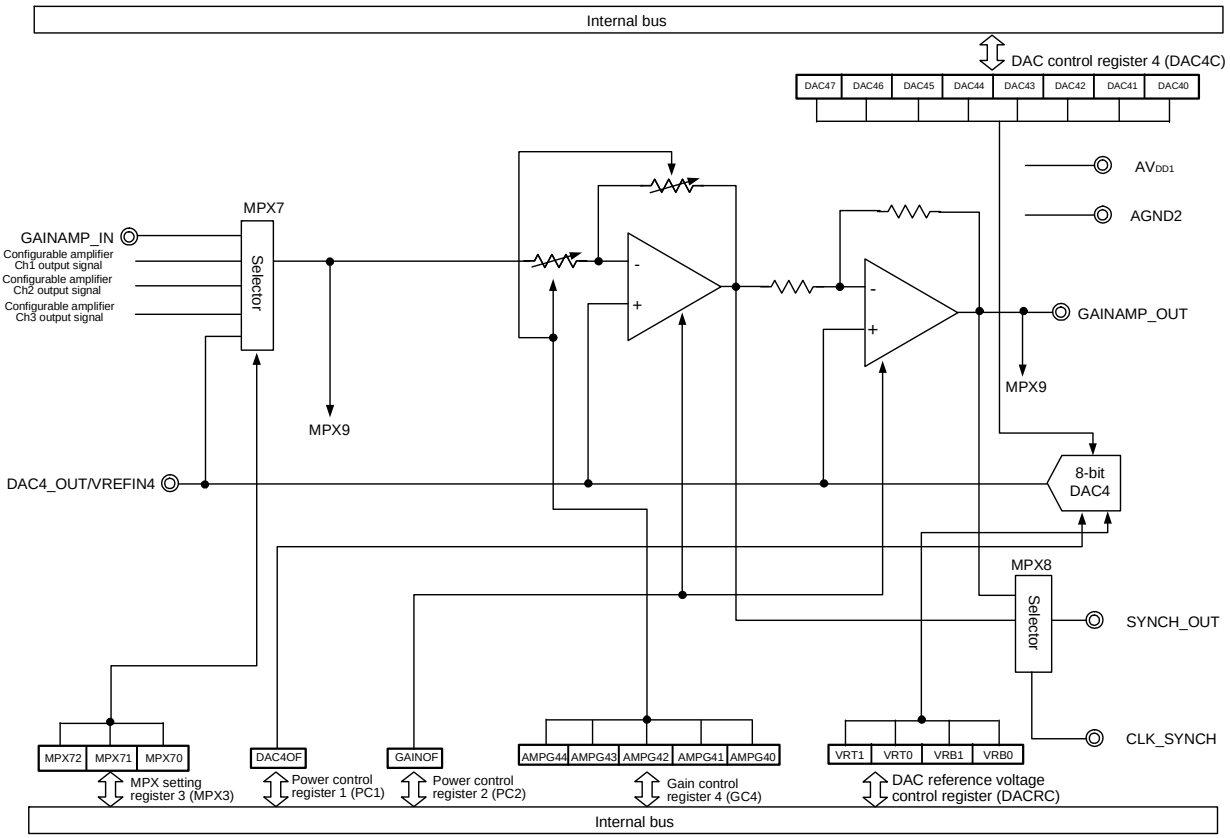


Remark *: don't care

Example of procedure for stopping configurable amplifier Ch3 (inverting amplifier)



- **80-pin products**



4. 2. 3 Registers controlling the gain adjustment amplifier

The gain adjustment amplifier is controlled by the following 3 registers:

- MPX setting register 3 (MPX3)
- Gain control register 4 (GC4)
- Power control register 2 (PC2)

(1) MPX setting register 3 (MPX3)

This register is used to control MPX7, MPX9, MPX10, and MPX11.

When selecting the signal to be input to the gain adjustment amplifier, use bits 2 to 0.

Reset signal input clears this register to 00H.

- **64-pin products**

Address: 05H After reset: 00H R/W

	7	6	5	4	3	2	1	0
MPX3	0	0	SCF2	SCF1	0	MPX72	MPX71	MPX70

MPX72	MPX71	MPX70	Source of gain adjustment amplifier input
0	0	0	–
0	0	1	Configurable amplifier Ch1 output signal
0	1	0	Configurable amplifier Ch2 output signal
0	1	1	Configurable amplifier Ch3 output signal
1	0	0	D/A converter Ch4 output signal or VREFIN4 pin
Other than above			Setting prohibited

Caution Be sure to clear bit 3 to "0".

<R> **Remark** Bits 7 and 6 are fixed at 0 of read only.

- **80-pin products**

Address: 05H After reset: 00H R/W

	7	6	5	4	3	2	1	0
MPX3	0	0	SCF2	SCF1	SCF0	MPX72	MPX71	MPX70

MPX72	MPX71	MPX70	Source of gain adjustment amplifier input
0	0	0	GAINAMP_IN pin
0	0	1	Configurable amplifier Ch1 output signal
0	1	0	Configurable amplifier Ch2 output signal
0	1	1	Configurable amplifier Ch3 output signal
1	0	0	D/A converter Ch4 output signal or VREFIN4 pin
Other than above			Setting prohibited

<R> **Remark** Bits 7 and 6 are fixed at 0 of read only.

4. 5 High-Pass Filter

The RL78/G1E (80-pin products) has one on-chip switched-capacitor high-pass filter channel [Note].

Note The high-pass filter is not provided in the RL78/G1E (64-pin products).

4. 5. 1 Overview of high-pass filter features

The features of high-pass filter are described below.

- Butterworth characteristics (Q value = 0.702)
- Cutoff frequency (f_C) range: 8 Hz to 800 Hz
- External input clock frequency (f_{CLK_HPF}) range: $f_C \times 2 / 0.008$ = 2 kHz to 200 kHz
<R> - Includes a power-off function.

And also, the DAC4_OUT output signals can be used as the reference voltage for high-pass filter.

If D/A converter is powered off, the external reference voltage is to be input to DAC4_OUT/VREFIN4 pin.

For details about use of D/A converter, see **4. 3 D/A Converter**.

Remarks 1. The internal control clock (f_S) of the high-pass filter has a duty of 50%, so the external input clock is divided by two at the internal D flip-flop before being used for the low-pass filter. If the internal control clock frequency (f_S) is 100 kHz, therefore, input a 200 kHz clock signal to the CLK_HPF pin.

2. The phase of the signal input to the high-pass filter inverts after passing the high-pass filter.

5. 2. 5. 2 Temperature sensor, internal reference voltage output characteristics

(T_A = –40 to +85°C, 2.4 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V, HS (high-speed main) mode)

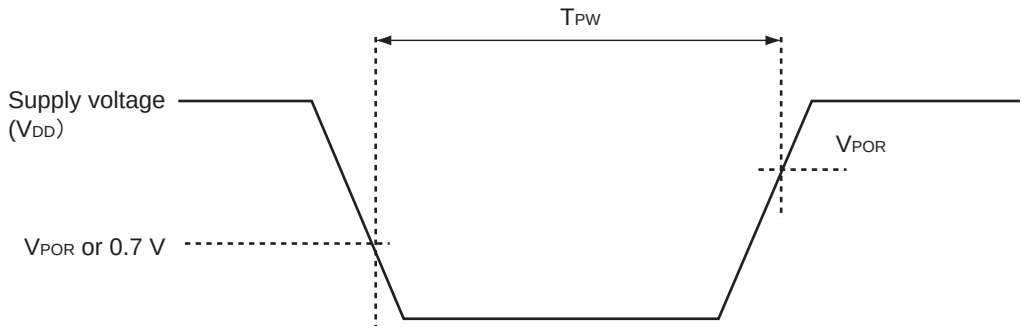
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Temperature sensor output voltage	V_{TMPS25}	ADS register = 80H, T_A = +25°C		1.05		V
Internal reference voltage	V_{BGR}	ADS register = 81H	1.38	1.45	1.5	V
Temperature coefficient	F_{VTMPS}	Temperature sensor output voltage that depends on the temperature		–3.6		mV/°C
Operation stabilization wait time	t_{AMP}		10			μs

5. 2. 5. 3 POR circuit characteristics

(T_A = –40 to +85°C, V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Detection voltage	V_{POR}	When power supply voltage is rising	1.47	1.51	1.55	V
	V_{PDR}	When power supply voltage is falling	1.46	1.50	1.54	V
Minimum pulse width[Note]	T_{PW}		300			μs

Note This is the time required for the POR circuit to execute a reset when V_{DD} falls below V_{PDR}. When the microcontroller enters STOP mode or if the main system clock (f_{MAIN}) has been stopped by setting bit 0 (HIOSTOP) and bit 7 (MSTOP) of the clock operation status control register (CSC), this is the time required for the POR circuit to execute a reset before V_{DD} rises to V_{POR} after having fallen below 0.7 V.



(-40°C ≤ T_A ≤ 85°C, AV_{DD1} = AV_{DD2} = AV_{DD3} = DV_{DD} = 5.0 V, VREFIN = VREFIN2 = VREFIN3 = 1.7 V,
AMP1OF = AMP2OF = AMP3OF = 1, DAC1OF = DAC2OF = DAC3OF = 0, differential amplifier) (2/2)

Parameter	Symbol	Conditions	Ratings			Unit
			MIN	TYP	MAX	
Input conversion offset voltage	VOFF00	CC1, CC0 = 0, 0, T_A = 25°C GCn = 07H (20 dB)	-7	–	7	mV
	VOFF01	CC1, CC0 = 0, 1, T_A = 25°C GCn = 07H (20 dB)	-10	–	10	mV
	VOFF10	CC1, CC0 = 1, 0, T_A = 25°C GCn = 07H (20 dB)	-10	–	10	mV
	VOFF11	CC1, CC0 = 1, 1, T_A = 25°C GCn = 07H (20 dB)	-12	–	12	mV
Input conversion offset voltage temperature coefficient	VOTC		–	±6	–	μV/°C
<R> Slew rate	SR00	CC1, CC0 = 0, 0, CL = 30 pF, GCn = 00H (6 dB)	–	0.68	–	V/μs
	SR01	CC1, CC0 = 0, 1, CL = 30 pF, GCn = 00H (6 dB)	–	0.35	–	V/μs
	SR10	CC1, CC0 = 1, 0 CL = 30 pF, GCn = 00H (6 dB)	–	0.25	–	V/μs
	SR11	CC1, CC0 = 1, 1, CL = 30 pF, GCn = 00H (6 dB)	–	0.09	–	V/μs
Common mode rejection ratio	CMRR00	CC1, CC0 = 0, 0, GCn = 11H (40 dB), f = 1 kHz	–	84	–	dB
	CMRR01	CC1, CC0 = 0, 1, GCn = 11H (40 dB) f = 1 kHz	–	82	–	dB
	CMRR10	CC1, CC0 = 1, 0, GCn = 11H (40 dB) f = 1 kHz	–	80	–	dB
	CMRR11	CC1, CC0 = 1, 1, GCn = 11H (40 dB) f = 1 kHz	–	76	–	dB
Power supply rejection ratio	PSRR00	CC1, CC0 = 0, 0, GCn = 00H (6 dB), f = 1 kHz	–	70	–	dB
	PSRR01	CC1, CC0 = 0, 1, GCn = 00H (6 dB) f = 1 kHz	–	68	–	dB
	PSRR10	CC1, CC0 = 1, 0, GCn = 00H (6 dB) f = 1 kHz	–	62	–	dB
	PSRR11	CC1, CC0 = 1, 1, GCn = 00H (6 dB) f = 1 kHz	–	50	–	dB
Gain setting error	GAIN_Accu1	T_A = 25°C	-0.6	–	0.6	dB
	GAIN_Accu2	T_A = –40 to 85°C	-1.0	–	1.0	dB

Remark n = 1 to 3

(4/6)

Edition	Description	Chapter
Rev.1.00	Modification of the description in **5. 2. 8 Timing specs for switching flash memory programming modes**	**CHAPTER 5 ELECTRICAL SPECIFICATIONS**
	Addition of the specification depending on the products in **5. 3. 3. 2 Gain adjustment amplifier characteristics**	
	Addition of the specification for “CLK_SYNCH input voltage” in **5. 3. 3. 2 Gain adjustment amplifier characteristics (2) 80-pin products**	
	Error correction of the description and addition of the specification for “CLK_SYNCH input voltage” in **5. 3. 3. 4 Low-pass filter characteristics**	
	Error correction of the description and addition of the specification for “CLK_SYNCH input voltage” in **5. 3. 3. 5 High-pass filter characteristics**	
Rev.0.04	Change of the name for CS from “Slave Select” to “Chip Select”	Whole pages
	Deletion of the word “interface” from the name of SPI	
	Error correction of the figures in **1. 4 Pin Configuration (Top View)**	**CHAPTER 1 OUTLINE**
	Error correction of the description (deletion of “SCLA0”, “SCLA1”) in **1. 4. 3 Pin identification (Microcontroller Block)**	
	Error correction of the figures in **1. 5 Block Diagram**	
	Error correction of the function names and modification of the description for the function in **2. 2 Pin Functions in Analog Block**	**CHAPTER 2 PIN FUNCTIONS**
	Error correction of the description for the pin of ANI30 (D/A converter -> A/D converter) in **2. 3. 4 P40 to P42 (port 4)**	
	Modification of the description in **2. 3. 43 I.C**	
	Addition of “Remarks” on the tables in **3. 1 Differences in Functions between RL78/G1E and RL78/G1A**	**CHAPTER 3 MICROCONTROLLER FUNCTION**
	Modification of the description on the tables (deletion of the same registers as RL78/G1A) in **3. 2 Differences in (Expanded) Special-Function Registers between RL78/G1E and RL78/G1A**	
	Modification of the description and change of the sequence flow of the setting procedure (2) in **3. 3. 3 Connecting to an external device with different potential (1.8 V, 2.5 V, 3 V)**	
	Addition of **3. 4. 4 Resonator and Oscillator Constants**	
	Error correction of the description on **Table 3-14.**	
	Addition of **3. 13 Safety Functions**	
	Modification of the gain setting of non-inverting amplifier in **5. 1 Overview of Configurable Amplifier Features** and in **5. 3 Registers Controlling the Configurable Amplifiers**	**CHAPTER 5 CONFIGURABLE AMPLIFIERS**
	Modification of the description in **8. 1 Overview of Low-Pass Filter Features**	**CHAPTER 8 LOW-PASS FILTER**
	Modification of the description in **9. 1 Overview of High-Pass Filter Features**	**CHAPTER 8 HIGH-PASS FILTER**
	Addition of **Note** in **11. 3 Registers Controlling the Variable Output Voltage Regulator**	**CHAPTER 11 VARIABLE OUTPUT VOLTAGE REGULATOR**