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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	RL78
Core Size	16-Bit
Speed	32MHz
Connectivity	CSI, I²C, LINbus, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	26
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	1.6V ~ 5.5V
Data Converters	A/D 17x8/12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	80-LQFP
Supplier Device Package	80-LFQFP (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f10fmeafb-x0

NOTES FOR CMOS DEVICES

(1) VOLTAGE APPLICATION WAVEFORM AT INPUT PIN: Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between VIL (MAX) and VIH (MIN) due to noise, etc., the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between VIL (MAX) and VIH (MIN).

(2) HANDLING OF UNUSED INPUT PINS: Unconnected CMOS device inputs can be cause of malfunction. If an input pin is unconnected, it is possible that an internal input level may be generated due to noise, etc., causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using pull-up or pull-down circuitry. Each unused pin should be connected to VDD or GND via a resistor if there is a possibility that it will be an output pin. All handling related to unused pins must be judged separately for each device and according to related specifications governing the device.

(3) PRECAUTION AGAINST ESD: A strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it when it has occurred. Environmental control must be adequate. When it is dry, a humidifier should be used. It is recommended to avoid using insulators that easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors should be grounded. The operator should be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with mounted semiconductor devices.

(4) STATUS BEFORE INITIALIZATION: Power-on does not necessarily define the initial status of a MOS device. Immediately after the power source is turned ON, devices with reset functions have not yet been initialized. Hence, power-on does not guarantee output pin levels, I/O settings or contents of registers. A device is not initialized until the reset signal is received. A reset operation must be executed immediately after power-on for devices with reset functions.

(5) POWER ON/OFF SEQUENCE: In the case of a device that uses different power supplies for the internal operation and external interface, as a rule, switch on the external power supply after switching on the internal power supply. When switching the power supply off, as a rule, switch off the external power supply and then the internal power supply. Use of the reverse power on/off sequences may result in the application of an overvoltage to the internal elements of the device, causing malfunction and degradation of internal elements due to the passage of an abnormal current. The correct power on/off sequence must be judged separately for each device and according to related specifications governing the device.

(6) INPUT OF SIGNAL DURING POWER OFF STATE : Do not input signals or an I/O pull-up power supply while the device is not powered. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Input of signals during the power off state must be judged separately for each device and according to related specifications governing the device.

2. 2 Pin Functions in Analog Block

<R> About I/O circuit type, see **2. 4 Block Diagrams of Pins**.

<R> 2. 2. 1 64-pin products

Function Name	I/O Circuit Type	I/O	Function
AV_{DD3}	–	–	Power supply pin for filter
AGND2	–	–	GND pin for gain adjustment amplifier
MPXIN60	ANALOG6	Input	Multiplexer 6 input pin 0 (Configurable amplifier Ch3 input pin 0 (+))
MPXIN50	ANALOG6		Multiplexer 5 input pin 0 (Configurable amplifier Ch3 input pin 0 (-))
AMP3_OUT	ANALOG10	Output	Configurable amplifier Ch3 output pin
DAC3_OUT/ VREFIN3	ANALOG2	I/O	D/A converter Ch3 output pin/configurable amplifier Ch3 reference voltage input pin
AMP2_OUT	ANALOG11	Output	Configurable amplifier Ch2 output pin
AGND1	–	–	GND pin for configurable amplifiers Ch1 to Ch3.
AMP1_OUT	ANALOG11	Output	Configurable amplifier Ch1 output pin
AV_{DD1}	–	–	Power supply pin for configurable amplifiers Ch1 to Ch3
DAC2_OUT/ VREFIN2	ANALOG2	I/O	D/A converter Ch2 output pin/configurable amplifier Ch2 reference voltage input pin
DAC1_OUT/ VREFIN1	ANALOG2		D/A converter Ch1 output pin/configurable amplifier Ch1 reference voltage input pin
MPXIN41	ANALOG6	Input	Multiplexer 4 input pin 1 (Configurable amplifier Ch2 input pin 1 (+))
MPXIN31	ANALOG6		Multiplexer 3 input pin 1 (Configurable amplifier Ch2 input pin 1 (-))
MPXIN40	ANALOG6		Multiplexer 4 input pin 0 (Configurable amplifier Ch2 input pin 0 (+))
MPXIN30	ANALOG6		Multiplexer 3 input pin 0 (Configurable amplifier Ch2 input pin 0 (-))
MPXIN21	ANALOG6		Multiplexer 2 input pin 1 (Configurable amplifier Ch1 input pin 1 (+))
MPXIN11	ANALOG6		Multiplexer 1 input pin 1 (Configurable amplifier Ch1 input pin 1 (-))
MPXIN20	ANALOG6		Multiplexer 2 input pin 0 (Configurable amplifier Ch1 input pin 0 (+))
MPXIN10	ANALOG6		Multiplexer 1 input pin 0 (Configurable amplifier Ch1 input pin 0 (-))
AGND3	–	–	GND pin for variable output voltage regulator and reference voltage generator
BGR_OUT	ANALOG9	Output	Reference voltage generator output pin
AV_{DD2}	–	–	Power supply pin for variable output voltage regulator and reference voltage generator
LDO_OUT	ANALOG3	Output	Variable output voltage regulator output pin
TEMP_OUT	ANALOG4	Output	Temperature sensor output pin
$\overline{ARESET}$	ANALOG5	Input	External reset signal input for the functions of analog block
DV_{DD}	–	–	Power supply pin for SPI
$\overline{SCLK}$	ANALOG8	Input	Serial clock input pin for SPI
SDO	ANALOG12	Output	Serial data output pin for SPI
SDI	ANALOG8	Input	Serial data input pin for SPI
$\overline{CS}$	ANALOG8	Input	Chip select input pin for SPI
DGND	–	–	GND pin for SPI
DAC4_OUT/ VREFIN4	ANALOG13	I/O	D/A converter Ch4 output pin/gain adjustment amplifier, filter reference voltage input pin
CLK_LPF	ANALOG7	Input	Pin for inputting low-pass filter control clock
AGND4	–	–	GND pin for filter
LPF_OUT	ANALOG1	Output	Low-pass filter output pin

Table 3-1. List of Differences in Special Function Registers (SFRs) (2/4)

Address	RL78/G1E (64-pin products)			RL78/G1A (64-pin products)		
	SFRs Name	Symbol		SFRs Name	Symbol	
FFF34H	Same as RL78/G1A (64-pin products)	KRCTL		Key return control register	KRCTL	
FFF35H	Same as RL78/G1A (64-pin products)	KRF		Key return flag register	KRF	
FFF36H				Key return mode control register 1	KRM1	
FFF37H	Key return mode control register 0 Note	KRM0		Key return mode control register 0	KRM0	
FFF38H	External interrupt rising edge enable register 0 Note	EGP0		External interrupt rising edge enable register 0	EGP0	
FFF39H	External interrupt falling edge enable register 0 Note	EGN0		External interrupt falling edge enable register 0	EGN0	
FFF3AH				External interrupt rising edge enable register 1	EGP1	
FFF3BH				External interrupt falling edge enable register 1	EGN1	
FFF44H	Same as RL78/G1A (64-pin products)	TXD1/SIO10	SDR02	Serial data register 02	TXD1/SIO10	SDR02
FFF45H		—			—	
FFF46H	Same as RL78/G1A (64-pin products)	RXD1/SIO11	SDR03	Serial data register 03	RXD1/SIO11	SDR03
FFF47H		—			—	
FFF48H	Same as RL78/G1A (64-pin products)	TXD2/SIO20	SDR10	Serial data register 10	TXD2/SIO20	SDR10
FFF49H		—			—	
FFF4AH	Same as RL78/G1A (64-pin products)	RXD2/SIO21	SDR11	Serial data register 11	RXD2/SIO21	SDR11
FFF4BH		—			—	
FFF50H				IICA shift register 0	IICA0	
FFF51H				IICA status register 0	IICS0	
FFF52H				IICA flag register 0	IICF0	
FFF64H	Same as RL78/G1A (64-pin products)	TDR02		Timer data register 02	TDR02	
FFF65H						
FFF66H	Same as RL78/G1A (64-pin products)	TDR03L	TDR03	Timer data register 03	TDR03L	TDR03
FFF67H		TDR03H			TDR03H	
FFF68H	Same as RL78/G1A (64-pin products)	TDR04		Timer data register 04	TDR04	
FFF69H						
FFF6AH	Same as RL78/G1A (64-pin products)	TDR05		Timer data register 05	TDR05	
FFF6BH						
FFF6CH	Same as RL78/G1A (64-pin products)	TDR06		Timer data register 06	TDR06	
FFF6DH						
FFF6EH	Same as RL78/G1A (64-pin products)	TDR07		Timer data register 07	TDR07	
FFF6FH						

Note The bit setting is different from that of RL78/G1A (64-pin products).

Caution Do not write data to the registers which is in the row with painted gray.

3. 4 Port Functions

In this section, the differences of the functions and registers from RL78/G1A (64-pin products) are described. For details, see **CHAPTER 4 PORT FUNCTIONS** in **RL78/G1A Hardware User's Manual (R01UH0305E)**.

3. 4. 1 Port functions

The RL78/G1E microcontrollers (64-pin products, 80-pin products) are provided with digital I/O ports, which enable variety of control operations. In addition to the function as digital I/O ports, these ports have several alternate functions. For details of the alternate functions, see **CHAPTER 2 PIN FUNCTIONS**.

3. 4. 2 Port configuration

Ports include the following hardware.

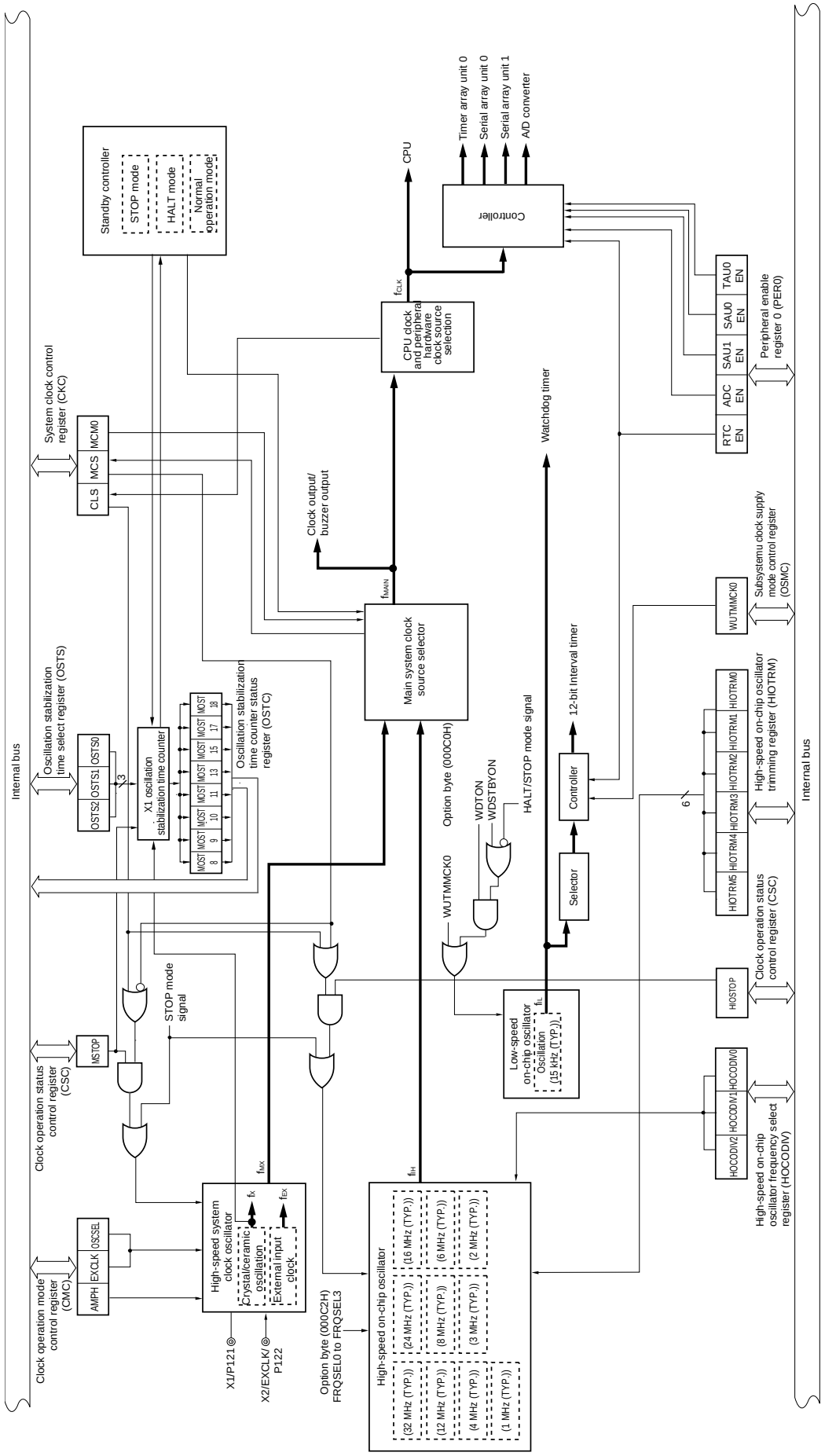
Table 3-5. Port Configuration

Item	Configuration
Control registers	Port mode registers (PM0 to PM2, PM4 to PM7, PM14, PM15) Port registers (P0 to P2, P4, P5, P7, P12 to P14) Pull-up resistor option registers (PU0, PU1, PU4, PU5, PU7, PU14) Port input mode registers (PIM0, PIM1) Port output mode registers (POM0, POM1, POM5) Port mode control registers (PMC0, PMC1, PMC3, PMC5, PMC7) A/D port configuration register (ADPC) Peripheral I/O redirection register (PIOR) Global analog input disable register (GAIDIS)
Port	· 64-pin products Total: 24 (CMOS I/O: 20, CMOS input: 3, CMOS output: 1) · 80-pin products Total: 30 (CMOS I/O: 26, CMOS input: 3, CMOS output: 1)
Pull-up resistor	· 64-pin products Total: 16 · 80-pin products Total: 21

For details of each port, also see **4. 2 Port Configuration** in **RL78/G1A Hardware User's Manual (R01UH0305E)**.

Figure 3-1. Block Diagram of Clock Generator

<R>



(**Remark** is listed on the next page)

3. 5. 3. 2 System clock control register (CKC)

Address: FFFA4H After reset: 00H R/W[Note]

Symbol	<7>	6	<5>	<4>	3	2	1	0
CKC	CLS	0	MCS	MCM0	0	0	0	0

CLS	Status of CPU/peripheral hardware clock (f_{CLK})
0	Main system clock (f_{MAIN})
1	–

MCS	Status of main system clock (f_{MAIN})
0	High-speed on-chip oscillator clock (f_{IH})
1	High-speed system clock (f_{MX})

MCM0	Main system clock (f_{MAIN}) operation control
0	Selects the high-speed on-chip oscillator clock (f_{IH}) as the main system clock (f_{MAIN})
1	Selects the high-speed system clock (f_{MX}) as the main system clock (f_{MAIN})

Note Bits 7 and 5 are read-only.

Caution Be sure to clear bits 0 to 3 and 6 to "0".

Remark f_{IH}: High-speed on-chip oscillator clock frequency
f_{MX}: High-speed system clock frequency
f_{MAIN}: Main system clock frequency

- Format of Timer Mode Register mn (TMRmn) (3/4)

Address: F0190H, F0191H (TMR00) - F019EH, F019FH (TMR07) After reset: 0000H R/W

Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TMRmn (n = 2, 4, 6)	CKS mn1	CKS mn0	0	CCS mn	MAS TER mn	STS mn2	STS mn1	STS mn0	CIS mn1	CIS mn0	0	0	MD mn3	MD mn2	MD mn1	MD mn0

Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TMRmn (n = 1, 3)	CKS mn1	CKS mn0	0	CCS mn	SPLIT mn	STS mn2	STS mn1	STS mn0	CIS mn1	CIS mn0	0	0	MD mn3	MD mn2	MD mn1	MD mn0

Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TMRmn (n = 0, 5, 7)	CKS mn1	CKS mn0	0	CCS mn	0[Note]	STS mn2	STS mn1	STS mn0	CIS mn1	CIS mn0	0	0	MD mn3	MD mn2	MD mn1	MD mn0

CISmn1	CISmn0	Selection of TImn pin input valid edge
0	0	Falling edge
0	1	Rising edge
1	0	Both edges (when low-level width is measured) Start trigger: Falling edge, Capture trigger: Rising edge
1	1	Both edges (when high-level width is measured) Start trigger: Rising edge, Capture trigger: Falling edge
If both the edges are specified when the value of the STSmn2 to STSmn0 bits is other than 010B, set the CISmn1 to CISmn0 bits to 10B.		

<R> **Note** Bit 11 is fixed at 0 of read only, write is ignored.

Remark m: Unit number (m = 0), n: Channel number (n = 0 to 7 (however, timer input pin (TImn), timer output pin (TOmn): n = 0, 4, 7))

3. 12. 1. 3 Simplified I²C (IIC00, IIC10, IIC20)

This is a clocked communication function to communicate with two or more devices by using two lines: serial clock (SCL) and serial data (SDA). This simplified I²C is designed for single communication with a device such as EEPROM, flash memory, or A/D converter, and therefore, it functions only as a master.

Make sure by using software, as well as operating the control registers, that the AC specifications of the start and stop conditions are observed.

For details about the settings, see **3. 12. 8 Operation of simplified I²C (IIC00, IIC10, IIC20)**.

[Data transmission/reception]

- Master transmission, master reception (only master function with a single master)
- ACK output function Note and ACK detection function
- Data length of 8 bits

(When an address is transmitted, the address is specified by the higher 7 bits, and the least significant bit is used for R/W control.)

- Manual generation of start condition and stop condition

[Interrupt function]

- Transfer end interrupt

[Error detection flag]

- Parity error (ACK error), or overrun error

[Functions not supported by simplified I²C]

- Slave transmission, slave reception
- Arbitration loss detection function
- Wait detection functions

Note When receiving the last data, ACK will not be output if 0 is written to the SOEmn bit (serial output enable register m (SOEm)) and serial communication data output is stopped. For details, see **3. 12. 8 Operation of simplified I²C (IIC00, IIC10, IIC20)**.

- 80-pin products

Address: FFFE8H After reset: FFH R/W

Symbol	7	6	5	<4>	<3>	<2>	<1>	<0>
PR00L	1	1	1	PPR02	PPR01	PPR00	LVIPR0	WDTIPR0

Address: FFFECH After reset: FFH R/W

Symbol	7	6	5	4	<3>	<2>	<1>	<0>
PR10L	1	1	1	PPR12	PPR11	PPR10	LVIPR1	WDTIPR1

Address: FFFE9H After reset: FFH R/W

Symbol	<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>
PR00H	TMPR001H SREPR00	SRPR00	STPR00 IICPR000	DMAPR01	DMAPR00	SREPR02	SRPR02 CSIPR021	STPR02 CSIPR020 IICPR020

Address: FFFEDH After reset: FFH R/W

Symbol	<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>
PR10H	TMPR101H SREPR10	SRPR10	STPR10 CSIPR100 IICPR100	DMAPR11	DMAPR10	SREPR12	SRPR12 CSIPR121	STPR12 CSIPR120 IICPR120

Address: FFFEAH After reset: FFH R/W

Symbol	<7>	<6>	<5>	<4>	3	<2>	<1>	<0>
PR01L	TMPR003	TMPR002	TMPR001	TMPR000	1	SREPR01 TMPR003H	SRPR01	STPR01 CSIPR010 IICPR010

Address: FFFEEH After reset: FFH R/W

Symbol	<7>	<6>	<5>	<4>	3	<2>	<1>	<0>
PR11L	TMPR103	TMPR102	TMPR101	TMPR100	1	SREPR11 TMPR103H	SRPR11	STPR11 CSIPR110 IICPR110

Address: FFFEBH After reset: FFH R/W

Symbol	<7>	6	5	4	<3>	<2>	1	<0>
PR01H	TMPR004	1	1	1	KRPR0	ITPR0	1	ADPR0

Address: FFFEFH After reset: FFH R/W

Symbol	<7>	6	5	4	<3>	<2>	1	<0>
PR11H	TMPR104	1	1	1	KRPR1	ITPR1	1	ADPR1

3. 17. 3. 4 Port mode registers 0 to 2, 7 (PM0 to PM2, PM7)

(1) 64-pin products

Symbol	7	6	5	4	3	2	1	0	Address	After Reset	R/W
PM0	1	PM06	PM05	PM04	PM03	PM02	PM01	PM00	FFF20H	FFH	R/W
PM1	1	PM16	1	PM14	PM13	PM12	PM11	PM10	FFF21H	FFH	R/W
PM2	PM27	PM26	PM25	PM24	PM23	PM22	PM21	PM20	FFF22H	FFH	R/W
PM7	PM77	PM76	PM75	PM74	PM73	PM72	PM71	PM70	FFF27H	FFH	R/W

Cautions 1. Be sure to clear bits 4 to 6 of the PM0 register, bit 6 of the PM1 register, bits 4 to 7 of the PM2 register, bits 4 to 7 of the PM7 register to "0".

2. Be sure to set bit 7 of the PM0 register, bits 5 and 7 of the PM1 register to "1".

(2) 80-pin products

Symbol	7	6	5	4	3	2	1	0	Address	After Reset	R/W
PM0	1	PM06	PM05	PM04	PM03	PM02	PM01	PM00	FFF20H	FFH	R/W
PM1	1	PM16	PM15	PM14	PM13	PM12	PM11	PM10	FFF21H	FFH	R/W
PM2	PM27	PM26	PM25	PM24	PM23	PM22	PM21	PM20	FFF22H	FFH	R/W
PM7	PM77	PM76	PM75	PM74	PM73	PM72	PM71	PM70	FFF27H	FFH	R/W

Cautions 1. Be sure to clear bits 5 and 6 of the PM0 register, bit 6 of the PM1 register, bits 5 to 7 of the PM2 register, bits 4 to 7 of the PM7 register to "0".

2. Be sure to set bit 7 of the PM0 register, bit 7 of the PM1 register to "1".

3. 23 Regulator

See **CHAPTER 23 REGULATOR** in **RL78/G1A Hardware User's Manual (R01UH0305E)**.

3. 25 Flash Memory

In this section, the differences of the functions and registers from RL78/G1A (64-pin products) are described. For details, see **CHAPTER 25 FLASH MEMORY** in **RL78/G1A Hardware User's Manual (R01UH0305E)**.

<R> 3. 25. 1 Serial Programming Using Flash Memory Programmer

The following dedicated flash memory programmer can be used to write data to the internal flash memory of the RL78/G1E.

- PG-FP5, FL-PR5
- E1 on-chip debugging emulator

Data can be written to the flash memory on-board or off-board, by using a dedicated flash memory programmer.

(1) On-board programming

The contents of the flash memory can be rewritten after the RL78/G1E has been mounted on the target system. The connectors that connect the dedicated flash memory programmer must be mounted on the target system.

(2) Off-board programming

Data can be written to the flash memory with a dedicated program adapter (FA series) before the RL78/G1E is mounted on the target system.

Remark FL-PR5 and FA series are products of Naito Densei Machida Mfg. Co., Ltd.

(9) Power control register 1 (PC1)

This register is used to enable or disable operation of the configurable amplifiers and the D/A converters.

Use this register to stop unused functions to reduce power consumption and noise.

When using one of configurable amplifier channels Ch1 to Ch3, be sure to set the control bit that corresponds to the channel (bits 0 to 2) to 1.

Reset signal input clears this register to 00H.

Address: 11H After reset: 00H R/W

	7	6	5	4	3	2	1	0
PC1	DAC4OF	DAC3OF	DAC2OF	DAC1OF	0	AMP3OF	AMP2OF	AMP1OF

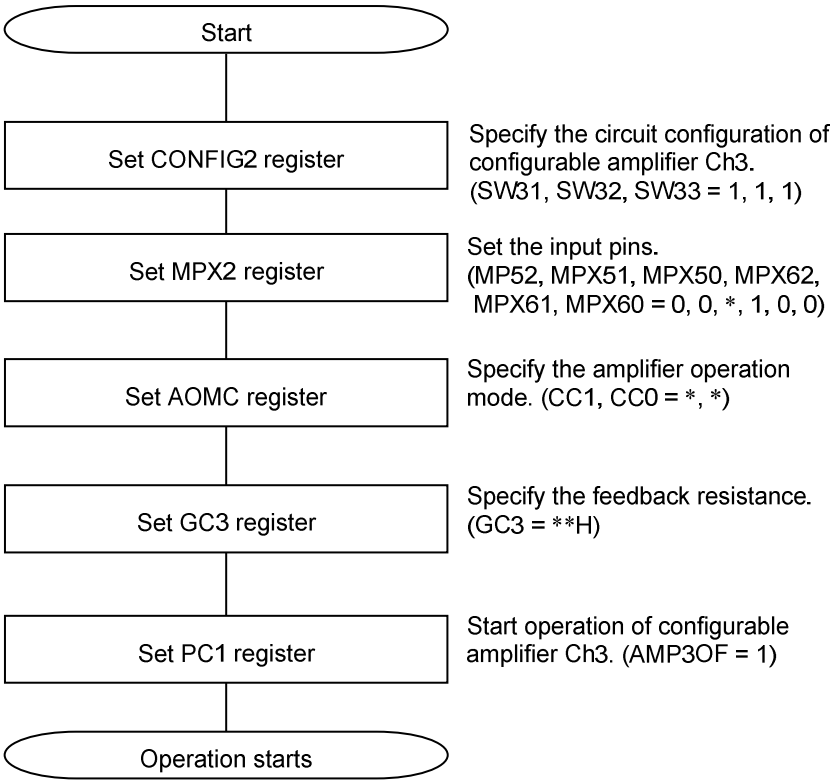
AMP3OF	Operation of configurable amplifier Ch3
0	Stop operation of configurable amplifier Ch3.
1	Enable operation of configurable amplifier Ch3.

AMP2OF	Operation of configurable amplifier Ch2
0	Stop operation of configurable amplifier Ch2.
1	Enable operation of configurable amplifier Ch2.

AMP1OF	Operation of configurable amplifier Ch1
0	Stop operation of configurable amplifier Ch1.
1	Enable operation of configurable amplifier Ch1.

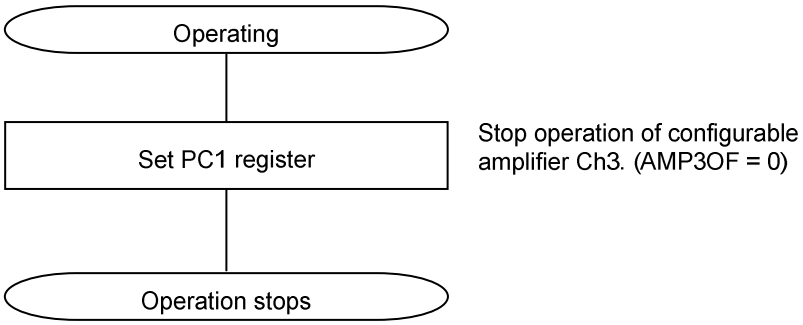
Caution Be sure to clear bit 3 to "0".

Example of procedure for starting configurable amplifier Ch3 (transimpedance amplifier)



Remark *: don't care

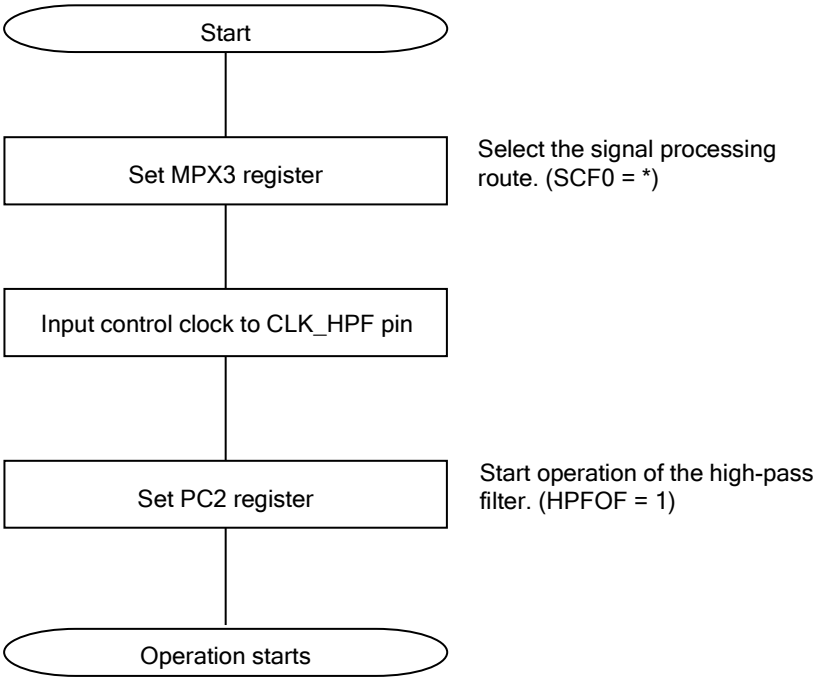
Example of procedure for stopping configurable amplifier Ch3 (transimpedance amplifier)



4. 5. 4 Procedure for operating the high-pass filter

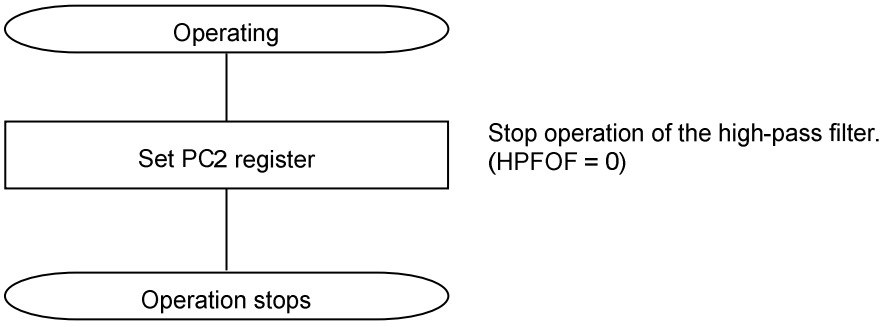
Follow the procedures below to start and stop the high-pass filter.

Example of procedure for starting the high-pass filter



Remark *: don't care

Example of procedure for stopping the high-pass filter



<R> **(9) Communication between devices at different potential (1.8 V, 2.5 V or 3 V) (CSI mode) (slave mode, SCKp ... External clock input) (1/2)**

(T_A = –40 to +85°C, 1.8 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V) (1/2)

Parameter	Symbol	Conditions	HS Note 1		LS Note 2		LV Note 3		Unit
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
SCKp cycle time Note 4	t_{KCY2}	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ Vb ≤ 4.0 V							
		24 MHz < f_{MCK}	14/f_{MCK}		–		–		ns
		20 MHz < f_{MCK} ≤ 24 MHz	12/f_{MCK}		–		–		ns
		8 MHz < f_{MCK} ≤ 20 MHz	10/f_{MCK}		–		–		ns
		4 MHz < f_{MCK} ≤ 8 MHz	8/f_{MCK}		16/f_{MCK}		–		ns
		f_{MCK} ≤ 4 MHz	6/f_{MCK}		10/f_{MCK}		10/f_{MCK}		ns
		2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ Vb ≤ 2.7 V							
		24 MHz < f_{MCK}	20/f_{MCK}		–		–		ns
		20 MHz < f_{MCK} ≤ 24 MHz	16/f_{MCK}		–		–		ns
		16 MHz < f_{MCK} ≤ 20 MHz	14/f_{MCK}		–		–		ns
		8 MHz < f_{MCK} ≤ 16 MHz	12/f_{MCK}		–		–		ns
		4 MHz < f_{MCK} ≤ 8 MHz	8/f_{MCK}		16/f_{MCK}		–		ns
		f_{MCK} ≤ 4 MHz	6/f_{MCK}		10/f_{MCK}		10/f_{MCK}		ns
		1.8 V ≤ V_{DD} < 3.3 V, 1.6 V ≤ Vb ≤ 2.0 V Note 5							
		24 MHz < f_{MCK}	48/f_{MCK}		–		–		ns
		20 MHz < f_{MCK} ≤ 24 MHz	36/f_{MCK}		–		–		ns
		16 MHz < f_{MCK} ≤ 20 MHz	32/f_{MCK}		–		–		ns
		8 MHz < f_{MCK} ≤ 16 MHz	26/f_{MCK}		–		–		ns
		4 MHz < f_{MCK} ≤ 8 MHz	16/f_{MCK}		16/f_{MCK}		–		ns
		f_{MCK} ≤ 4 MHz	10/f_{MCK}		10/f_{MCK}		10/f_{MCK}		ns

Notes 1. HS is condition of HS (high-speed main) mode.

2. LS is condition of LS (low-speed main) mode.

3. LV is condition of LV (low-voltage main) mode.

4. Transfer rate in the SNOOZE mode: MAX. 1 Mbps

5. Specify a value so as to satisfy V_{DD} ≥ Vb.

Caution Select the TTL input buffer for the SIp pin and SCKp pin and the N-ch open drain output (V_{DD} tolerance) mode for the SOp pin by using port input mode register g (PIMg) and port output mode register g (POMg).For V_{IH} and V_{IL}, see the DC characteristics with TTL input buffer selected.

(**Remarks** are listed on the page after the next page.)

<R> **(10) Communication between devices at different potential (1.8 V, 2.5 V or 3 V) (simplified I^2C mode) (1/2)**

(T_A = –40 to +85°C, 1.8 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V) (1/2)

Parameter	Symbol	Conditions	HS Note 1		LS Note 2		LV Note 3		Unit
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
SCLr clock frequency	f_{SCL}	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ Vb ≤ 4.0 V, Cb = 50 pF, Rb = 2.7 kΩ		1000 Note 4		300 Note 4		300 Note 4	kHz
		2.7 V ≤ V_{DD} ≤ 4.0 V, 2.3 V ≤ Vb ≤ 2.7 V, Cb = 50 pF, Rb = 2.7 kΩ		1000 Note 4		300 Note 4		300 Note 4	kHz
		4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ Vb ≤ 4.0 V, Cb = 100 pF, Rb = 2.8 kΩ		400 Note 4		300 Note 4		300 Note 4	kHz
		2.7 V ≤ V_{DD} ≤ 4.0 V, 2.3 V ≤ Vb ≤ 2.7 V, Cb = 100 pF, Rb = 2.7 kΩ		400 Note 4		300 Note 4		300 Note 4	kHz
		1.8 V ≤ V_{DD} < 3.3 V, 1.6 V ≤ Vb ≤ 2.0 V Note 5, Cb = 100 pF, Rb = 5.5 kΩ		300 Note 4		300 Note 4		300 Note 4	kHz
Hold time when SCLr = L	t_{LOW}	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ Vb ≤ 4.0 V, Cb = 50 pF, Rb = 2.7 kΩ	475		1550		1550		ns
		2.7 V ≤ V_{DD} ≤ 4.0 V, 2.3 V ≤ Vb ≤ 2.7 V, Cb = 50 pF, Rb = 2.7 kΩ	475		1550		1550		ns
		4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ Vb ≤ 4.0 V, Cb = 100 pF, Rb = 2.8 kΩ	1150		1550		1550		ns
		2.7 V ≤ V_{DD} ≤ 4.0 V, 2.3 V ≤ Vb ≤ 2.7 V, Cb = 100 pF, Rb = 2.7 kΩ	1150		1550		1550		ns
		1.8 V ≤ V_{DD} < 3.3 V, 1.6 V ≤ Vb ≤ 2.0 V Note 5, Cb = 100 pF, Rb = 5.5 kΩ	1550		1550		1550		ns
Hold time when SCLr = H	t_{HIGH}	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ Vb ≤ 4.0 V, Cb = 50 pF, Rb = 2.7 kΩ	245		610		610		ns
		2.7 V ≤ V_{DD} ≤ 4.0 V, 2.3 V ≤ Vb ≤ 2.7 V, Cb = 50 pF, Rb = 2.7 kΩ	200		610		610		ns
		4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ Vb ≤ 4.0 V, Cb = 100 pF, Rb = 2.8 kΩ	675		610		610		ns
		2.7 V ≤ V_{DD} ≤ 4.0 V, 2.3 V ≤ Vb ≤ 2.7 V, Cb = 100 pF, Rb = 2.7 kΩ	600		610		610		ns
		1.8 V ≤ V_{DD} < 3.3 V, 1.6 V ≤ Vb ≤ 2.0 V Note 5, Cb = 100 pF, Rb = 5.5 kΩ	610		610		610		ns

(**Notes** are listed on the next page.)

(-40°C ≤ T_A ≤ 85°C, AV_{DD1} = AV_{DD2} = AV_{DD3} = DV_{DD} = 5.0 V, VREFIN1 = VREFIN2 = VREFIN3 = 1.7 V, AMP1OF = AMP2OF = AMP3OF = 1, DAC1OF = DAC2OF = DAC3OF = 0, non-inverting amplifier) (2/2)

Parameter	Symbol	Conditions	Ratings			Unit
			MIN	TYP	MAX	
Input conversion offset voltage	VOFF00	CC1, CC0 = 0, 0, T_A = 25°C GCn = 07H (20.8 dB)	-7	–	7	mV
	VOFF01	CC1, CC0 = 0, 1, T_A = 25°C GCn = 07H (20.8 dB)	-10	–	10	mV
	VOFF10	CC1, CC0 = 1, 0, T_A = 25°C GCn = 07H (20.8 dB)	-10	–	10	mV
	VOFF11	CC1, CC0 = 1, 1, T_A = 25°C GCn = 07H (20.8 dB)	-12	–	12	mV
Input conversion offset voltage temperature coefficient	VOTC		–	±6	–	μV/°C
Slew rate	SR00	CC1, CC0 = 0, 0, CL = 30 pF, GCn = 00H (9.5 dB)	–	0.68	–	V/μs
	SR01	CC1, CC0 = 0, 1, CL = 30 pF, GCn = 00H (9.5 dB)	–	0.35	–	V/μs
	SR10	CC1, CC0 = 1, 0, CL = 30 pF, GCn = 00H (9.5 dB)	–	0.25	–	V/μs
	SR11	CC1, CC0 = 1, 1, CL = 30 pF, GCn = 00H (9.5 dB)	–	0.09	–	V/μs
Power supply rejection ratio	PSRR00	CC1, CC0 = 0, 0, GCn = 00H (9.5 dB), f = 1 kHz	–	70	–	dB
	PSRR01	CC1, CC0 = 0, 1, GCn = 00H (9.5 dB), f = 1 kHz	–	68	–	dB
	PSRR10	CC1, CC0 = 1, 0, GCn = 00H (9.5 dB), f = 1 kHz	–	62	–	dB
	PSRR11	CC1, CC0 = 1, 1, GCn = 00H (9.5 dB), f = 1 kHz	–	50	–	dB
Gain setting error	GAIN_Accu1	T_A = 25°C	-0.6	–	0.6	dB
	GAIN_Accu2	T_A = –40 to 85°C	-1.0	–	1.0	dB

Remark n = 1 to 3

($-40°C \le T_A \le 85°C$, $AV_{DD1} = AV_{DD2} = AV_{DD3} = DV_{DD} = 5.0$ V, VREFIN1 = VREFIN2 = VREFIN3 = 1.7 V, AMP1OF = AMP2OF = AMP3OF = 1, DAC1OF = DAC2OF = DAC3OF = 0, GC1 = GC2 = 03H, instrumentation amplifier) (1/2)

Parameter	Symbol	Conditions	Ratings			Unit
			MIN	TYP	MAX	
Current consumption	Icc00	AMP1OF = AMP2OF = AMP3OF = 1, CC1, CC0 = 0, 0	–	970	2,150	μA
	Icc01	AMP1OF = AMP2OF = AMP3OF = 1, CC1, CC0 = 0, 1	–	510	1,150	μA
	Icc10	AMP1OF = AMP2OF = AMP3OF = 1, CC1, CC0 = 1, 0	–	350	780	μA
	Icc11	AMP1OF = AMP2OF = AMP3OF = 1, CC1, CC0 = 1, 1	–	140	330	μA
Input voltage	VINL		AGND1 - 0.1	–	–	V
	VINH		–	–	AV_{DD1} - 1.5	V
Output voltage	VOUTL	IOL = -200 μA	–	AGND1 + 0.02	AGND1 + 0.06	V
	VOUTH	IOH = 200 μA	AV_{DD1}- 0.06	AV_{DD1} - 0.02	–	V
Settling time	t_{SET_AMP00}	GC3 = 00H (20 dB), CC1, CC0 = 0, 0, CL = 30 pF, output voltage = $1V_{PP}$, output convergence voltage V_{PP} = 999 mV	–	–	9	μs
	t_{SET_AMP01}	GC3 = 00H (20 dB), CC1, CC0 = 0, 1, CL = 30 pF, output voltage = $1V_{PP}$, output convergence voltage V_{PP} = 999 mV	–	–	18	μs
	t_{SET_AMP10}	GC3 = 00H (20 dB), CC1, CC0 = 1, 0, CL = 30 pF, output voltage = $1V_{PP}$, output convergence voltage V_{PP} = 999 mV	–	–	28	μs
	t_{SET_AMP11}	GC3 = 00H (20 dB), CC1, CC0 = 1, 1, CL = 30 pF, output voltage = $1V_{PP}$, output convergence voltage V_{PP} = 999 mV	–	–	71	μs
Gain bandwidth	GBW00	CL = 30 pF, CC1, CC0 = 0, 0 GC3 = 11H (54 dB)	–	1.82	–	MHz
	GBW01	CL = 30 pF, CC1, CC0 = 0, 1 GC3 = 11H (54 dB)	–	1.03	–	MHz
	GBW10	CL = 30 pF, CC1, CC0 = 1, 0 GC3 = 11H (54 dB)	–	0.69	–	MHz
	GBW11	CL = 30 pF, CC1, CC0 = 1, 1 GC3 = 11H (54 dB)	–	0.22	–	MHz
Equivalent input noise	En00	CC1, CC0 = 0, 0 GC3 = 11H (54 dB) f = 1 kHz	–	90	–	nV/√ Hz
	En01	CC1, CC0 = 0, 1 GC3 = 11H (54 dB) f = 1 kHz	–	119	–	nV/√ Hz
	En10	CC1, CC0 = 1, 0 GC3 = 11H (54 dB) f = 1 kHz	–	150	–	nV/√ Hz
<R>	En11	CC1, CC0 = 1, 1 GC3 = 11H (54 dB) f = 1 kHz	–	260	–	nV/√ Hz

(2) 80-pin products

(–40°C ≤ T_A ≤ 85°C, AV_{DD1} = AV_{DD2} = AV_{DD3} = DV_{DD} = 5.0 V, VREFIN4 = 1.7 V, GAINOF = 1, DAC4OF = 0)

Parameter	Symbol	Conditions	Ratings			Unit
			MIN	TYP	MAX	
Current consumption	IccA		–	530	1,300	μA
Input voltage	VINL		AGND2 - 0.1	–	–	V
	VINH		–	–	AV_{DD1} - 0.05	V
Output voltage	VOUTL1	IOL = -100 μA, GAINAMP_OUT pin	–	AGND2 + 0.02	AGND2 + 0.05	V
	VOUTH1	IOH = 100 μA, GAINAMP_OUT pin	AV_{DD1} - 0.05	AV_{DD1} - 0.02	–	V
	VOUTL2	IOL = -100 μA, SYNCH_OUT pin	–	AGND2 + 0.03	AGND2 + 0.06	V
	VOUTH2	IOH = 100 μA, SYNCH_OUT pin	AV_{DD1} - 0.06	AV_{DD1} - 0.03	–	V
Gain bandwidth	GBW1	CLK_SYNCH = H, SYNCH_OUT pin CL = 30 pF, GC4 = 11H (40 dB)	–	1.38	–	MHz
	GBW2	CLK_SYNCH = L, SYNCH_OUT or GAINAMP_OUT pin CL = 30 pF, GC4 = 11H (40 dB)	–	0.86	–	MHz
Input conversion offset voltage	VOFF	GC4 = 00H (6 dB), T_A = 25°C, GAINAMP_IN = 2.5 V	-30	–	30	mV
Input conversion offset voltage temperature coefficient	VOTC1	CLK_SYNCH = H, SYNCH_OUT pin	–	±6	–	μV/°C
	VOTC2	CLK_SYNCH = L, GAINAMP_OUT pin	–	±18	–	μV/°C
Slew rate	SR	CL = 30 pF	–	0.9	–	V/μs
Equivalent input noise	En_Gain	f = 1 kHz, GC4 = 11H (40 dB) GAINAMP_OUT pin	–	700	–	nV/√ Hz
Power supply rejection ratio	PSRR1	CLK_SYNCH = H, SYNCH_OUT pin, f = 1 kHz, GC4 = 00H (6 dB)	–	60	–	dB
	PSRR2	CLK_SYNCH = L, SYNCH_OUT or GAINAMP_OUT pin, f = 1 kHz, GC4 = 00H (6 dB)	–	45	–	dB
Gain setting error	GAIN_Accu1	T_A = 25°C	-0.6	–	0.6	dB
	GAIN_Accu2	T_A = –40 to 85°C	-1.0	–	1.0	dB
CLK_SYNCH low-level input voltage	V_{ILCLK_SYNCH}				0.3 × AV_{DD1}	V
CLK_SYNCH high-level input voltage	V_{IHCLK_SYNCH}		0.7 × AV_{DD1}			V