# Renesas Electronics America Inc - R5F10FMEAFB#YB1 Datasheet

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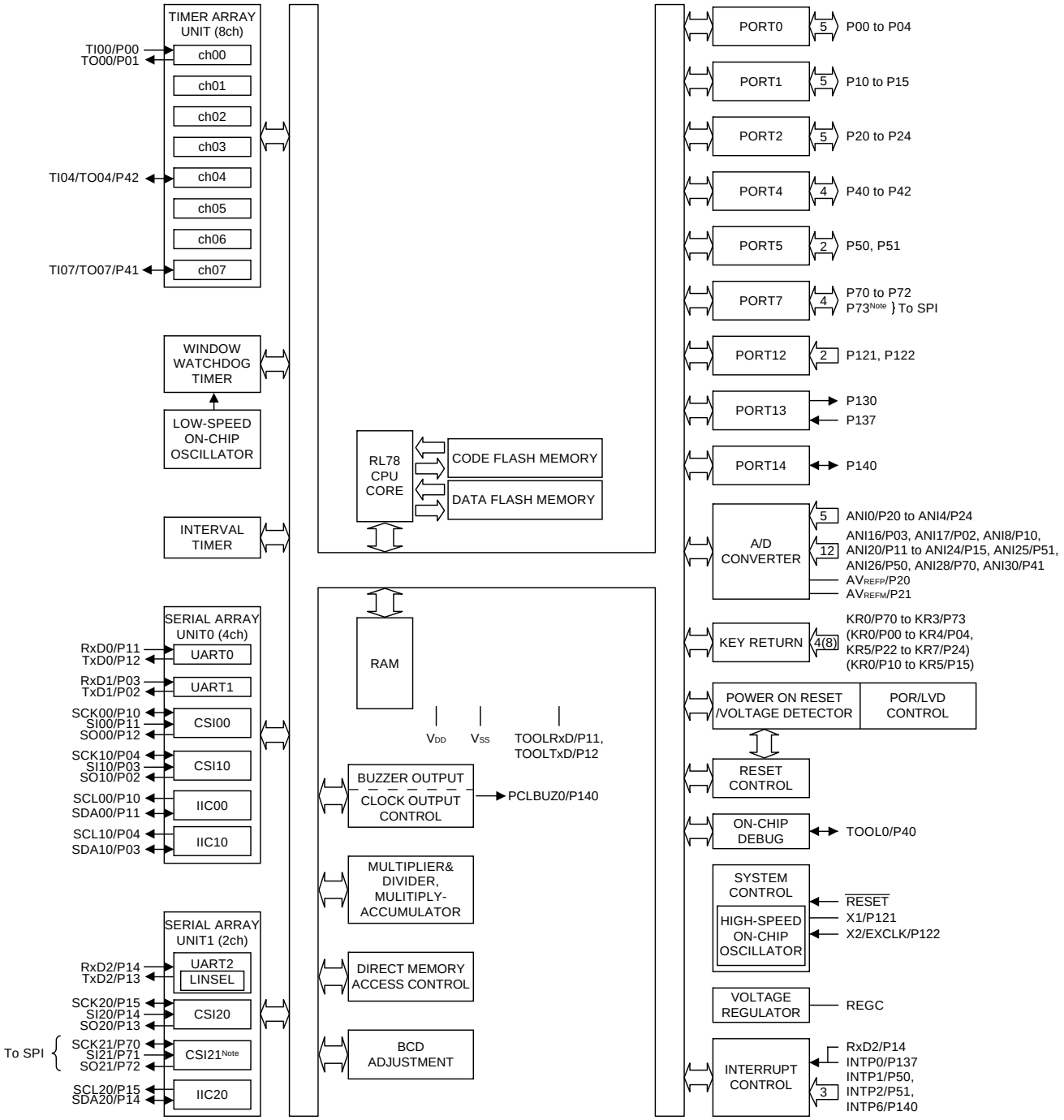
## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Obsolete |
| Core Processor | RL78 |
| Core Size | 16-Bit |
| Speed | 32MHz |
| Connectivity | CSI, I²C, LINbus, UART/USART |
| Peripherals | DMA, LVD, POR, PWM, WDT |
| Number of I/O | 26 |
| Program Memory Size | 64KB (64K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | 4K x 8 |
| RAM Size | 4K x 8 |
| Voltage - Supply (Vcc/Vdd) | 1.6V ~ 5.5V |
| Data Converters | A/D 17x8/12b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 80-LQFP |
| Supplier Device Package | 80-LFQFP (12x12) |
| Purchase URL | https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f10fmeafb-yb1 |

<R> **(1) Block diagram in microcontroller block (80-pin products)**




**Note** Connected inside the package.

**Table 1-1 Outline of Functions (Microcontroller Block)** (2/2)

| Item | | 64-pin products | 80-pin products |
|---|---|---|---|
| | | R5F10FLx | R5F10FMx |
| Serial interface | | • 64-pin products<br>CSI: 1 channel / simplified $I^2C$: 1 channel / UART: 1 channel<br>UART: 1 channel<br>CSI: 1 channel / UART (LIN-bus supported): 1 channel<br>• 80-pin products<br>CSI: 1 channel / simplified $I^2C$: 1 channel / UART: 1 channel<br>CSI: 1 channel / simplified $I^2C$: 1 channel / UART: 1 channel<br>CSI: 2 channels / simplified $I^2C$: 1 channel / UART (LIN-bus supported): 1 channel | |
| | $I^2C$ bus | – | |
| Multiplier and divider / multiply accumulator | | Multiplier: 16 bits × 16 bits (Unsigned or signed)<br>Divider: 32 bits ÷ 32 bits (Unsigned)<br>Multiply accumulator: 16 bits × 16 bits + 32 bits (Unsigned or signed) | |
| DMA controller | | 2 channels | |
| Vectored interrupt sources | Internal | 25 | |
| | External | 2 | 5 |
| Key interrupt | | 4 ch (7) Note 1 | 4 ch (8) Note 1 |
| Reset | | • Reset by $\overline{\text{RESET}}$ pin<br>• Internal reset by watchdog timer<br>• Internal reset by power-on-reset<br>• Internal reset by voltage detector<br>• Internal reset by illegal instruction execution Note 2<br>• Internal reset by RAM parity error<br>• Internal reset by illegal-memory access | |
| Power-on-reset circuit | | • Power-on-reset: 1.51 ±0.03 V<br>• Power-down-reset: 1.50 ±0.03 V | |
| Voltage detector | | Detection level: 3 stages | |
| On-chip debug function | | Provided | |

<R>

**Notes 1.** The number in parentheses is the channels of key interrupt when using the peripheral I/O redirection register (PIOR).

**2.** The illegal instruction is generated when instruction code FFH is executed. Rest by the illegal instruction execution is not issued by emulation with the in-circuit emulator or on-chip debug emulator.

<R> **2. 1. 1. 1 64-pin products**

(1/2)

| Function Name | Pin Type | I/O | After Reset | Alternate Function | Function |
|---|---|---|---|---|---|
| P00 | 8-1-1 | I/O | Input port | TI00/(KR0) | Port 0.<br>4-bit I/O port.<br>Input of P00, P01, and P03 can be set to TTL input buffer.<br>Output of P02 and P03 can be set to N-ch open-drain output ($V_{DD}$ tolerance).<br>P02 and P03 can be set to analog input. Note1<br>Input/output can be specified in 1-bit units.<br>Use of an on-chip pull-up resistor can be specified by a software setting at input port. |
| P01 | | | | TO00/(KR1) | |
| P02 | 7-3-2 | | Analog input port | ANI17/TxD1/(KR2) | |
| P03 | 8-3-2 | | | ANI16/RxD1/(KR3) | |
| P10 | 8-3-2 | I/O | Analog input port | ANI18/SCK00/SCL00/(KR0) | Port 1.<br>5-bit I/O port.<br>Input of P10, P11, and P14 can be set to TTL input buffer.<br>Output of P10 to P14 can be set to N-ch open-drain output ($V_{DD}$ tolerance).<br>P10 to P14 can be set to analog input. Note 1<br>Input/output can be specified in 1-bit units.<br>Use of an on-chip pull-up resistor can be specified by a software setting at input port. |
| P11 | | | | ANI20/SI00/RxD0/TOOLRxD/SDA00/(KR1) | |
| P12 | 7-3-2 | | | ANI21/SO00/TxD0/TOOLTxD/(KR2) | |
| P13 | | | | ANI22/TxD2/(KR3) | |
| P14 | 8-3-2 | | | ANI23/RxD2/(KR4) | |
| P20 | 4-3-1 | I/O | Analog input port | ANI0/$AV_{REFP}$ | Port 2.<br>4-bit I/O port.<br>Can be set to analog input. Note 2<br>Input/output can be specified in 1-bit units. |
| P21 | | | | ANI1/$AV_{REFM}$ | |
| P22 | | | | ANI2/(KR5) | |
| P23 | | | | ANI3/(KR6) | |
| P40 | 7-1-1 | I/O | Input port | TOOL0 | Port 4.<br>3-bit I/O port.<br>P41 can be set to analog input. Note 1<br>Input/output can be specified in 1-bit units.<br>Use of an on-chip pull-up resistor can be specified by a software setting at input port. |
| P41 | 7-3-1 | | Analog input port | ANI30/TI07/TO07 | |
| P42 | 7-1-1 | | Input port | TI04/TO04 | |
| P70 | 7-3-1 | I/O | Analog input port | ANI28/KR0/SCK21/$\overline{SCLK}$ Note3 | Port 7.<br>4-bit I/O port.<br>P70 can be set to analog input. Note 1<br>Input/output can be specified in 1-bit units.<br>Use of an on-chip pull-up resistor can be specified by a software setting at input port. |
| P71 | 7-1-2 | | Input port | KR1/SI21/SDO Note3 | |
| P72 | 7-1-1 | | | KR2/SO21/SDI Note3 | |
| P73 | | | | KR3/$\overline{CS}$ Note3 | |

<R> **Notes 1.** Digital or analog for each pin can be selected with the port mode control register x (PMCx) (can be set in 1-bit units).

**2.** Digital or analog for each pin can be selected with the A/D port configuration register (ADPC).

**3.** $\overline{SCLK}$, SDO, SDI, $\overline{CS}$ represent the pin functions of analog block. P70 to P73 which are connected to the pins of the chip of analog block inside the package have some alternate functions for analog block.

<R> **Remark** Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR). About format, see Figure in **3. 4. 3. 8 Peripheral I/O redirection register (PIOR)**.

(2/2)

<R>

| Function Name | Pin Type | I/O | After Reset | Alternate Function | Function |
|---|---|---|---|---|---|
| P50 | 7-3-2 | I/O | Analog input port | ANI26/INTP1 | Port 5.<br>2-bit I/O port.<br>Output of P50 can be set to N-ch open-drain output ($V_{DD}$ tolerance).<br>P50 and P51 can be set to analog input. Note 1<br>Input/output can be specified in 1-bit units.<br>Use of an on-chip pull-up resistor can be specified by software setting at input port. |
| P51 | 7-3-1 | | | ANI25/INTP2 | |
| P70 | 7-3-1 | I/O | Analog input port | ANI28/KR0/ SCK21/$\overline{\text{SCLK}}$ Note2 | Port 7.<br>4-bit I/O port.<br>P70 can be set to analog input. Note 1<br>Input/output can be specified in 1-bit units.<br>Use of an on-chip pull-up resistor can be specified by software setting at input port. |
| P71 | 7-1-2 | | Input port | KR1/SI21/SDO Note2 | |
| P72 | 7-1-1 | | | KR2/SO21/SDI Note2 | |
| P73 | | | | KR3/$\overline{\text{CS}}$ Note2 | |
| P121 | 2-2-1 | Input | Input port | X1 | Port 12.<br>2-bit input port. |
| P122 | | | | X2/EXCLK | |
| P130 | 1-1-1 | Output | Output port | – | Port 13.<br>1-bit output port and 1-bit input port. |
| P137 | 2-1-2 | Input | Input port | INTP0 | |
| P140 | 7-1-1 | I/O | Input port | PCLBUZ0/INTP6 | Port 14.<br>1-bit I/O port.<br>Input/output can be specified in 1-bit units.<br>Use of an on-chip pull-up resistor can be specified by a software setting at input port. |
| RESET | 2-1-1 | Input | – | – | Input only pin for external reset.<br>When external reset is not used, connect this pin to $V_{DD}$ directly or via a resistor. |

<R> **Notes 1.** Digital or analog for each pin can be selected with the port mode control register x (PMCx) (can be set in 1-bit units).

**2.** $\overline{\text{SCLK}}$, SDO, SDI, $\overline{\text{CS}}$ represent the pin functions of analog block. P70 to P73 which are connected to the pins of the chip of analog block inside the package have some alternate functions for analog block.

**Table 3-3. List of Differences in Expanded Special Function Registers (2nd SFRs) (5/6)**

| Address | RL78/G1E (64-pin products) | | | RL78/G1A (64-pin products) | | |
|---|---|---|---|---|---|---|
| | 2nd SFRs Name | Symbol | | 2nd SFRs Name | Symbol | |
| F0180H | Same as RL78/G1A (64-pin products) | TCR00 | | Timer counter register 00 | TCR00 | |
| F0181H | | | | | | |
| F0182H | Same as RL78/G1A (64-pin products) | TCR01 | | Timer counter register 01 | TCR01 | |
| F0183H | | | | | | |
| F0184H | Same as RL78/G1A (64-pin products) | TCR02 | | Timer counter register 02 | TCR02 | |
| F0185H | | | | | | |
| F0186H | Same as RL78/G1A (64-pin products) | TCR03 | | Timer counter register 03 | TCR03 | |
| F0187H | | | | | | |
| F0188H | Same as RL78/G1A (64-pin products) | TCR04 | | Timer counter register 04 | TCR04 | |
| F0189H | | | | | | |
| F018AH | Same as RL78/G1A (64-pin products) | TCR05 | | Timer counter register 05 | TCR05 | |
| F018BH | | | | | | |
| F018CH | Same as RL78/G1A (64-pin products) | TCR06 | | Timer counter register 06 | TCR06 | |
| F018DH | | | | | | |
| F018EH | Same as RL78/G1A (64-pin products) | TCR07 | | Timer counter register 07 | TCR07 | |
| F018FH | | | | | | |
| F0190H | Same as RL78/G1A (64-pin products) | TMR00 | | Timer mode register 00 | TMR00 | |
| F0191H | | | | | | |
| F0192H | Timer mode register 01 Note | TMR01 | | Timer mode register 01 | TMR01 | |
| F0193H | | | | | | |
| F0194H | Timer mode register 02 Note | TMR02 | | Timer mode register 02 | TMR02 | |
| F0195H | | | | | | |
| F0196H | Timer mode register 03 Note | TMR03 | | Timer mode register 03 | TMR03 | |
| F0197H | | | | | | |
| F0198H | Same as RL78/G1A (64-pin products) | TMR04 | | Timer mode register 04 | TMR04 | |
| F0199H | | | | | | |
| F019AH | Timer mode register 05 Note | TMR05 | | Timer mode register 05 | TMR05 | |
| F019BH | | | | | | |
| F019CH | Timer mode register 06 Note | TMR06 | | Timer mode register 06 | TMR06 | |
| F019DH | | | | | | |
| F019EH | Same as RL78/G1A (64-pin products) | TMR07 | | Timer mode register 07 | TMR07 | |
| F019FH | | | | | | |
| F01A0H | Same as RL78/G1A (64-pin products) | TSR00L | TSR00 | Timer status register 00 | TSR00L | TSR00 |
| F01A1H | | – | | | – | |
| F01A2H | Same as RL78/G1A (64-pin products) | TSR01L | TSR01 | Timer status register 01 | TSR01L | TSR01 |
| F01A3H | | – | | | – | |
| F01A4H | Same as RL78/G1A (64-pin products) | TSR02L | TSR02 | Timer status register 02 | TSR02L | TSR02 |
| F01A5H | | – | | | – | |
| F01A6H | Same as RL78/G1A (64-pin products) | TSR03L | TSR03 | Timer status register 03 | TSR03L | TSR03 |
| F01A7H | | – | | | – | |
| F01A8H | Same as RL78/G1A (64-pin products) | TSR04L | TSR04 | Timer status register 04 | TSR04L | TSR04 |
| F01A9H | | – | | | – | |
| F01AAH | Same as RL78/G1A (64-pin products) | TSR05L | TSR05 | Timer status register 05 | TSR05L | TSR05 |
| F01ABH | | – | | | – | |
| F01ACH | Same as RL78/G1A (64-pin products) | TSR06L | TSR06 | Timer status register 06 | TSR06L | TSR06 |
| F01ADH | | – | | | – | |
| F01AEH | Same as RL78/G1A (64-pin products) | TSR07L | TSR07 | Timer status register 07 | TSR07L | TSR07 |
| F01AFH | | – | | | – | |

**Note** The bit setting is different from that of RL78/G1A (64-pin products).

**Table 3-4. List of Differences in Expanded Special Function Registers (2nd SFRs) (5/6)**

| Address | RL78/G1E (80-pin products) | | | RL78/G1A (64-pin products) | | |
|---|---|---|---|---|---|---|
| | 2nd SFRs Name | Symbol | | 2nd SFRs Name | Symbol | |
| F0180H | Same as RL78/G1A (64-pin products) | TCR00 | | Timer counter register 00 | TCR00 | |
| F0181H | | | | | | |
| F0182H | Same as RL78/G1A (64-pin products) | TCR01 | | Timer counter register 01 | TCR01 | |
| F0183H | | | | | | |
| F0184H | Same as RL78/G1A (64-pin products) | TCR02 | | Timer counter register 02 | TCR02 | |
| F0185H | | | | | | |
| F0186H | Same as RL78/G1A (64-pin products) | TCR03 | | Timer counter register 03 | TCR03 | |
| F0187H | | | | | | |
| F0188H | Same as RL78/G1A (64-pin products) | TCR04 | | Timer counter register 04 | TCR04 | |
| F0189H | | | | | | |
| F018AH | Same as RL78/G1A (64-pin products) | TCR05 | | Timer counter register 05 | TCR05 | |
| F018BH | | | | | | |
| F018CH | Same as RL78/G1A (64-pin products) | TCR06 | | Timer counter register 06 | TCR06 | |
| F018DH | | | | | | |
| F018EH | Same as RL78/G1A (64-pin products) | TCR07 | | Timer counter register 07 | TCR07 | |
| F018FH | | | | | | |
| F0190H | Same as RL78/G1A (64-pin products) | TMR00 | | Timer mode register 00 | TMR00 | |
| F0191H | | | | | | |
| F0192H | Timer mode register 01 Note | TMR01 | | Timer mode register 01 | TMR01 | |
| F0193H | | | | | | |
| F0194H | Timer mode register 02 Note | TMR02 | | Timer mode register 02 | TMR02 | |
| F0195H | | | | | | |
| F0196H | Timer mode register 03 Note | TMR03 | | Timer mode register 03 | TMR03 | |
| F0197H | | | | | | |
| F0198H | Same as RL78/G1A (64-pin products) | TMR04 | | Timer mode register 04 | TMR04 | |
| F0199H | | | | | | |
| F019AH | Timer mode register 05 Note | TMR05 | | Timer mode register 05 | TMR05 | |
| F019BH | | | | | | |
| F019CH | Timer mode register 06 Note | TMR06 | | Timer mode register 06 | TMR06 | |
| F019DH | | | | | | |
| F019EH | Same as RL78/G1A (64-pin products) | TMR07 | | Timer mode register 07 | TMR07 | |
| F019FH | | | | | | |
| F01A0H | Same as RL78/G1A (64-pin products) | TSR00L | TSR00 | Timer status register 00 | TSR00L | TSR00 |
| F01A1H | | — | | | — | |
| F01A2H | Same as RL78/G1A (64-pin products) | TSR01L | TSR01 | Timer status register 01 | TSR01L | TSR01 |
| F01A3H | | — | | | — | |
| F01A4H | Same as RL78/G1A (64-pin products) | TSR02L | TSR02 | Timer status register 02 | TSR02L | TSR02 |
| F01A5H | | — | | | — | |
| F01A6H | Same as RL78/G1A (64-pin products) | TSR03L | TSR03 | Timer status register 03 | TSR03L | TSR03 |
| F01A7H | | — | | | — | |
| F01A8H | Same as RL78/G1A (64-pin products) | TSR04L | TSR04 | Timer status register 04 | TSR04L | TSR04 |
| F01A9H | | — | | | — | |
| F01AAH | Same as RL78/G1A (64-pin products) | TSR05L | TSR05 | Timer status register 05 | TSR05L | TSR05 |
| F01ABH | | — | | | — | |
| F01ACH | Same as RL78/G1A (64-pin products) | TSR06L | TSR06 | Timer status register 06 | TSR06L | TSR06 |
| F01ADH | | — | | | — | |
| F01AEH | Same as RL78/G1A (64-pin products) | TSR07L | TSR07 | Timer status register 07 | TSR07L | TSR07 |
| F01AFH | | — | | | — | |

**Note** The bit setting is different from that of RL78/G1A (64-pin products).

### 3. 6. 3. 13 Input switch control register (ISC)

The bit setting is same as that of RL78/G1A (64-pin products). For details, see **6. 3. 13 Input switch control register (ISC)** in **RL78/G1A Hardware User's Manual (R01UH0305E)**.

### 3. 6. 3. 14 Noise filter enable register 1 (NFEN1)

Address: F0071H After reset: 00H R/W

| Symbol | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| NFEN1 | TNFEN07 | 0 | 0 | TNFEN04 | 0 | 0 | 0 | TNFEN00 |

| TNFEN07 | Enable/disable using noise filter of TI07/TO07/P41 pin or RxD2/P14 pin input signal[Note] |
|---|---|
| 0 | Noise filter OFF |
| 1 | Noise filter ON |

| TNFEN04 | Enable/disable using noise filter of TI04/TO04/P42 pin input signal |
|---|---|
| 0 | Noise filter OFF |
| 1 | Noise filter ON |

| TNFEN00 | Enable/disable using noise filter of TI00/P00 pin input signal |
|---|---|
| 0 | Noise filter OFF |
| 1 | Noise filter ON |

**Note** The applicable pin can be switched by setting the ISC1 bit of the ISC register.
ISC1 = 0: Whether or not to use the noise filter of the TI07 pin can be selected.
ISC1 = 1: Whether or not to use the noise filter of the RxD2 pin can be selected.

**Caution Be sure to clear bits 6, 5, 3 to 1 to "0".**

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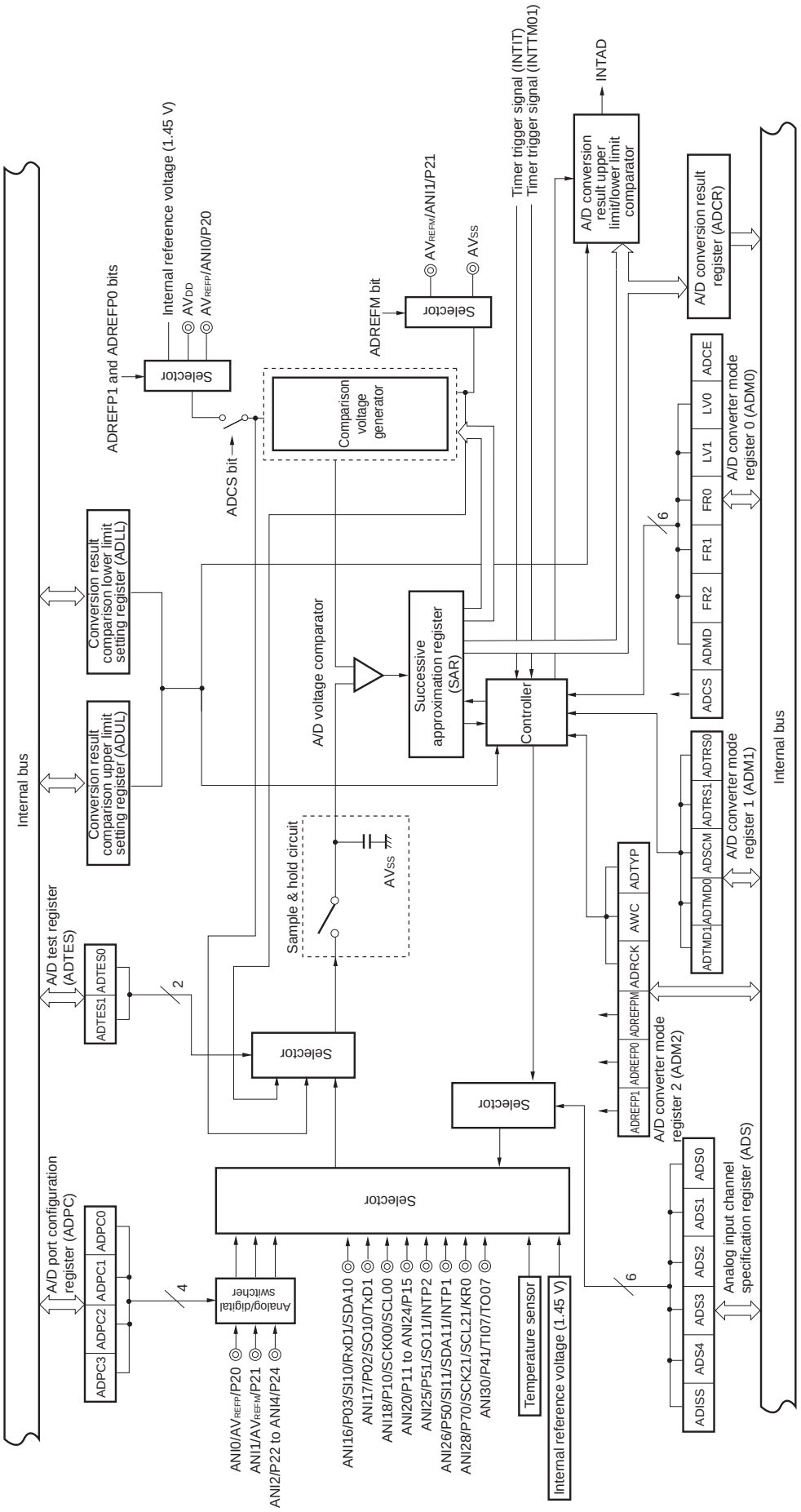
**Figure 3-8. Block Diagram of A/D Converter**




**Remark** Analog input pins drawn in this figure is for the case of 80-pin products

**Table 3-13. Interrupt Source List (2/3)**

| | Interrupt Type | Default Priority[Note 1] | Interrupt Source | | Internal/External | Vector Table Address | Basic Configuration Type[Note 2] | RL78/G1E | |
|---|---|---|---|---|---|---|---|---|---|
| | | | Name | Trigger | | | | 64-pin | 80-pin |
| | Maskable | 16 | INTST1/ INTCSI10/ INTIIC10 | UART1 transmission transfer end or buffer empty interrupt/ CSI10 transfer end or buffer empty interrupt/ IIC10 transfer end | Internal | 0024H | (A) | √[Note 3] | √ |
| | | 17 | INTSR1/ INTCSI11/ INTIIC11 | UART1 reception transfer end/ CSI11 transfer end or buffer empty interrupt/ IIC11 transfer end | | 0026H | | √[Note 4] | √[Note 4] |
| | | 18 | INTSRE1 | UART1 reception communication error occurrence | | 0028H | | √ | √ |
| <R> | | | INTTM03H | End of timer channel 3 count or capture (at higher 8-bit timer operation) | | | | √ | √ |
| | | 19 | INTIICA0 | End of IICA0 communication | | 002AH | | – | – |
| | | 20 | INTTM00 | End of timer channel 0 count or capture | | 002CH | | √ | √ |
| <R> | | 21 | INTTM01 | End of timer channel 1 count or capture (at 16-bit/lower 8-bit timer operation) | | 002EH | | √ | √ |
| | | 22 | INTTM02 | End of timer channel 2 count or capture | | 0030H | | √ | √ |
| <R> | | 23 | INTTM03 | End of timer channel 3 count or capture (at 16-bit/lower 8-bit timer operation) | | 0032H | | √ | √ |
| | | 24 | INTAD | End of A/D conversion | | 0034H | | √ | √ |
| | | 25 | INTRTC | Fixed-cycle signal of real-time clock/alarm match detection | | 0036H | | – | – |
| | | 26 | INTIT | Interval signal of 12-bit interval timer detection | | 0038H | | √ | √ |
| | | 27 | INTKR | Key return signal detection | External | 003AH | (C) | √ | √ |
| | | 28 | INTTM04 | End of timer channel 4 count or capture | Internal | 0042H | (A) | √ | √ |

**Notes 1.** The default priority determines the sequence of interrupts if two or more maskable interrupts occur simultaneously. Zero indicates the highest priority and 39 indicates the lowest priority.

**2.** Basic configuration types (A) to (D) correspond to (A) to (D) in Figure 3-13.

**3.** INTST1 only.

**4.** INTSR1 only.

**Format of User Option Byte (000C1H/010C1H) (2/2)**

Address: 000C1H/010C1H[Note]

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| VPOC2 | VPOC1 | VPOC0 | 1 | LVIS1 | LVIS0 | LVIMDS1 | LVIMDS0 |

- LVD setting (interrupt mode)

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| Detection voltage | | Option byte setting value | | | | | | |
|---|---|---|---|---|---|---|---|---|
| $V_{LVDH}$ | | VPOC2 | VPOC1 | VPOC0 | LVIS1 | LVIS0 | Mode setting | |
| Rising edge | Falling edge | | | | | | LVIMDS1 | LVIMDS0 |
| 3.13 | 3.06 | 0 | 0 | 1 | 0 | 0 | 0 | 1 |
| 3.75 | 3.67 | 0 | 1 | 0 | 0 | 0 | | |
| 4.06 | 3.98 | 0 | 1 | 1 | 0 | 0 | | |
| – | | Value other than above is setting prohibited. | | | | | | |

- LVD off (use of external reset input via $\overline{\text{RESET}}$ pin)

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| Detection voltage | | Option byte setting value | | | | | | |
|---|---|---|---|---|---|---|---|---|
| $V_{LVD}$ | | VPOC2 | VPOC1 | VPOC0 | LVIS1 | LVIS0 | Mode setting | |
| Rising edge | Falling edge | | | | | | LVIMDS1 | LVIMDS0 |
| – | – | 1 | × | × | × | × | × | 1 |
| – | | Value other than above is setting prohibited. | | | | | | |

**Note** Set the same value as 000C1H to 010C1H when the boot swap operation is used because 000C1H is replaced by 010C1H.

<R> **Cautions1. Set bit 4 to 1.**

**2. After power is supplied, the reset state must be retained until the operating voltage becomes in the range defined in 5. 2. 3 AC characteristics. This is done by utilizing the voltage detector or controlling the externally input reset signal. After the power supply is turned off, this LSI should be placed in the STOP mode, or placed in the reset state by utilizing the voltage detector or controlling the externally input reset signal, before the voltage falls below the operating range. The range of operating voltage varies with the setting of the user option byte (000C2H or 010C2H).**

<R> **Remarks 1.** ×: don't care

**2.** For details on the LVD circuit, see **3. 21 Voltage Detector**.

**3.** The detection voltage is a TYP. value. For details, see **5. 2. 5. 4 LVD circuit characteristics**.

**Table 4-2. Gain of Configurable Amplifier Ch1 (Inverting Amplifier and Differential Amplifier)**

| AMPG14 | AMPG13 | AMPG12 | AMPG11 | AMPG10 | Gain of Configurable Amplifier Ch1 (Typ.) |
|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 6 dB |
| 0 | 0 | 0 | 0 | 1 | 8 dB |
| 0 | 0 | 0 | 1 | 0 | 10 dB |
| 0 | 0 | 0 | 1 | 1 | 12 dB |
| 0 | 0 | 1 | 0 | 0 | 14 dB |
| 0 | 0 | 1 | 0 | 1 | 16 dB |
| 0 | 0 | 1 | 1 | 0 | 18 dB |
| 0 | 0 | 1 | 1 | 1 | 20 dB |
| 0 | 1 | 0 | 0 | 0 | 22 dB |
| 0 | 1 | 0 | 0 | 1 | 24 dB |
| 0 | 1 | 0 | 1 | 0 | 26 dB |
| 0 | 1 | 0 | 1 | 1 | 28 dB |
| 0 | 1 | 1 | 0 | 0 | 30 dB |
| 0 | 1 | 1 | 0 | 1 | 32 dB |
| 0 | 1 | 1 | 1 | 0 | 34 dB |
| 0 | 1 | 1 | 1 | 1 | 36 dB |
| 1 | 0 | 0 | 0 | 0 | 38 dB |
| 1 | 0 | 0 | 0 | 1 | 40 dB |
| Other than above | | | | | Setting prohibited |

# CHAPTER 5 ELECTRICAL SPECIFICATIONS

In this capter, the electrical specification is described for the target products shown below.

Target products A: Consumer applications $T_A$ = −40 to +85°C
R5F10FLCANA, R5F10FLCANA, R5F10FLDANA, R5F10FLDANA,
R5F10FLEANA, R5F10FLEANA, R5F10FMCAFB, R5F10FMCAFB,
R5F10FMDAFB, R5F10FMDAFB, R5F10FMEAFB, R5F10FMEAFB

Target products D: Industrial applications $T_A$ = −40 to +85°C
R5F10FLCDNA, R5F10FLCDNA, R5F10FLDDNA, R5F10FLDDNA,
R5F10FLEDNA, R5F10FLEDNA, R5F10FMCDFB, R5F10FMCDFB,
R5F10FMDDFB, R5F10FMDDFB, R5F10FMEDFB, R5F10FMEDFB

**Cautions 1. The RL78/G1E microcontrollers have an on-chip debug function, which is provided for development and evaluation. Do not use the on-chip debug function in products designated for mass production, because the guaranteed number of rewritable times of the flash memory may be exceeded when this function is used, and product reliability therefore cannot be guaranteed. Renesas Electronics is not liable for problems occurring when the on-chip debug function is used.**

**2. The pins mounted depend on the product, so that refer to CHAPTER 2 PIN FUNCTIONS. In this Chapter, most of the descriptions use the case of 80-pin products as an example.**

($T_A$ = –40 to +85°C, 1.6 V ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = 0 V) (3/3)

| Parameter | Symbol | Conditions | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|
| <R> Low-speed on-chip oscillator operating current | $I_{FIL}$ Note 1 | | | | 0.20 | | μA |
| 12-bit Interval timer operating current | $I_{IT}$ Note 1, 2, 3 | | | | 0.02 Note 3 | | μA |
| Watchdog timer operating current | $I_{WDT}$ Note 1, 2, 4 | $f_{IL}$ = 15 kHz, $f_{MAIN}$ is stopped | | | 0.22 | | μA |
| A/D converter operating current | $I_{ADC}$ Note 5, 6 | $AV_{DD}$ = 3.0 V, When conversion at maximum speed | | | 420 | 720 | μA |
| $AV_{REF(+)}$ current | $I_{AVREF}$ Note 7 | $AV_{DD}$ = 3.0 V, ADREFP1 = 0, ADREFP0 = 0 Note 6 | | | 14.0 | 25.0 | μA |
| | | $AV_{REFP}$ = 3.0 V, ADREFP1 = 0, ADREFP0 = 1 Note 9 | | | 14.0 | 25.0 | μA |
| | | ADREFP1 = 1, ADREFP0 = 0 Note 1 | | | 14.0 | 25.0 | μA |
| A/D converter reference voltage current | $I_{ADREF}$ Note 1, 8 | $V_{DD}$ = 3.0 V | | | 75.0 | | μA |
| Temperature sensor operating current | $I_{TMPS}$ Note 1 | $V_{DD}$ = 3.0 V | | | 75.0 | | μA |
| LVD operating current | $I_{LVD}$ Note 1, 10 | | | | 0.08 | | μA |
| BGO operating current | $I_{BGO}$ Note 1, 11 | | | | 2.5 | 12.2 | mA |
| Selfprogramming operating current | $I_{FSP}$ Note 1, 12 | | | | 2.5 | 12.2 | mA |
| SNOOZE operating current | $I_{SNOZ}$ | A/D converter operation ($AV_{DD}$ = 3.0 V) | The mode is performed Note 1, 13 | | 0.50 | 0.60 | mA |
| | | | During A/D conversion Note 1 | | 0.60 | 0.75 | mA |
| | | | During A/D conversion Note 6 | | 420 | 720 | μA |
| | | CSI/UART operation Note 1 | | | 0.70 | 0.84 | mA |

(**Notes** and **Remarks** are listed on the next page.)

<R> **(4) Communication between devices at same potential (CSI mode)**
**(slave mode, SCKp ... External clock input) (1/2)**

($T_A$ = –40 to +85°C, 1.6 V ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = 0 V) (1/2)

| Parameter | Symbol | Conditions | | HS Note 1 | | LS Note 2 | | LV Note 3 | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN. | MAX. | MIN. | MAX. | MIN. | MAX. | |
| SCKp cycle time Note 4 | $t_{KCY2}$ | 4.0V ≤ $V_{DD}$ ≤ 5.5V | 20MHz < $f_{MCK}$ | 8/$f_{MCK}$ | | – | | – | | ns |
| | | | $f_{MCK}$ ≤ 20MHz | 6/$f_{MCK}$ | | 6/$f_{MCK}$ | | 6/$f_{MCK}$ | | ns |
| | | 2.7V ≤ $V_{DD}$ ≤ 5.5V | 16MHz < $f_{MCK}$ | 8/$f_{MCK}$ | | – | | – | | ns |
| | | | $f_{MCK}$ ≤ 16MHz | 6/$f_{MCK}$ | | 6/$f_{MCK}$ | | 6/$f_{MCK}$ | | ns |
| | | 2.4 V ≤ $V_{DD}$ ≤ 5.5 V | | 6/$f_{MCK}$ and 500ns | | 6/$f_{MCK}$ and 500ns | | 6/$f_{MCK}$ and 500ns | | ns |
| | | 1.8 V ≤ $V_{DD}$ ≤ 5.5 V | | 6/$f_{MCK}$ and 750ns | | 6/$f_{MCK}$ and 750ns | | 6/$f_{MCK}$ and 750ns | | ns |
| | | 1.7 V ≤ $V_{DD}$ ≤ 5.5 V | | 6/$f_{MCK}$ and 1500ns | | 6/$f_{MCK}$ and 1500ns | | 6/$f_{MCK}$ and 1500ns | | ns |
| | | 1.6 V ≤ $V_{DD}$ ≤ 5.5 V | | – | | 6/$f_{MCK}$ and 1500ns | | 6/$f_{MCK}$ and 1500ns | | ns |
| SCKp high-level width low-level width | $t_{KH2}$, $t_{KL2}$ | 4.0 V ≤ $V_{DD}$ ≤ 5.5 V | | $t_{KCY2}$/2 -7 | | $t_{KCY2}$/2 -7 | | $t_{KCY2}$/2 -7 | | ns |
| | | 2.7 V ≤ $V_{DD}$ ≤ 5.5 V | | $t_{KCY2}$/2 -8 | | $t_{KCY2}$/2 -8 | | $t_{KCY2}$/2 -8 | | ns |
| | | 1.8 V ≤ $V_{DD}$ ≤ 5.5 V | | $t_{KCY2}$/2 -18 | | $t_{KCY2}$/2 -18 | | $t_{KCY2}$/2 -18 | | ns |
| | | 1.7 V ≤ $V_{DD}$ ≤ 5.5 V | | $t_{KCY2}$/2 -66 | | $t_{KCY2}$/2 -66 | | $t_{KCY2}$/2 -66 | | ns |
| | | 1.6 V ≤ $V_{DD}$ ≤ 5.5 V | | – | | $t_{KCY2}$/2 -66 | | $t_{KCY2}$/2 -66 | | ns |

**Notes 1.** HS is condition of HS (high-speed main) mode.

**2.** LS is condition of LS (low-speed main) mode.

**3.** LV is condition of LV (low-voltage main) mode.

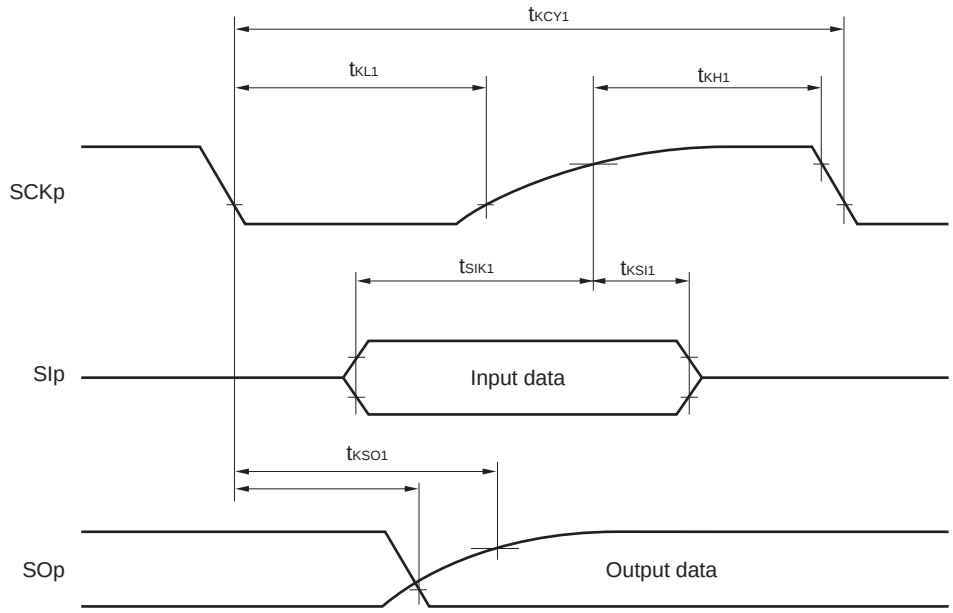
**4.** Transfer rate in the SNOOZE mode: MAX. 1 Mbps

**Caution Select the normal input buffer for the SIp pin and SCKp pin and the normal output mode for the SOp pin by using port input mode register g (PIMg) and port output mode register g (POMg).**

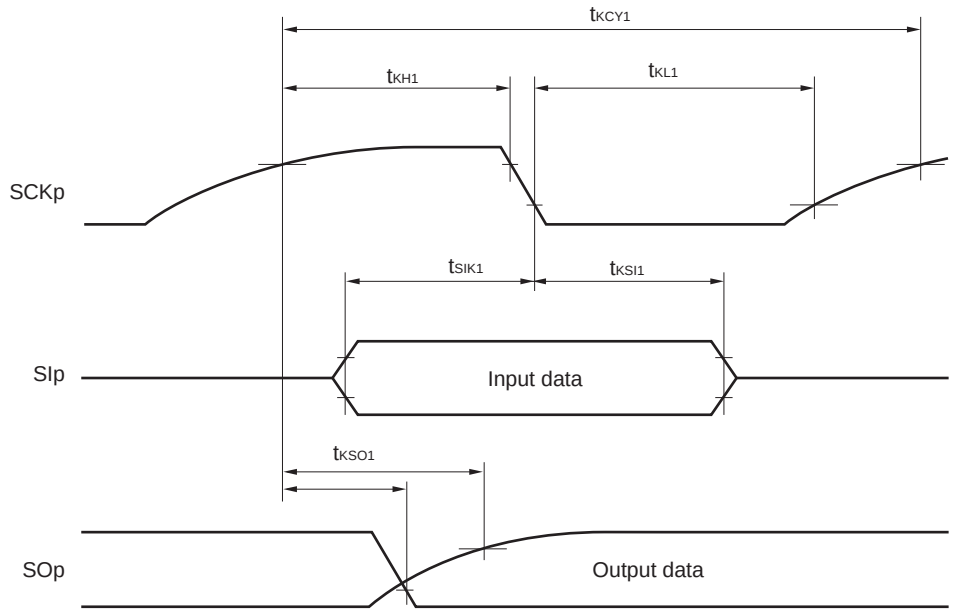
**Remarks 1.** p: CSI number (p = 00, 10, 20, 21), m: Unit number (m = 0, 1), n: Channel number (n = 0 to 2), g: PIM and POM numbers (g = 0, 1)

**2.** $f_{MCK}$: Serial array unit operating clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn).
m: Unit number, n: Channel number (mn = 00 to 03, 10, 11))

**CSI mode serial transfer timing: master mode (during communication between devices at different potential)**
**(when DAPmn = 0 and CKPmn = 0 or DAPmn = 1 and CKPmn = 1)**



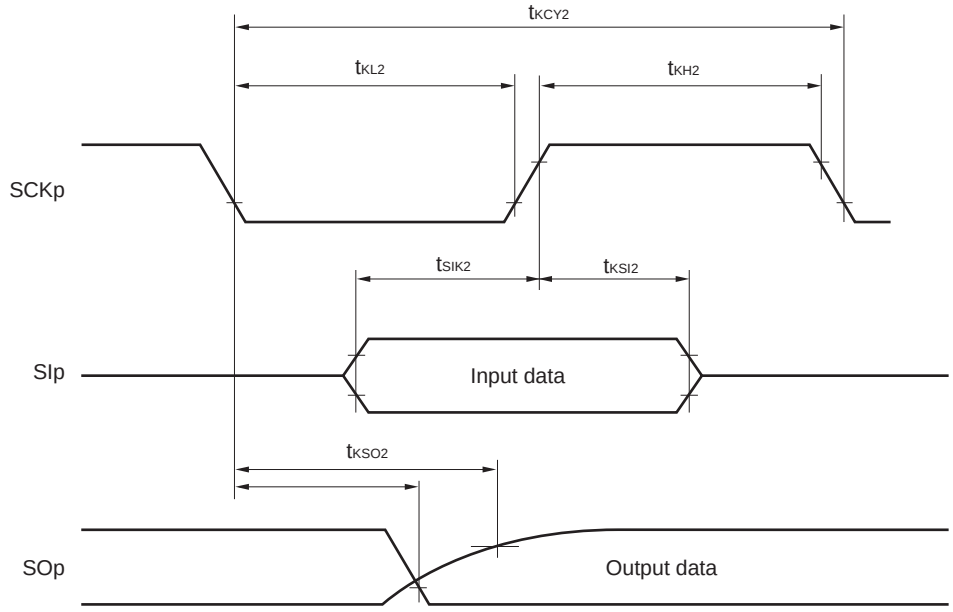

**CSI mode serial transfer timing: master mode (during communication between devices at different potential)**
**(when DAPmn = 0 and CKPmn = 1 or DAPmn = 1 and CKPmn = 0)**



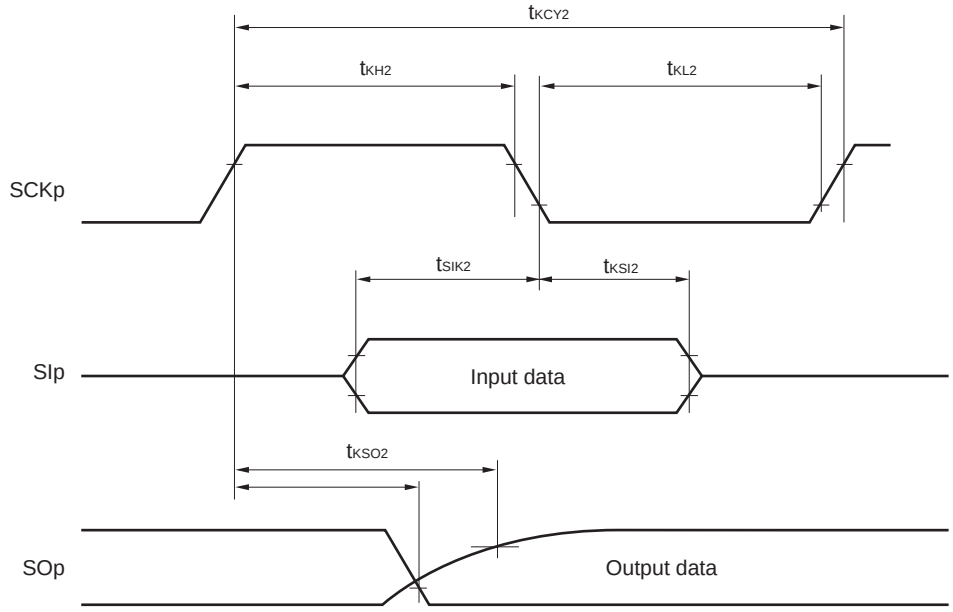

**Remarks 1.** p: CSI number (p = 00, 10, 20), m: Unit number, n: Channel number (mn = 00, 10, 20), g: PIM and POM numbers (g = 0, 1)

**2.** CSI21 cannot communicate with a device at different potential. Use other CSI channels for communication between devices at different potential.

**CSI mode serial transfer timing: slave mode (during communication between devices at different potential)**
**(when DAPmn = 0 and CKPmn = 0 or DAPmn = 1 and CKPmn = 1)**




**CSI mode serial transfer timing: slave mode (during communication between devices at different potential)**
**(when DAPmn = 0 and CKPmn = 1 or DAPmn = 1 and CKPmn = 0)**




**Remarks 1.** p: CSI number (p = 00, 10, 20), m: Unit number, n: Channel number (mn = 00, 10, 20),
g: PIM and POM numbers (g = 0, 1)

**2.** CSI21 cannot communicate with a device at different potential. Use other CSI channels for communication between devices at different potential.

### <R> 5. 2. 8 Dedicated flash memory programmer communication (UART)

($T_A$ = –40 to +85°C, 1.8 V ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = 0 V)

| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|
| Transfer rate | | When programming for flash memory | 115.2 k | | 1 M | bps |

(-40°C ≤ $T_A$ ≤ 85°C, $AV_{DD1}$ = $AV_{DD2}$ = $AV_{DD3}$ = $DV_{DD}$ = 5.0 V, VREFIN1 = VREFIN2 = VREFIN3 = 1.7 V, AMP1OF = AMP2OF = AMP3OF = 1, DAC1OF = DAC2OF = DAC3OF = 0, inverting amplifier) (1/2)

| Parameter | Symbol | Conditions | Ratings | | | Unit |
|---|---|---|---|---|---|---|
| | | | MIN | TYP | MAX | |
| Current consumption Note | Icc00 | CC1, CC0 = 0, 0 | – | 330 | 720 | μA |
| | Icc01 | CC1, CC0 = 0, 1 | – | 175 | 390 | μA |
| | Icc10 | CC1, CC0 = 1, 0 | – | 125 | 275 | μA |
| | Icc11 | CC1, CC0 = 1, 1 | – | 55 | 120 | μA |
| Input voltage | VINL | | AGND1 - 0.1 | – | – | V |
| | VINH | | – | – | $AV_{DD1}$ - 1.5 | V |
| Output voltage | VOUTL | IOL = -200 μA | – | AGND1 + 0.02 | AGND1 + 0.06 | V |
| | VOUTH | IOH = 200 μA | $AV_{DD1}$ - 0.06 | $AV_{DD1}$ - 0.02 | – | V |
| Settling time | $t_{SET\_AMP00}$ | GCn = 00H (6 dB), CC1, CC0 = 0, 0, CL = 30 pF, output voltage = $1V_{PP}$, output convergence voltage $V_{PP}$ = 999 mV | – | – | 9 | μs |
| | $t_{SET\_AMP01}$ | GCn = 00H (6 dB), CC1, CC0 = 0, 1, CL = 30 pF, output voltage = $1V_{PP}$, output convergence voltage $V_{PP}$ = 999 mV | – | – | 18 | μs |
| | $t_{SET\_AMP10}$ | GCn = 00H (6 dB), CC1, CC0 = 1, 0, CL = 30 pF, output voltage = $1V_{PP}$, output convergence voltage $V_{PP}$ = 999 mV | – | – | 28 | μs |
| | $t_{SET\_AMP11}$ | GCn = 00H (6 dB), CC1, CC0 = 1, 1, CL = 30 pF, output voltage = $1V_{PP}$, output convergence voltage $V_{PP}$ = 999 mV | – | – | 71 | μs |
| Gain bandwidth | GBW00 | CL = 30 pF,CC1, CC0 = 0, 0 GCn = 11H (40 dB) | – | 1.5 | | MHz |
| | GBW01 | CL = 30 pF,CC1, CC0 = 0, 1 GCn = 11H (40 dB) | – | 0.9 | | MHz |
| | GBW10 | CL = 30 pF,CC1, CC0 = 1, 0 GCn = 11H (40 dB) | – | 0.67 | | MHz |
| | GBW11 | CL = 30 pF,CC1, CC0 = 1, 1 GCn = 11H (40 dB) | – | 0.22 | | MHz |
| Equivalent input noise | En00 | CC1, CC0 = 0, 0 f = 1 kHz, GCn = 11H (40 dB) | – | 63 | – | nV/√ Hz |
| | En01 | CC1, CC0 = 0, 1 f = 1 kHz, GCn = 11H (40 dB) | – | 85 | – | nV/√ Hz |
| | En10 | CC1, CC0 = 1, 0 f = 1 kHz, GCn = 11H (40 dB) | – | 105 | – | nV/√ Hz |
| | En11 | CC1, CC0 = 1, 1 f = 1 kHz, GCn = 11H (40 dB) | – | 150 | – | nV/√ Hz |

**Note** These are the values for one channel of configurable amplifier.

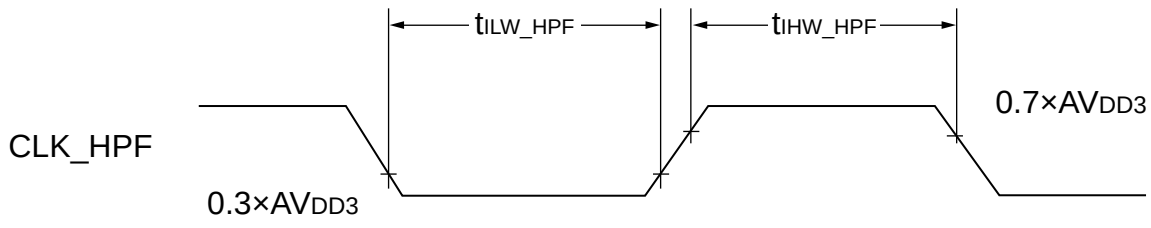
**Remark** n = 1 to 3

### 5. 3. 3. 5 High-pass filter characteristics

($-40°C \le T_A \le 85°C$, $AV_{DD1} = AV_{DD2} = AV_{DD3} = AV_{DD4} = DV_{DD} = 5.0$ V, HPFOF = 1)

| Parameter | Symbol | Conditions | Ratings | | | Unit |
|---|---|---|---|---|---|---|
| | | | MIN. | TYP. | MAX. | |
| Current consumption | IccA | | – | 800 | 1800 | μA |
| Input voltage | $V_{ILHPF}$ | | AGND4 +0.2 | – | – | V |
| | $V_{IHHPF}$ | | – | – | $AV_{DD3}$ - 1.5 | V |
| <R> Output voltage | $V_{OLHPF}$ | IOL = –200 μA | – | AGND4 +0.22 | AGND4 +0.25 | V |
| | $V_{OHHPF}$ | IOH = 200 μA | $AV_{DD3}$ -1.55 | $AV_{DD3}$ -1.52 | – | V |
| Cutoff frequency | fc1 | $f_{CLK\_HPF}$ = 2 kHz | – | 8 | – | Hz |
| | fc2 | $f_{CLK\_HPF}$ = 200 kHz | – | 800 | – | Hz |
| CLK_HPF low-level input voltage | $V_{ILCLK\_HPF}$ | | | | $0.3 \times AV_{DD3}$ | V |
| CLK_HPF high-level input voltage | $V_{IHCLK\_HPF}$ | | $0.7 \times AV_{DD3}$ | | | V |
| CLK_HPF Input frequency | $f_{CLK\_HPF}$ | | 2 | – | 200 | kHz |
| CLK_HPF Input low-level-width Input high-level-width | $t_{ILW\_HPF}$ $t_{IHW\_HPF}$ | | 200 | – | – | ns |

**Clock Timing**



RL78/G1E

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