Renesas Electronics America Inc - R5F10FMEAFB#YK1 Datasheet

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	RL78
Core Size	16-Bit
Speed	32MHz
Connectivity	CSI, I²C, LINbus, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	26
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	1.6V ~ 5.5V
Data Converters	A/D 17x8/12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	80-LQFP
Supplier Device Package	80-LFQFP (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f10fmeafb-yk1

CHAPTER 1 OUTLINE

<R> 1. 1 Features

The RL78/G1E is a multi-chip package (MCP) device that integrates a chip of an analog block and a chip of 16-bit microcontroller block in a single package. The chip of analog block features a range of front-end analog circuits for small sensor signal processing such as a configurable gain amplifier, gain adjustment amplifier, filter circuit, D/A converter, and temperature sensor. The chip of 16-bit microcontroller block corresponds to the RL78/G1A (64-pin products).

1. 1. 1 Microcontroller block

Low power consumption technology by standby function

- HALT mode
- STOP mode
- SNOOZE mode

RL78 CPU core

- CISC architecture with 3-stage pipeline
- Minimum instruction execution time: Can be changed from 0.03125 μs (32 MHz operation with high-speed on-chip oscillator) to 0.05 μs (20 MHz operation with high-speed system clock)
- Address space: 1 MB
- General-purpose registers: (8-bit register × 8) × 4 banks
- On-chip RAM: 2 to 4 KB

Code flash memory

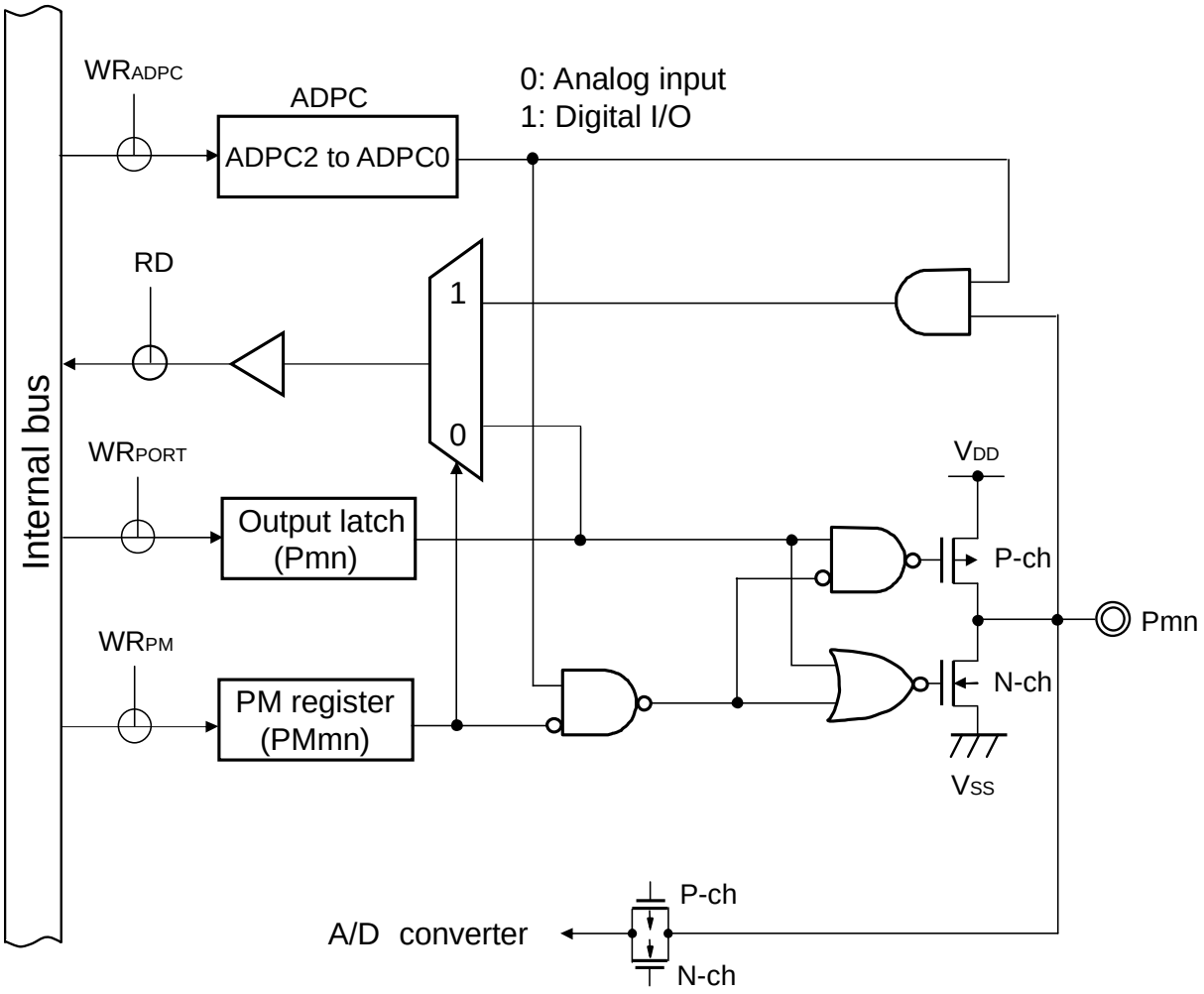
- Code flash memory: 32 to 64 KB
- Block size: 1 KB
- Prohibition of block erase and rewriting (security function)
- On-chip debug function
- Self-programming (with boot swap function/flash shield window function)

Data flash memory

- Data flash memory: 4 KB
- Back ground operation (BGO): Instructions can be executed from the program memory while rewriting the data flash memory.
- Number of rewrites: 1,000,000 times (TYP.)
- Voltage of rewrites: V_{DD} = 1.8 to 5.5 V

<R>

Figure 2-5. Pin Block Diagram for Pin Type 4-3-1



2. 5. 10 AV_{DD}, AV_{SS}, V_{DD}, V_{SS}

(a) AV_{DD}

This is the A/D converter reference voltage input pin and the positive power supply pin of P20 to P24, and A/D converter.

(b) AV_{SS}

This is the A/D converter ground potential pin. Even when the A/D converter is not used, always use this pin with the same potential as the V_{SS} pin.

(c) V_{DD}

This is the positive power supply pin.

(d) V_{SS}

This is the ground potential pin.

Remark Use bypass capacitors (about 0.1 μF) as noise and latch up countermeasures with relatively thick wires at the shortest distance to V_{DD} to V_{SS} line.

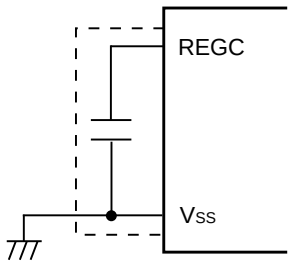
2. 5. 11 $\overline{\text{RESET}}$

This is the active-low system reset input pin for the functions of microcontroller block. When the external reset pin is not used, connect this pin directly or via a resistor to V_{DD}. When the external reset pin is used, design the circuit based on V_{DD}. For details of the functions, see **3. 5. 5 Clock generator operation, 3. 19 Reset Function, 3. 20 Power-On-Reset Circuit**.

2. 5. 12 REGC

This is the pin for connecting regulator output stabilization capacitance for internal operation. Connect this pin to V_{SS} via a capacitor (0.47 to 1 μF).

Also, use a capacitor with good characteristics, since it is used to stabilize internal voltage.



Caution Keep the wiring length as short as possible for the broken-line part in the above figure.

Table 3-1. List of Differences in Special Function Registers (SFRs) (3/4)

Address	RL78/G1E (64-pin products)		RL78/G1A (64-pin products)	
	SFRs Name	Symbol	SFRs Name	Symbol
FFF90H	Same as RL78/G1A (64-pin products)	ITMC	Interval timer control register	ITMC
FFF91H				
FFF92H			Second count register	SEC
FFF93H			Minute count register	MIN
FFF94H			Hour count register	HOUR
FFF95H			Week count register	WEEK
FFF96H			Day count register	DAY
FFF97H			Month count register	MONTH
FFF98H			Year count register	YEAR
FFF99H			Watch error correction register	SUBCUD
FFF9AH			Alarm minute register	ALARMWM
FFF9BH			Alarm hour register	ALARMWH
FFF9CH			Alarm week register	ALARMWW
FFF9DH			Real-time clock control register 0	RTCC0
FFF9EH			Real-time clock control register 1	RTCC1
FFFA0H	Clock operation mode control register Note	CMC	Clock operation mode control register	CMC
FFFA1H	Clock operation status control register Note	CSC	Clock operation status control register	CSC
FFFA2H	Same as RL78/G1A (64-pin products)	OSTC	Oscillation stabilization time counter status register	OSTC
FFFA3H	Same as RL78/G1A (64-pin products)	OSTS	Oscillation stabilization time select register	OSTS
FFFA4H	System clock control register Note	CKC	System clock control register	CKC
FFFA5H			Clock output select register 0	CKS0
FFFA6H			Clock output select register 1	CKS1
FFFA8H	Same as RL78/G1A (64-pin products)	RESF	Reset control flag register	RESF
FFFA9H	Same as RL78/G1A (64-pin products)	LVIM	Voltage detection register	LVIM
FFFAAH	Same as RL78/G1A (64-pin products)	LVIS	Voltage detection level register	LVIS
FFFABH	Same as RL78/G1A (64-pin products)	WDTE	Watchdog timer enable register	WDTE
FFFACH	Same as RL78/G1A (64-pin products)	CRCIN	CRC input register	CRCIN

Note The bit setting is different from that of RL78/G1A (64-pin products).

Caution Do not write data to the registers which is in the row with painted gray.

Table 3-4. List of Differences in Expanded Special Function Registers (2nd SFRs) (4/6)

Address	RL78/G1E (80-pin products)			RL78/G1A (64-pin products)		
	2nd SFRs Name	Symbol		2nd SFRs Name	Symbol	
F0148H	Same as RL78/G1A (64-pin products)	SIR10L	SIR10	Serial flag clear trigger register 10	SIR10L	SIR10
F0149H		—			—	
F014AH	Same as RL78/G1A (64-pin products)	SIR11L	SIR11	Serial flag clear trigger register 11	SIR11L	SIR11
F014BH		—			—	
F0150H	Same as RL78/G1A (64-pin products)	SMR10		Serial mode register 10	SMR10	
F0151H						
F0152H	Serial mode register 11 Note	SMR11		Serial mode register 11	SMR11	
F0153H						
F0158H	Same as RL78/G1A (64-pin products)	SCR10		Serial communication operation setting register 10	SCR10	
F0159H						
F015AH	Serial communication operation setting register 11 Note	SCR11		Serial communication operation setting register 11	SCR11	
F015BH						
F0160H	Same as RL78/G1A (64-pin products)	SE1L	SE1	Serial channel enable status register 1	SE1L	SE1
F0161H		—			—	
F0162H	Same as RL78/G1A (64-pin products)	SS1L	SS1	Serial channel start register 1	SS1L	SS1
F0163H		—			—	
F0164H	Same as RL78/G1A (64-pin products)	ST1L	ST1	Serial channel stop register 1	ST1L	ST1
F0165H		—			—	
F0166H	Same as RL78/G1A (64-pin products)	SPS1L	SPS1	Serial clock select register 1	SPS1L	SPS1
F0167H		—			—	
F0168H	Same as RL78/G1A (64-pin products)	SO1		Serial output register 1	SO1	
F0169H						
F016AH	Same as RL78/G1A (64-pin products)	SOE1L	SOE1	Serial output enable register 1	SOE1L	SOE1
F016BH		—			—	
F0174H	Same as RL78/G1A (64-pin products)	SOL1L	SOL1	Serial output level register 1	SOL1L	SOL1
F0175H		—			—	

Note The bit setting is different from that of RL78/G1A (64-pin products).

3. 5. 4 System clock oscillator

See **5. 4 System Clock Oscillator** in **RL78/G1A Hardware User's Manual (R01UH0305E)**.

3. 5. 5 Clock generator operation

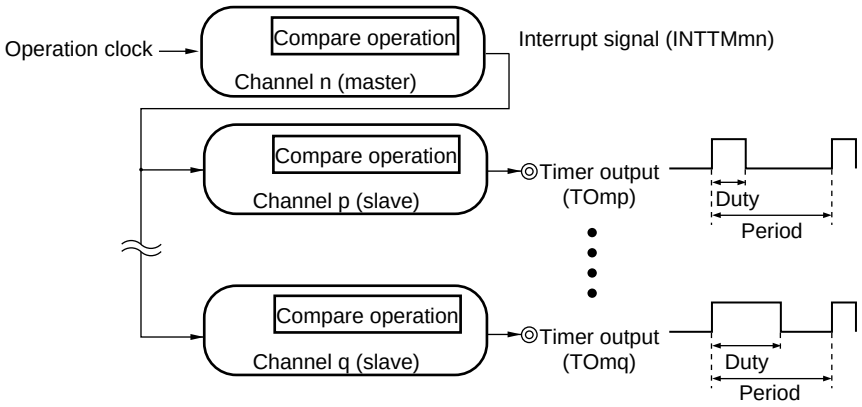
See **5. 5 Clock Generator Operation** in **RL78/G1A Hardware User's Manual (R01UH0305E)**.

3. 5. 6 Controlling clock

See **5. 6 Controlling Clock** in **RL78/G1A Hardware User's Manual (R01UH0305E)**.

<3> Multiple PWM (Pulse Width Modulation) output

By extending the PWM function and using one master channel and two or more slave channels, up to seven types of PWM signals that have a specific period and a specified duty factor can be generated.



Caution For details about the rules of simultaneous channel operation function, see 3. 6. 4 Basic rules of timer array unit.

Remark m: Unit number (m = 0), n: Channel number (n = 0 to 7 (however, timer input pin (TImn) , timer output pin (TOmn) : n = 0, 4, 7)), p, q: Slave channel number (4, 7)

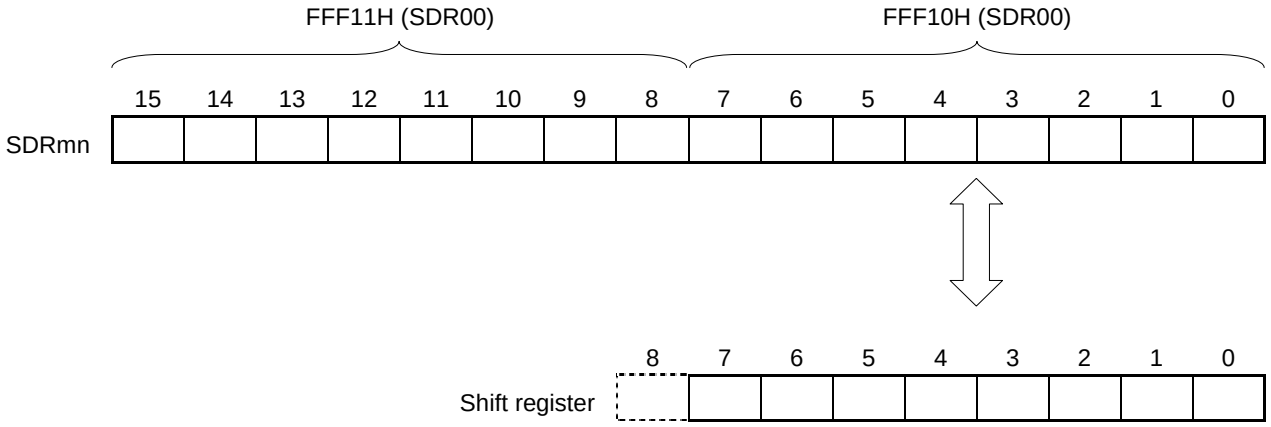
3. 6. 1. 3 8-bit timer operation function (channels 1 and 3 only)

The 8-bit timer operation function makes it possible to use a 16-bit timer channel in a configuration consisting of two 8-bit timer channels. This function can only be used for channels 1 and 3.

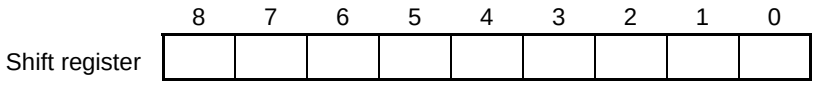
Caution There are several rules for using 8-bit timer operation function. For details, see 3. 6. 4 Basic rules of timer array unit.

<R> **Figure 3-11. Format of Serial Data Register mn (SDRmn) (mn = 00, 01, 02, 03, 10, 11)**

Address: FFF10H, FFF11H (SDR00), FFF12H, FFF13H (SDR01) After reset: 0000H R/W
FFF44H, FFF45H (SDR02), FFF46H, FFF47H (SDR03),
FFF48H, FFF49H (SDR10)Note, FFF4AH, FFF4BH (SDR11)Note



- For 9-bit data communication with UART0 (mn = 00, 01)



Caution For 9-bit data communication, be sure to clear bit 8 of the SDRmn register to "0".

Table 3-14. Flags Corresponding to Interrupt Request Sources (4/4)

Interrupt Source	Interrupt Request Flag	Register	Interrupt Mask Flag	Register	Priority Specification Flag	Register	RL78/G1E 64-pin	RL78/G1E 80-pin
INTTM05	TMIF05	IF2L	TMMK05	MK2L	TMPR005, TMPR105	PR02L, PR12L	√	√
INTTM06	TMIF06		TMMK06		TMPR006, TMPR106		√	√
INTTM07	TMIF07		TMMK07		TMPR007, TMPR107		√	√
INTP6	PIF6		PMK6		PPR06, PPR16		–	√
INTP7	PIF7		PMK7		PPR07, PPR17		–	–
INTP8	PIF8		PMK8		PPR08, PPR18		–	–
INTP9	PIF9		PMK9		PPR09, PPR19		–	–
INTP10	PIF10		PMK10		PPR010, PPR110		–	–
INTP11	PIF11	IF2H	PMK11	MK2H	PPR011, PPR111	PR02H, PR12H	–	–
INTMD	MDIF		MDMK		MDPR0, MDPR1		√	√
INTFL	FLIF		FLMK		FLPR0, FLPR1		√	√

The bit settings which are different from that of RL78/G1A (64-pin products) are shown on the next page. For details of each register, see **16. 3 Registers Controlling Interrupt Functions** in **RL78/G1A Hardware User's Manual (R01UH0305E)**.

<R> **3. 25. 2 Serial programming using external device (that Incorporates UART)**

See **25. 2 Serial Programming Using External Device (that Incorporates UART)** in **RL78/G1A Hardware User's Manual (R01UH0305E)**.

3. 25. 3 Connection of pins on board

See **25. 3 Connection of Pins on Board** in **RL78/G1A Hardware User's Manual (R01UH0305E)**.

<R> **3. 25. 4 Serial programming method**

See **25. 4 Serial Programming Method** in **RL78/G1A Hardware User's Manual (R01UH0305E)**.

<R> **3. 25. 5 Processing time for each command when PG-FP5 Is in use (Reference value)**

See **25. 5 Processing Time for Each Command When PG-FP5 Is in Use (Reference Value)** in **RL78/G1A Hardware User's Manual (R01UH0305E)**.

<R> **3. 25. 6 Self-programming**

See **25. 6 Self-Programming** in **RL78/G1A Hardware User's Manual (R01UH0305E)**.

<R> **3. 25. 7 Security Settings**

See **25. 7 Security Settings** in **RL78/G1A Hardware User's Manual (R01UH0305E)**.

<R> **3. 25. 8 Data flash**

See **25. 8 Data Flash** in **RL78/G1A Hardware User's Manual (R01UH0305E)**.

4. 4 Low-Pass Filter

The RL78/G1E (64-pin products, 80-pin products) has one on-chip switched-capacitor low-pass filter channel.

4. 4. 1 Overview of low-pass filter features

The features of low-pass filter are described below.

- Butterworth characteristics (Q value = 0.702)
- Cutoff frequency (f_C) range: 9 Hz to 4.5 kHz
- External input clock frequency (f_{CLK_LPF}) range: $f_C \times 2 / 0.009$ = 2 kHz to 1 MHz
<R> - Includes a power-off function.

And also, the DAC4_OUT output signals can be used as the reference voltage for low-pass filter.

If D/A converter is powered off, the external reference voltage is to be input to DAC4_OUT/VREFIN4 pin.

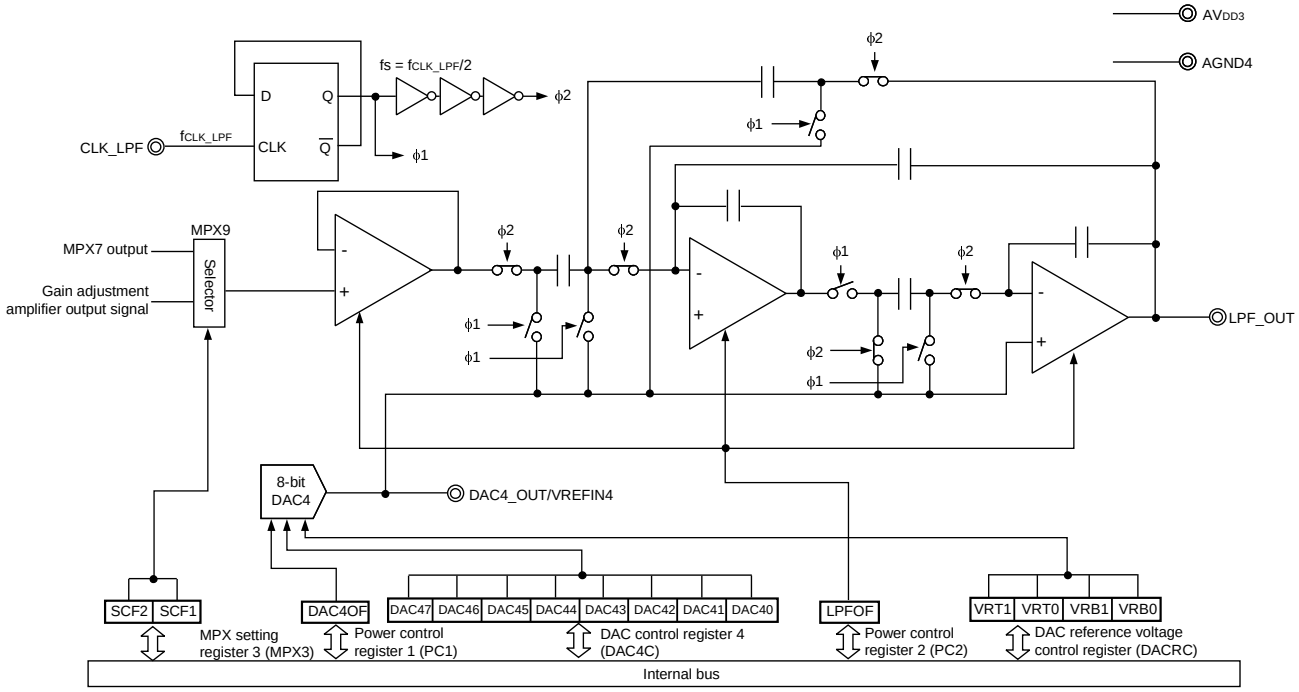
For details about use of D/A converter, see **4. 3 D/A Converter**.

Remarks 1. The internal control clock (f_S) of the low-pass filter has a duty of 50%, so the external input clock is divided by two at the internal D flip-flop before being used for the low-pass filter. If the internal control clock frequency (f_S) is 100 kHz, therefore, input a 200 kHz clock signal to the CLK_LPF pin.

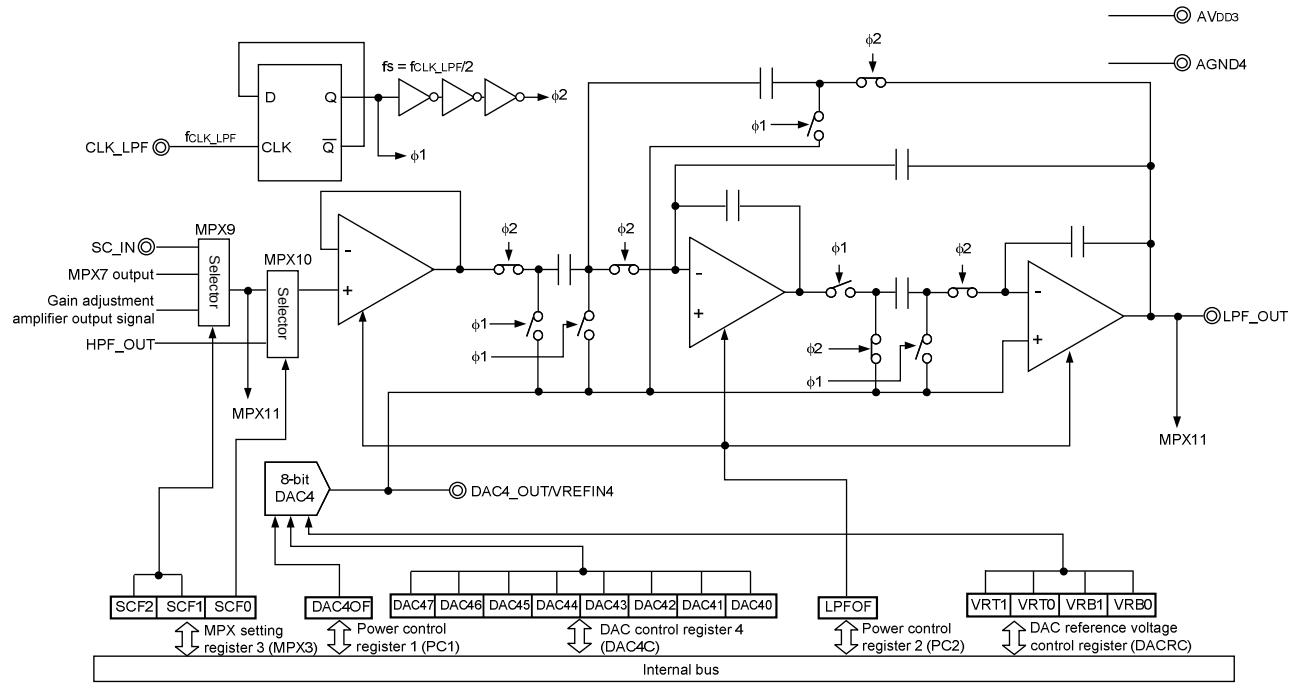
2. The phase of the signal input to the low-pass filter inverts after passing the low-pass filter.

4. 4. 2 Block diagram

- **64-pin products**



- **80-pin products**



4. 9 SPI

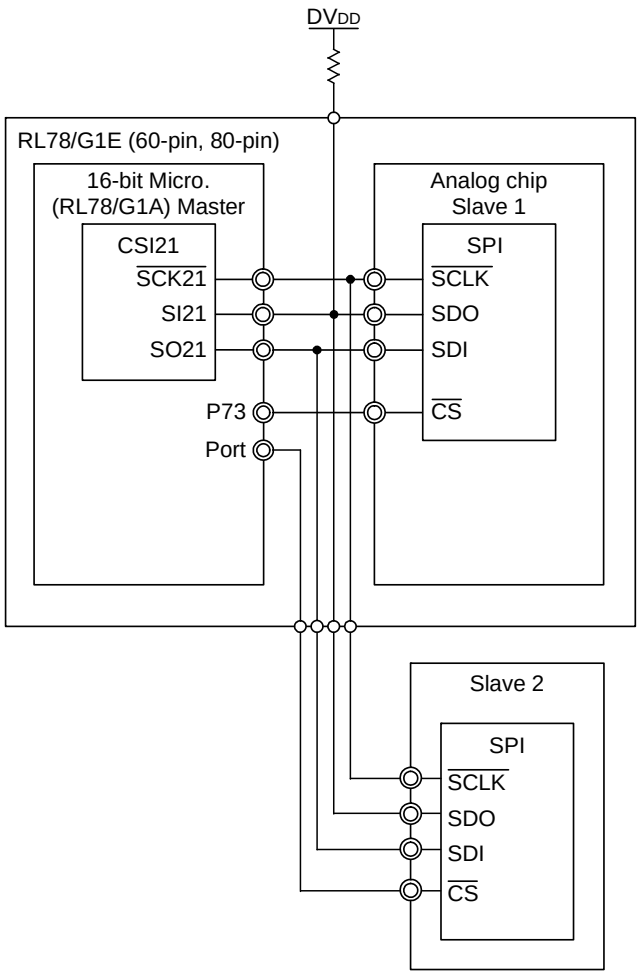
4. 9. 1 Overview of SPI features

The SPI interface is used to allow control from external devices by using clocked communication via four lines: a serial clock line ($\overline{\text{SCLK}}$), two serial data lines (SDI and SDO), and a chip select input line ($\overline{\text{CS}}$).

Data transmission/reception:

- 16-bit data unit
- MSB first

Figure 4-4. SPI Configuration Example

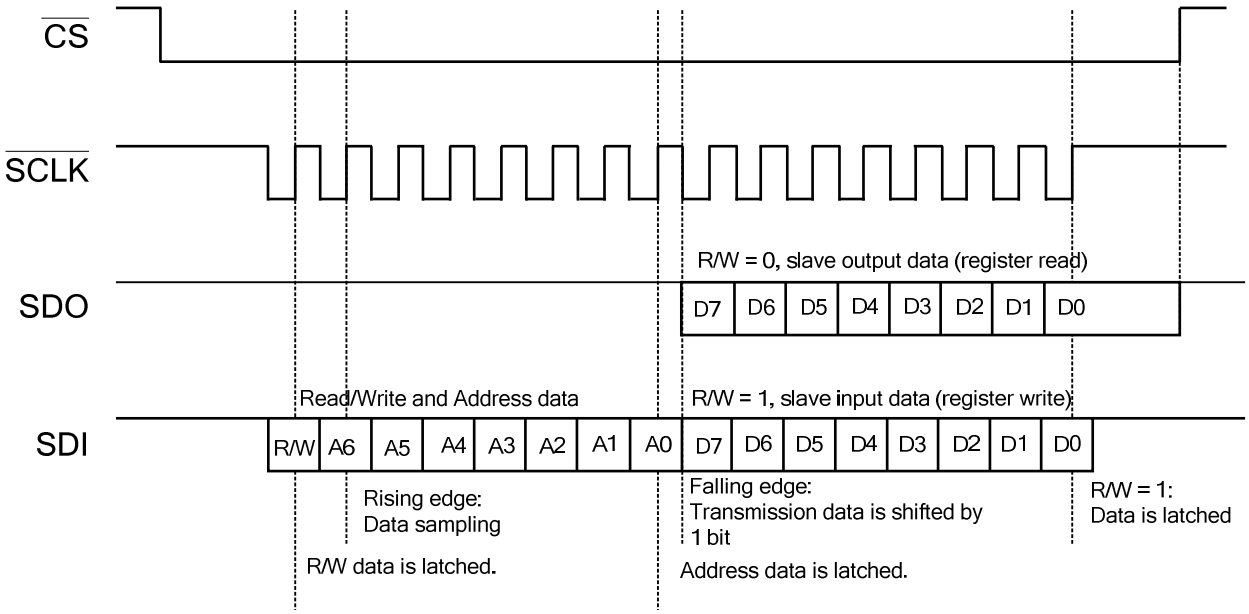


Caution After turning on DV_{DD}, be sure to generate external reset by inputting a reset signal to $\overline{\text{ARESET}}$ pin before starting SPI communication. For details, see 4.10 Analog Reset.

4. 9. 2 SPI communication

The SPI transmits and receives data in 16-bit units. Data can be transmitted and received when $\overline{CS}$ is low. Data is transmitted one bit at a time in synchronization with the falling edge of the serial clock, and is received one bit at a time in synchronization with the rising edge of the serial clock. When the R/W bit is 1, data is written to the SPI control register in accordance with the address/data setting after the 16th rising edge of $\overline{SCLK}$ has been detected following the fall of $\overline{CS}$, and the operation specified by the data is executed. When the R/W bit is 0, the data is output from the register in accordance with the address/data setting in synchronization with the 9th and later falling edges of $\overline{SCLK}$ following the fall of $\overline{CS}$.

Figure 4-5. SPI Communication Timing



5. 2 Electrical Specifications of Microcontroller Block

5. 2. 1 Oscillator characteristics

5. 2. 1. 1 X1 oscillator characteristics

(T_A = –40 to +85°C, 1.6 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

<R>

Parameter	Resonator	Conditions	MIN.	TYP.	MAX.	Unit
X1 clock oscillation frequency (f_X)Note	Ceramic resonator / Crystal resonator	2.7 V ≤ V_{DD} ≤ 5.5 V	1.0		20.0	MHz
		2.4 V ≤ V_{DD} < 2.7 V	1.0		16.0	
		1.8 V ≤ V_{DD} < 2.4 V	1.0		8.0	
		1.6 V ≤ V_{DD} < 1.8 V	1.0		4.0	

<R> **Note** Indicates only oscillator characteristics. Refer to AC Characteristics for instruction execution time. Also, be sure to apply to the resonator manufacturer for evaluation on the actual circuit so as to confirm the oscillation characteristics.

Caution Since the CPU is started by the high-speed on-chip oscillator clock after a reset release, check the X1 clock oscillation stabilization time using the oscillation stabilization time counter status register (OSTC) by the user. Determine the oscillation stabilization time of the OSTC register and the oscillation stabilization time select register (OSTS) after sufficiently evaluating the oscillation stabilization time with the resonator to be used.

<R> **Remark** When using the X1 oscillator, see **3. 5. 4 System clock oscillator**.

5. 2. 2. 2 Supply current characteristics

(T_A = –40 to +85°C, 1.6 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V) (1/3)

Parameter	Symbol	Conditions					MIN.	TYP.	MAX.	Unit
Supply current Note 1	I_{DD1}	Operating mode	HS(High-speed main) mode Note 4	f_{IH} = 32 MHz Note 3	Basic operation	V_{DD} = 5.0 V		2.1		mA
						V_{DD} = 3.0 V		2.1		
					Normal operation	V_{DD} = 5.0 V		4.6	7.0	mA
						V_{DD} = 3.0 V		4.6	7.0	
				f_{IH} = 24 MHz Note 3	Normal operation	V_{DD} = 5.0 V		3.7	5.5	mA
						V_{DD} = 3.0 V		3.7	5.5	
				f_{IH} = 16 MHz Note 3	Normal operation	V_{DD} = 5.0 V		2.7	4.0	mA
						V_{DD} = 3.0 V		2.7	4.0	
			LS (Low-speed main) mode Note 4	f_{IH} = 8 MHz Note 3	Normal operation	V_{DD} = 3.0 V		1.2	1.8	mA
						V_{DD} = 2.0 V		1.2	1.8	
			LV (Low-voltage main) mode Note 4	f_{IH} = 4 MHz Note 3	Normal operation	V_{DD} = 3.0 V		1.2	1.7	mA
						V_{DD} = 2.0 V		1.2	1.7	
			HS (High-speed main) mode Note 4	f_{MX} = 20 MHz Note 2, V_{DD} = 5.0 V	Normal operation	Square wave input		3.0	4.6	mA
						Resonator connection		3.2	4.8	
				f_{MX} = 20 MHz Note 2, V_{DD} = 3.0 V	Normal operation	Square wave input		3.0	4.6	
						Resonator connection		3.2	4.8	
				f_{MX} = 10 MHz Note 2, V_{DD} = 5.0 V	Normal operation	Square wave input		1.9	2.7	mA
						Resonator connection		1.9	2.7	
				f_{MX} = 10 MHz Note 2, V_{DD} = 3.0 V	Normal operation	Square wave input		1.9	2.7	
						Resonator connection		1.9	2.7	
			LS (Low-speed main) mode Note 4	f_{MX} = 8 MHz Note 2, V_{DD} = 3.0 V	Normal operation	Square wave input		1.1	1.7	mA
						Resonator connection		1.1	1.7	
				f_{MX} = 8 MHz Note 2, V_{DD} = 2.0 V	Normal operation	Square wave input		1.1	1.7	
						Resonator connection		1.1	1.7	

Notes 1. Total current flowing into V_{DD}, including the input leakage current flowing when the level of the input pin is fixed to V_{DD} or V_{SS}. The values below the MAX. column include the peripheral operation current. However, not including the current flowing into the A/D converter, LVD circuit, I/O port, on-chip pullup/pull-down resistors, and data flash rewriting.

2. When the high-speed on-chip oscillator is stopped.

3. When the high-speed system clock is stopped.

4. The relationship between the operation voltage range, CPU operating frequency, and operating mode is as below.

HS (High-speed main) mode: V_{DD} = 2.7 to 5.5 V @ 1 MHz to 32 MHz
V_{DD} = 2.4 to 5.5 V @ 1 MHz to 16 MHz

LS (Low-speed main) mode: V_{DD} = 1.8 to 5.5 V @ 1 MHz to 8 MHz

LV (Low-voltage main) mode: V_{DD} = 1.6 to 5.5 V @ 1 MHz to 4 MHz

Remarks 1. f_{MX}: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)

2. f_{IH}: High-speed on-chip oscillator clock frequency

<R> (5) When reference voltage (+) = AV_{DD} (ADREFP1 = 0, ADREFP0 = 0), reference voltage (–) = AV_{SS} (ADREFM = 0), target for conversion: ANI16 to ANI18, ANI20 to ANI26, ANI28, and ANI30 (ANI pins that use V_{DD} as their power source), interanal reference voltage, temperature sensor output voltage

(T_A = –40 to +85°C, 1.6 V ≤ V_{DD} ≤ 5.5 V, 1.6 V ≤ AV_{DD} ≤ 3.6 V, AV_{DD} ≤ V_{DD}, V_{SS} = 0 V, AV_{SS} = 0 V, reference voltage (+) = AV_{DD}, reference voltage (–) = AV_{SS} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Resolution	R_{ES}		2.4 V ≤ AV_{DD} ≤ 3.6 V	8		12	bit
			1.8 V ≤ AV_{DD} ≤ 3.6 V	8		10 Note 1	
			1.6 V ≤ AV_{DD} ≤ 3.6 V	8 Note 2			
Overall error Note 3	AINL	12-bit resolution	2.4 V ≤ AV_{DD} ≤ 3.6 V			±8.5	LSB
		10-bit resolution	1.8 V ≤ AV_{DD} ≤ 3.6 V			±6.0	
		8-bit resolution	1.6 V ≤ AV_{DD} ≤ 3.6 V			±3.5	
Conversion time	t_{CONV}	ADTYP = 0, 12-bit resolution	2.4 V ≤ AV_{DD} ≤ 3.6 V	4.125			μs
		ADTYP = 0, 10-bit resolution Note 1	1.8 V ≤ AV_{DD} ≤ 3.6 V	9.5			
		ADTYP = 0, 8-bit resolution Note 2	1.6 V ≤ AV_{DD} ≤ 3.6 V	57.5			
		ADTYP = 1, 8-bit resolution	2.4 V ≤ AV_{DD} ≤ 3.6 V	3.3125			
			1.8 V ≤ AV_{DD} ≤ 3.6 V	7.875			
			1.6 V ≤ AV_{DD} ≤ 3.6 V	54.25			
Zero-scale error Notes 3	EZS	12-bit resolution	2.4 V ≤ AV_{DD} ≤ 3.6 V			±8.0	LSB
		10-bit resolution	1.8 V ≤ AV_{DD} ≤ 3.6 V			±5.5	
		8-bit resolution	1.6 V ≤ AV_{DD} ≤ 3.6 V			±3.0	
Full-scale error Notes 3	EFS	12-bit resolution	2.4 V ≤ AV_{DD} ≤ 3.6 V			±8.0	LSB
		10-bit resolution	1.8 V ≤ AV_{DD} ≤ 3.6 V			±5.5	
		8-bit resolution	1.6 V ≤ AV_{DD} ≤ 3.6 V			±3.0	
Integral linearity error Note 3	ILE	12-bit resolution	2.4 V ≤ AV_{DD} ≤ 3.6 V			±3.5	LSB
		10-bit resolution	1.8 V ≤ AV_{DD} ≤ 3.6 V			±2.5	
		8-bit resolution	1.6 V ≤ AV_{DD} ≤ 3.6 V			±1.5	
Differential linearity error Note 3	DLE	12-bit resolution	2.4 V ≤ AV_{DD} ≤ 3.6 V			±2.5	LSB
		10-bit resolution	1.8 V ≤ AV_{DD} ≤ 3.6 V			±2.5	
		8-bit resolution	1.6 V ≤ AV_{DD} ≤ 3.6 V			±2.0	
Analog input voltage	V_{AIN}			0		AV_{DD} and V_{DD}	V
		Intenal reference voltage (2.4 V ≤ V_{DD} ≤ 5.5 V, HS (high-speed main) mode)		V_{BGR} Note 4			V
		Temperature sensor output voltage (2.4 V ≤ V_{DD} ≤ 5.5 V, HS (high-speed main) mode)		V_{TMPS25} Note 4			V

Notes 1. The lower 2 bits of the ADCR register cannot be used.

2. The lower 4 bits of the ADCR register cannot be used.

3. Excludes quantization error (±1/2 LSB).

4. Refer to **5. 2. 5. 2 Temperature sensor, internal reference voltage output characteristics**.

(-40°C ≤ T_A ≤ 85°C, AV_{DD1} = AV_{DD2} = AV_{DD3} = DV_{DD} = 5.0 V, VREFIN1 = VREFIN2 = VREFIN3 = 1.7 V, AMP1OF = AMP2OF = AMP3OF = 1, DAC1OF = DAC2OF = DAC3OF = 0, inverting amplifier) (1/2)

Parameter	Symbol	Conditions	Ratings			Unit
			MIN	TYP	MAX	
Current consumption Note	Icc00	CC1, CC0 = 0, 0	–	330	720	μA
	Icc01	CC1, CC0 = 0, 1	–	175	390	μA
	Icc10	CC1, CC0 = 1, 0	–	125	275	μA
	Icc11	CC1, CC0 = 1, 1	–	55	120	μA
Input voltage	VINL		AGND1 - 0.1	–	–	V
	VINH		–	–	AV_{DD1} - 1.5	V
Output voltage	VOUTL	IOL = -200 μA	–	AGND1 + 0.02	AGND1 + 0.06	V
	VOUTH	IOH = 200 μA	AV_{DD1} - 0.06	AV_{DD1} - 0.02	–	V
Settling time	t_{SET_AMP00}	GCn = 00H (6 dB), CC1, CC0 = 0, 0, CL = 30 pF, output voltage = $1V_{PP}$, output convergence voltage V_{PP} = 999 mV	–	–	9	μs
	t_{SET_AMP01}	GCn = 00H (6 dB), CC1, CC0 = 0, 1, CL = 30 pF, output voltage = $1V_{PP}$, output convergence voltage V_{PP} = 999 mV	–	–	18	μs
	t_{SET_AMP10}	GCn = 00H (6 dB), CC1, CC0 = 1, 0, CL = 30 pF, output voltage = $1V_{PP}$, output convergence voltage V_{PP} = 999 mV	–	–	28	μs
	t_{SET_AMP11}	GCn = 00H (6 dB), CC1, CC0 = 1, 1, CL = 30 pF, output voltage = $1V_{PP}$, output convergence voltage V_{PP} = 999 mV	–	–	71	μs
Gain bandwidth	GBW00	CL = 30 pF,CC1, CC0 = 0, 0 GCn = 11H (40 dB)	–	1.5		MHz
	GBW01	CL = 30 pF,CC1, CC0 = 0, 1 GCn = 11H (40 dB)	–	0.9		MHz
	GBW10	CL = 30 pF,CC1, CC0 = 1, 0 GCn = 11H (40 dB)	–	0.67		MHz
	GBW11	CL = 30 pF,CC1, CC0 = 1, 1 GCn = 11H (40 dB)	–	0.22		MHz
Equivalent input noise	En00	CC1, CC0 = 0, 0 f = 1 kHz, GCn = 11H (40 dB)	–	63	–	nV/√ Hz
	En01	CC1, CC0 = 0, 1 f = 1 kHz, GCn = 11H (40 dB)	–	85	–	nV/√ Hz
	En10	CC1, CC0 = 1, 0 f = 1 kHz, GCn = 11H (40 dB)	–	105	–	nV/√ Hz
	En11	CC1, CC0 = 1, 1 f = 1 kHz, GCn = 11H (40 dB)	–	150	–	nV/√ Hz

Note These are the values for one channel of configurable amplifier.

Remark n = 1 to 3

(2) 80-pin products

(–40°C ≤ T_A ≤ 85°C, AV_{DD1} = AV_{DD2} = AV_{DD3} = DV_{DD} = 5.0 V, VREFIN4 = 1.7 V, GAINOF = 1, DAC4OF = 0)

Parameter	Symbol	Conditions	Ratings			Unit
			MIN	TYP	MAX	
Current consumption	IccA		–	530	1,300	μA
Input voltage	VINL		AGND2 - 0.1	–	–	V
	VINH		–	–	AV_{DD1} - 0.05	V
Output voltage	VOUTL1	IOL = -100 μA, GAINAMP_OUT pin	–	AGND2 + 0.02	AGND2 + 0.05	V
	VOUTH1	IOH = 100 μA, GAINAMP_OUT pin	AV_{DD1} - 0.05	AV_{DD1} - 0.02	–	V
	VOUTL2	IOL = -100 μA, SYNCH_OUT pin	–	AGND2 + 0.03	AGND2 + 0.06	V
	VOUTH2	IOH = 100 μA, SYNCH_OUT pin	AV_{DD1} - 0.06	AV_{DD1} - 0.03	–	V
Gain bandwidth	GBW1	CLK_SYNCH = H, SYNCH_OUT pin CL = 30 pF, GC4 = 11H (40 dB)	–	1.38	–	MHz
	GBW2	CLK_SYNCH = L, SYNCH_OUT or GAINAMP_OUT pin CL = 30 pF, GC4 = 11H (40 dB)	–	0.86	–	MHz
Input conversion offset voltage	VOFF	GC4 = 00H (6 dB), T_A = 25°C, GAINAMP_IN = 2.5 V	-30	–	30	mV
Input conversion offset voltage temperature coefficient	VOTC1	CLK_SYNCH = H, SYNCH_OUT pin	–	±6	–	μV/°C
	VOTC2	CLK_SYNCH = L, GAINAMP_OUT pin	–	±18	–	μV/°C
Slew rate	SR	CL = 30 pF	–	0.9	–	V/μs
Equivalent input noise	En_Gain	f = 1 kHz, GC4 = 11H (40 dB) GAINAMP_OUT pin	–	700	–	nV/√ Hz
Power supply rejection ratio	PSRR1	CLK_SYNCH = H, SYNCH_OUT pin, f = 1 kHz, GC4 = 00H (6 dB)	–	60	–	dB
	PSRR2	CLK_SYNCH = L, SYNCH_OUT or GAINAMP_OUT pin, f = 1 kHz, GC4 = 00H (6 dB)	–	45	–	dB
Gain setting error	GAIN_Accu1	T_A = 25°C	-0.6	–	0.6	dB
	GAIN_Accu2	T_A = –40 to 85°C	-1.0	–	1.0	dB
CLK_SYNCH low-level input voltage	V_{ILCLK_SYNCH}				0.3 × AV_{DD1}	V
CLK_SYNCH high-level input voltage	V_{IHCLK_SYNCH}		0.7 × AV_{DD1}			V

APPENDIX A CHARACTERISTICS CURVE (T_A = 25°C, TYP.) (REFERENCE VALUE)

• Configurable amplifier