Renesas Electronics America Inc - R5F10FMEDFB#V0 Datasheet

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	RL78
Core Size	16-Bit
Speed	32MHz
Connectivity	CSI, I²C, LINbus, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	26
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	1.6V ~ 5.5V
Data Converters	A/D 17x8/12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	80-LQFP
Supplier Device Package	80-LFQFP (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f10fmedfb-v0

How to Use This Manual

Readers

This manual is intended for user engineers who wish to understand the functions of the RL78/G1E and design and develop application systems and programs for these devices.
The target products are as follows.

- 64-pin: R5F10FLx (x = C, D, E)
- 80-pin: R5F10FMx (x = C, D, E)

Purpose

This manual is intended to give users an understanding of the functions described in the **Organization** below.

Organization

The RL78/G1E manual is separated into three parts: this manual, RL78/G1A user's manual, and the RL78 family software user's manual.

RL78/G1E User's Manual (This Manual)	**RL78/G1A Hardware User's Manual**	**RL78 family Software User's Manual**
• Pin functions • Internal block functions • On-chip peripheral functions • Electrical specifications	• Pin functions • Internal block functions • Interrupts • Other on-chip peripheral functions • Electrical specifications	• CPU functions • Instruction set • Explanation of each instruction

(3/4)

Item		RL78/G1E		RL78/G1A	Remarks
		64-pin products	80-pin products	(64-pin products)	
Clock output / Buzzer output		–	1 channel • 2.44 kHz, 4.88 kHz, 9.76 kHz, 1.25 MHz, 2.5 MHz, 5 MHz, 10 MHz (Main system clock: f_{MAIN} = 20 MHz operation)	2 channels • 2.44 kHz, 4.88 kHz, 9.76 kHz, 1.25 MHz, 2.5 MHz, 5 MHz, 10 MHz (Main system clock: f_{MAIN} = 20 MHz operation) • 256 Hz, 512 Hz, 1.024 kHz, 2.048 kHz, 4.096 kHz, 8.192 kHz, 16.384 kHz, 32.768 kHz (Subsystem clock: f_{SUB} = 32.768 kHz operation)	There are some differences between RL78/G1E and RL78/G1A. See the section 3. 9 about details.
8/12-bit resolution A/D converter (AV_{DD} = 1.6 to 3.6 V)		13 channels	17 channels	28 channels	Some differences. See the section 3. 11 about details.
Serial array unit		<Unit 0> • CSI: 1 channel/ simplified I^2C: 1 channel/ UART: 1 channel • UART: 1 channel <Unit 1> • CSI: 1 channel/ UART: 1 channel (LIN-bus supported)	<Unit 0> • CSI: 1 channel/ simplified I^2C: 1 channel/ UART: 1 channel • CSI: 1 channel/ simplified I^2C: 1 channel/ UART: 1 channel <Unit 1> • CSI: 2 channel/ simplified I^2C: 1 channel/ UART: 1 channel (LIN-bus supported)	<Unit 0> • CSI: 2 channel/ simplified I^2C: 2 channel/ UART: 1 channel • CSI: 2 channel/ simplified I^2C: 2 channel/ UART: 1 channel <Unit 1> • CSI: 2 channel/ simplified I^2C: 2 channel/ UART: 1 channel (LIN-bus supported)	Some differences. See the section 3. 12 about details.
	I^2C bus	–		1 channel	Not provided in RL78/G1E. (See 3. 13)
Multiplier and divider/ multiply accumulator		5 functions (Multiplier, divider, multiply accumulator)		5 functions (Multiplier, divider, multiply accumulator)	See the section 3. 14 about details.
DMA controller		2 channels		2 channels	See the section 3. 15 about details.
Vectored interrupt sources	Internal	25		27	Some differences. See the section 3. 16 about details.
	External	2	5	13	
Key interrupt		4 (7)[Note] channels	4 (8)[Note] channels	10 channels	Some differences. See the section 3. 17 about details.

Note Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR).

(2) 80-pin products

Table 3-2. List of Differences in Special Function Registers (SFRs) (1/4)

Address	RL78/G1E (80-pin products)			RL78/G1A (64-pin products)		
	SFRs Name	Symbol		SFRs Name	Symbol	
FFF00H	Port register 0 Note	P0		Port register 0	P0	
FFF01H	Port register 1 Note	P1		Port register 1	P1	
FFF02H	Port register 2 Note	P2		Port register 2	P2	
FFF03H				Port register 3	P3	
FFF04H	Port register 4 Note	P4		Port register 4	P4	
FFF05H	Same as RL78/G1A (64-pin products)	P5		Port register 5	P5	
FFF06H				Port register 6	P6	
FFF07H	Port register 7 Note	P7		Port register 7	P7	
FFF0CH	Port register 12 Note	P12		Port register 12	P12	
FFF0DH	Same as RL78/G1A (64-pin products)	P13		Port register 13	P13	
FFF0EH	Port register 14 Note	P14		Port register 14	P14	
FFF0FH				Port register 15	P15	
FFF10H	Same as RL78/G1A (64-pin products)	TXD0/ SIO00	SDR00	Serial data register 00	TXD0/ SIO00	SDR00
FFF11H		—			—	
FFF12H	Same as RL78/G1A (64-pin products)	RXD0/ SIO01	SDR01	Serial data register 01	RXD0/ SIO01	SDR01
FFF13H		—			—	
FFF18H	Same as RL78/G1A (64-pin products)	TDR00		Timer data register 00	TDR00	
FFF19H						
FFF1AH	Same as RL78/G1A (64-pin products)	TDR01L	TDR01	Timer data register 01	TDR01L	TDR01
FFF1BH		TDR01H			TDR01H	
FFF1EH	Same as RL78/G1A (64-pin products)	ADCR		12-bit A/D conversion result register	ADCR	
FFF1FH	Same as RL78/G1A (64-pin)	ADCRH		8-bit A/D conversion result register	ADCRH	
FFF20H	Port mode register 0 Note	PM0		Port mode register 0	PM0	
FFF21H	Port mode register 1 Note	PM1		Port mode register 1	PM1	
FFF22H	Port mode register 2 Note	PM2		Port mode register 2	PM2	
FFF23H				Port mode register 3	PM3	
FFF24H	Port mode register 4 Note	PM4		Port mode register 4	PM4	
FFF25H	Same as RL78/G1A (64-pin products)	PM5		Port mode register 5	PM5	
FFF26H	Port mode register 6 Note	PM6		Port mode register 6	PM6	
FFF27H	Port mode register 7 Note	PM7		Port mode register 7	PM7	
FFF2CH				Port mode register 12	PM12	
FFF2EH	Port mode register 14 Note	PM14		Port mode register 14	PM14	
FFF2FH	Port mode register 15 Note	PM15		Port mode register 15	PM15	
FFF30H	Same as RL78/G1A (64-pin products)	ADM0		A/D converter mode register 0	ADM0	
FFF31H	Analog input channel specification register Note	ADS		Analog input channel specification register	ADS	
FFF32H	A/D converter mode register 1 Note	ADM1		A/D converter mode register 1	ADM1	

Note The bit setting is different from that of RL78/G1A (64-pin products).

Caution Do not write data to the registers which is in the row with painted gray.

Table 3-2. List of Differences in Special Function Registers (SFRs) (3/4)

Address	RL78/G1E (80-pin products)		RL78/G1A (64-pin products)	
	SFRs Name	Symbol	SFRs Name	Symbol
FFF90H	Same as RL78/G1A (64-pin products)	ITMC	Interval timer control register	ITMC
FFF91H				
FFF92H			Second count register	SEC
FFF93H			Minute count register	MIN
FFF94H			Hour count register	HOUR
FFF95H			Week count register	WEEK
FFF96H			Day count register	DAY
FFF97H			Month count register	MONTH
FFF98H			Year count register	YEAR
FFF99H			Watch error correction register	SUBCUD
FFF9AH			Alarm minute register	ALARMWM
FFF9BH			Alarm hour register	ALARMWH
FFF9CH			Alarm week register	ALARMWW
FFF9DH			Real-time clock control register 0	RTCC0
FFF9EH			Real-time clock control register 1	RTCC1
FFFA0H	Clock operation mode control register Note	CMC	Clock operation mode control register	CMC
FFFA1H	Clock operation status control register Note	CSC	Clock operation status control register	CSC
FFFA2H	Same as RL78/G1A (64-pin products)	OSTC	Oscillation stabilization time counter status register	OSTC
FFFA3H	Same as RL78/G1A (64-pin products)	OSTS	Oscillation stabilization time select register	OSTS
FFFA4H	System clock control register Note	CKC	System clock control register	CKC
FFFA5H	Clock output select register 0 Note	CKS0	Clock output select register 0	CKS0
FFFA6H			Clock output select register 1	CKS1
FFFA8H	Same as RL78/G1A (64-pin products)	RESF	Reset control flag register	RESF
FFFA9H	Same as RL78/G1A (64-pin products)	LVIM	Voltage detection register	LVIM
FFFAAH	Same as RL78/G1A (64-pin products)	LVIS	Voltage detection level register	LVIS
FFFABH	Same as RL78/G1A (64-pin products)	WDTE	Watchdog timer enable register	WDTE
FFFACH	Same as RL78/G1A (64-pin products)	CRCIN	CRC input register	CRCIN

Note The bit setting is different from that of RL78/G1A (64-pin products).

Caution Do not write data to the registers which is in the row with painted gray.

<R> **(2) Low-speed on-chip oscillator clock (Low-speed on-chip oscillator)**

This circuit oscillates a clock of f_{IL} = 15 kHz (TYP.).

The low-speed on-chip oscillator clock cannot be used as the CPU clock.

Only the following peripheral hardware runs on the low-speed on-chip oscillator clock.

- Watchdog timer
- 12-bit Interval timer

<R> This clock operates when bit 4 (WDTON) of the option byte (000C0H), bit 4 (WUTMMCK0) of the subsystem clock supply mode control register (OSMC), or both are set to 1.

However, when WDTON = 1, WUTMMCK0 = 0, and bit 0 (WDSTBYON) of the option byte (000C0H) is 0, oscillation of the low-speed on-chip oscillator stops if the HALT or STOP instruction is executed.

Remark f_X: X1 clock oscillation frequency

f_{IH}: High-speed on-chip oscillator clock frequency

f_{EX}: External main system clock frequency

f_{IL}: Low-speed on-chip oscillator clock frequency

3. 5. 2 Configuration of clock generator

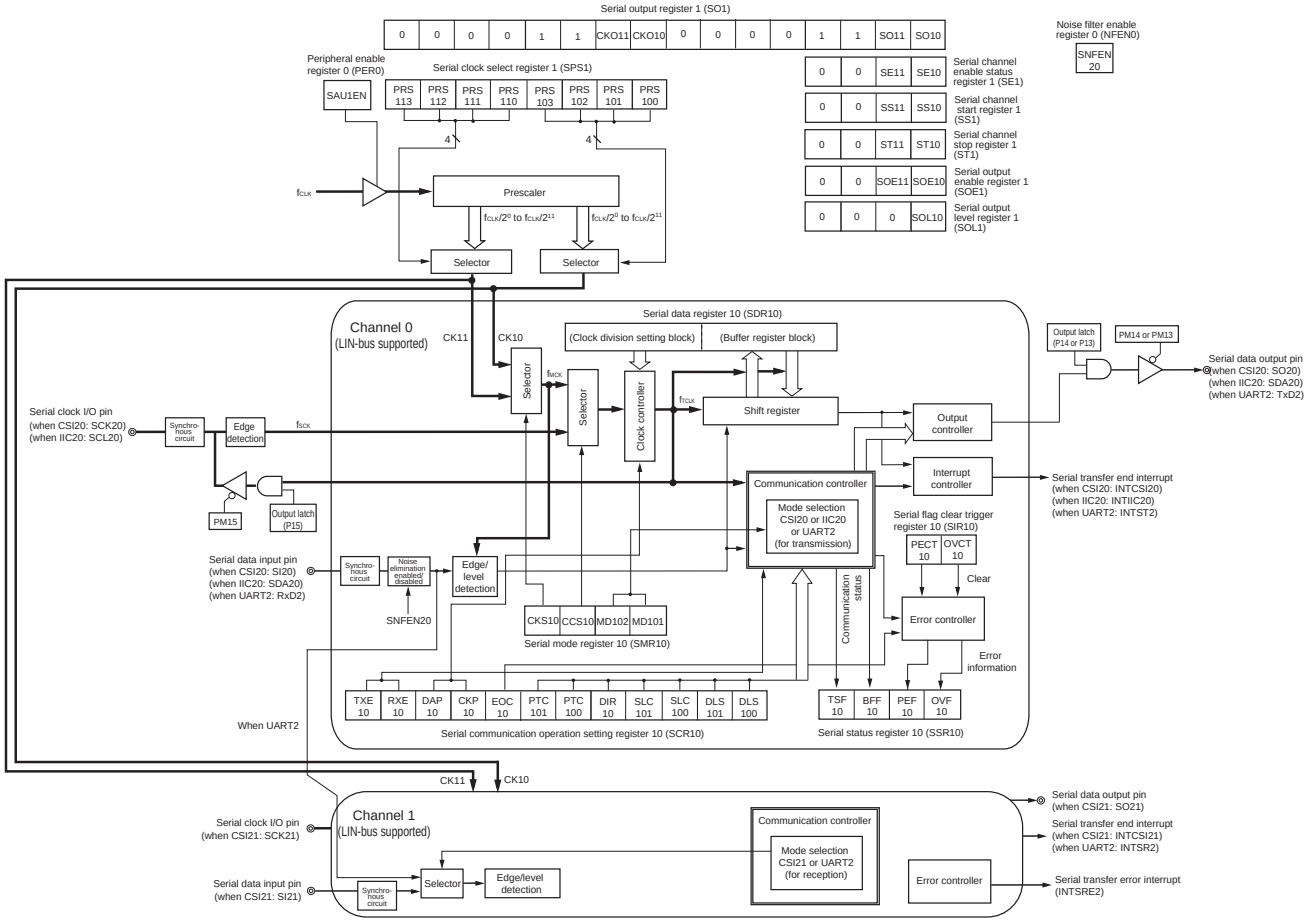
The clock generator includes the following hardware.

Table 3-6. Configuration of Clock Generator

Item	Configuration
Control registers	Clock operation mode control register (CMC) System clock control register (CKC) Clock operation status control register (CSC) Oscillation stabilization time counter status register (OSTC) Oscillation stabilization time select register (OSTS) Peripheral enable register 0 (PER0) <R> Subsystem clock supply mode control register (OSMC) High-speed on-chip oscillator frequency select register (HOCODIV) High-speed on-chip oscillator trimming register (HIOTRM)
Oscillators	X1 oscillator High-speed on-chip oscillator Low-speed on-chip oscillator

<R> Figure 3-10 shows the block diagram of the serial array unit 1.

Figure 3-10. Block Diagram of Serial Array Unit 1



<R> 3. 12. 2. 1 Shift register

This is a 9-bit register that converts parallel data into serial data or vice versa.

In case of the UART communication of nine bits of data, nine bits (bits 0 to 8) are used[Note 1].

The shift register cannot be directly manipulated by program.

During reception, it converts data input to the serial pin into parallel data, and stores to the lower 8/9 bits of the SDRmn register.

When data is transmitted, the value transferred from the lower 8/9 bits of the SDRmn register to this register is output as serial data from the serial output pin.

For details, see **3. 12. 2. 2 Lower 8/9 bits of the serial data register mn (SDRmn)**.

	8	7	6	5	4	3	2	1	0
Shift register									

<R> 3. 12. 2. 2 Lower 8/9 bits of the serial data register mn (SDRmn)

The SDRmn register is the transmit/receive data register (16 bits) of channel n. Bits 8 to 0 of SDR00, SDR01 (lower 9 bits) or bits 7 to 0 of SDR02, SDR03, SDR10Note 1, and SDR11Note 1 (lower 8 bits) function as a transmit/receive buffer register, and bits 15 to 9 (higher 7 bits) are used as a register that sets the division ratio of the operation clock (f_{MCK}).

Remark For the function of the higher 7 bits of the SDRmn register, see **12. 3. 5 Higher 7 bits of the serial data register mn (SDRmn)** in **RL78/G1A Hardware User's Manual (R01UH0305E)**.

When data is received, parallel data converted by the shift register is stored in the lower 8/9 bits. When data is to be transmitted, set transmit to be transferred to the shift register to the lower 8/9 bits.

The data stored in the lower 8/9 bits of this register is as follows, depending on the setting of bits 0 and 1 (DLSmn0, DLSmn1) of serial communication operation setting register mn (SCRmn), regardless of the output sequence of the data.

- 7-bit data length (stored in bits 0 to 6 of SDRmn register)
- 8-bit data length (stored in bits 0 to 7 of SDRmn register)
- 9-bit data length (stored in bits 0 to 8 of SDRmn register)[Note 1]

The SDRmn register can be read or written in 16-bit units.

The lower 8/9 bits of the SDRmn register can be read or written[Note 2] as the following SFR, depending on the communication mode.

- CSIp communication … SIOp (CSIp data register)
- UARTq reception … RXDq (UARTq receive data register)
- UARTq transmission … TXDq (UARTq transmit data register)
- IICr communication … SIOr (IICr data register)

The SDRmn register can be read or written in 16-bit units.

Reset signal generation clears the SDRmn register to 0000H.

Notes 1. Only following UART0 can be specified for the 9-bit data length.

2. Writing in 8-bit units is prohibited when the operation is stopped (SEmn = 0).

Remarks 1. After data is received, "0" is stored in bits 0 to 8 in bit portions that exceed the data length.

2. m: Unit number (m = 0, 1)
n: Channel number (n = 0 to 3)
p: CSI number (80-pin products: p = 00, 10, 20, 21 64-pin products: p = 00, 21)
q: UART number (q = 0 to 2)
r: IIC number (80-pin products: r = 00, 10, 20 64-pin products: r = 00)

<R> **Notes 1.** The SCR00, SCR02, and SCR10 registers only. Others are fixed to 0.

2. The SCR00 and SCR01 registers only. Others are fixed to 1.

3. When using CSImn not with EOCmn = 0, error interrupt INTSRE0 may be generated.

Caution Be sure to clear bits 3, 6, and 11 to "0". Be sure to set bit 2 to "1".

Remark m: Unit number (m = 0, 1)

n: Channel number (n = 0 to 3)

p: CSI number (80-pin products: p = 00, 10, 20, 21 64-pin products: p = 00, 21)

- 80-pin products

Address: FFFE8H After reset: FFH R/W

Symbol	7	6	5	<4>	<3>	<2>	<1>	<0>
PR00L	1	1	1	PPR02	PPR01	PPR00	LVIPR0	WDTIPR0

Address: FFFECH After reset: FFH R/W

Symbol	7	6	5	4	<3>	<2>	<1>	<0>
PR10L	1	1	1	PPR12	PPR11	PPR10	LVIPR1	WDTIPR1

Address: FFFE9H After reset: FFH R/W

Symbol	<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>
PR00H	TMPR001H SREPR00	SRPR00	STPR00 IICPR000	DMAPR01	DMAPR00	SREPR02	SRPR02 CSIPR021	STPR02 CSIPR020 IICPR020

Address: FFFEDH After reset: FFH R/W

Symbol	<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>
PR10H	TMPR101H SREPR10	SRPR10	STPR10 CSIPR100 IICPR100	DMAPR11	DMAPR10	SREPR12	SRPR12 CSIPR121	STPR12 CSIPR120 IICPR120

Address: FFFEAH After reset: FFH R/W

Symbol	<7>	<6>	<5>	<4>	3	<2>	<1>	<0>
PR01L	TMPR003	TMPR002	TMPR001	TMPR000	1	SREPR01 TMPR003H	SRPR01	STPR01 CSIPR010 IICPR010

Address: FFFEEH After reset: FFH R/W

Symbol	<7>	<6>	<5>	<4>	3	<2>	<1>	<0>
PR11L	TMPR103	TMPR102	TMPR101	TMPR100	1	SREPR11 TMPR103H	SRPR11	STPR11 CSIPR110 IICPR110

Address: FFFEBH After reset: FFH R/W

Symbol	<7>	6	5	4	<3>	<2>	1	<0>
PR01H	TMPR004	1	1	1	KRPR0	ITPR0	1	ADPR0

Address: FFFEFH After reset: FFH R/W

Symbol	<7>	6	5	4	<3>	<2>	1	<0>
PR11H	TMPR104	1	1	1	KRPR1	ITPR1	1	ADPR1

3. 17. 3. 4 Port mode registers 0 to 2, 7 (PM0 to PM2, PM7)

(1) 64-pin products

Symbol	7	6	5	4	3	2	1	0	Address	After Reset	R/W
PM0	1	PM06	PM05	PM04	PM03	PM02	PM01	PM00	FFF20H	FFH	R/W
PM1	1	PM16	1	PM14	PM13	PM12	PM11	PM10	FFF21H	FFH	R/W
PM2	PM27	PM26	PM25	PM24	PM23	PM22	PM21	PM20	FFF22H	FFH	R/W
PM7	PM77	PM76	PM75	PM74	PM73	PM72	PM71	PM70	FFF27H	FFH	R/W

Cautions 1. Be sure to clear bits 4 to 6 of the PM0 register, bit 6 of the PM1 register, bits 4 to 7 of the PM2 register, bits 4 to 7 of the PM7 register to "0".

2. Be sure to set bit 7 of the PM0 register, bits 5 and 7 of the PM1 register to "1".

(2) 80-pin products

Symbol	7	6	5	4	3	2	1	0	Address	After Reset	R/W
PM0	1	PM06	PM05	PM04	PM03	PM02	PM01	PM00	FFF20H	FFH	R/W
PM1	1	PM16	PM15	PM14	PM13	PM12	PM11	PM10	FFF21H	FFH	R/W
PM2	PM27	PM26	PM25	PM24	PM23	PM22	PM21	PM20	FFF22H	FFH	R/W
PM7	PM77	PM76	PM75	PM74	PM73	PM72	PM71	PM70	FFF27H	FFH	R/W

Cautions 1. Be sure to clear bits 5 and 6 of the PM0 register, bit 6 of the PM1 register, bits 5 to 7 of the PM2 register, bits 4 to 7 of the PM7 register to "0".

2. Be sure to set bit 7 of the PM0 register, bit 7 of the PM1 register to "1".

<R> The reset and internal interrupt signals are generated in each mode as follows.

Interrupt & reset mode (LVIMDS1, LVIMDS0 = 1, 0)	Reset mode (LVIMDS1, LVIMDS0 = 1, 1)	Interrupt mode (LVIMDS1, LVIMDS0 = 0, 1)
Generates an interrupt request signal by detecting $V_{DD} < V_{LVDH}$ when the operating voltage falls, and an internal reset by detecting $V_{DD} < V_{LVDL}$. Releases an internal reset by detecting $V_{DD} \geq V_{LVDH}$.	Releases an internal reset by detecting $V_{DD} \geq V_{LVD}$. Generates an interrupt request signal by detecting $V_{DD} < V_{LVD}$.	Releases an internal reset by detecting $V_{DD} \geq V_{LVD}$ at power on after the first release of the POR. Generates an interrupt request signal by detecting $V_{DD} < V_{LVD}$ or $V_{DD} \geq V_{LVD}$ at power on after the second release of the POR.

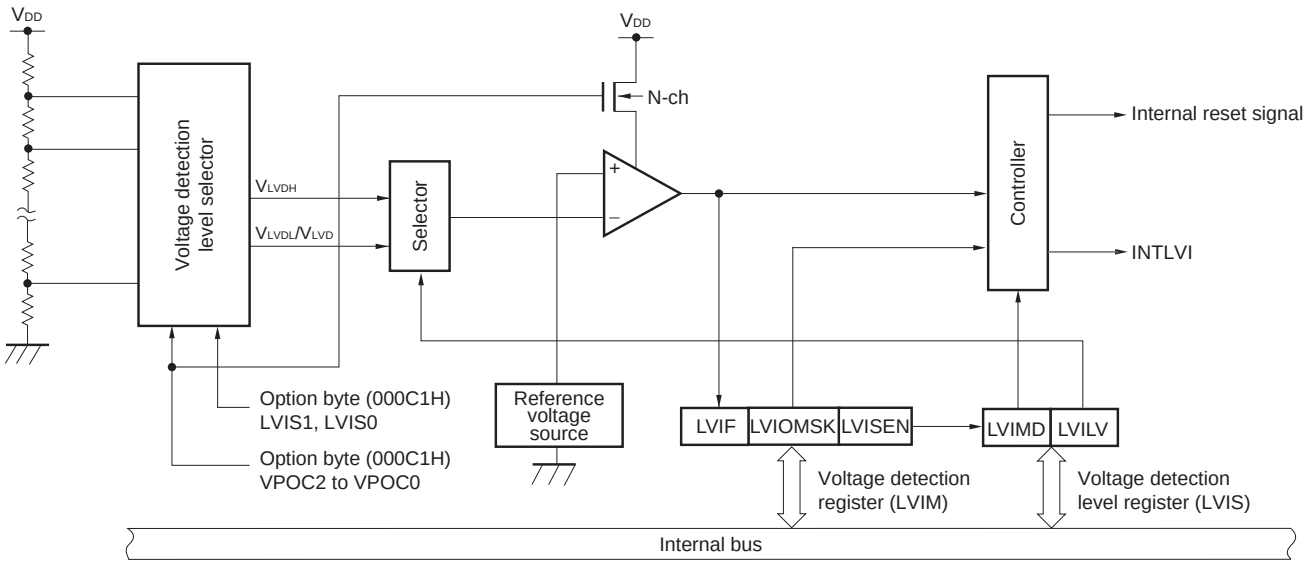
While the voltage detector is operating, whether the supply voltage or the input voltage from an external input pin is more than or less than the detection level can be checked by reading the voltage detection flag (LVIF: bit 0 of the voltage detection register (LVIM)).

Bit 0 (LVIRF) of the reset control flag register (RESF) is set to 1 if reset occurs. For details of the RESF register, see **3. 19 Reset Function**.

3. 21. 2 Configuration of voltage detector

The block diagram of the voltage detector is shown in Figure 3-15.

<R> **Figure 3-15. Block Diagram of Voltage Detector**



4. 1. 3 Registers controlling the configurable amplifiers

The configurable amplifiers are controlled by the following 9 registers:

- Configuration register 1 (CONFIG1)
- Configuration register 2 (CONFIG2)
- MPX setting register 1 (MPX1)
- MPX setting register 2 (MPX2)
- Gain control register 1 (GC1)
- Gain control register 2 (GC2)
- Gain control register 3 (GC3)
- AMP operation mode control register (AOMC)
- Power control register 1 (PC1)

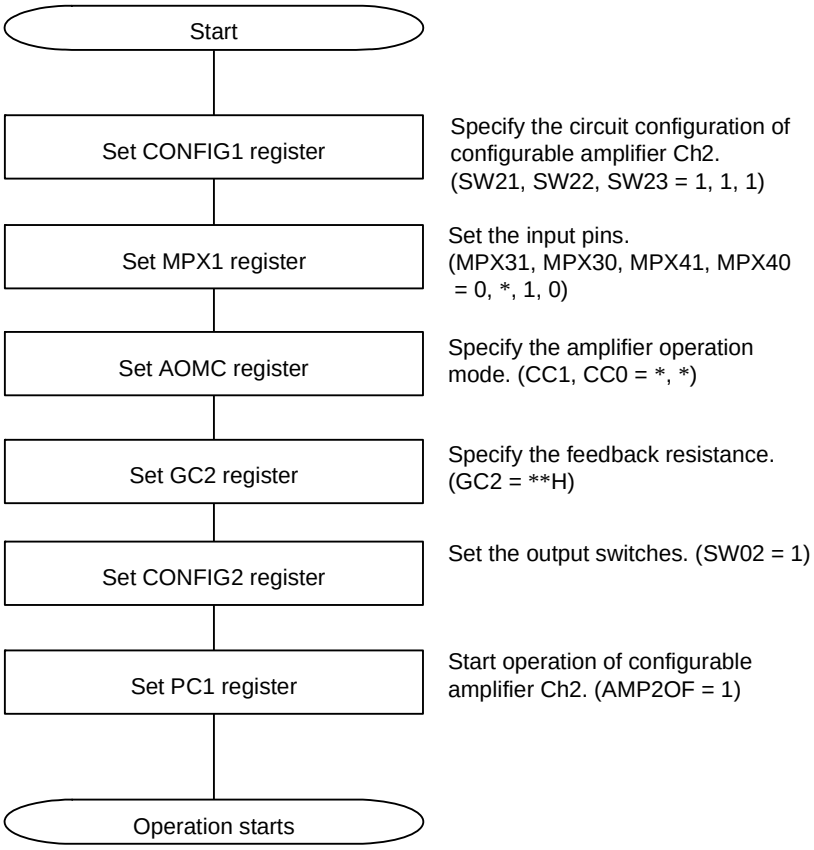
Table 4-5. Gain of Configurable Amplifier Ch2 (Inverting Amplifier and Differential Amplifier)

AMPG24	AMPG23	AMPG22	AMPG21	AMPG20	Gain of Configurable Amplifier Ch2 (Typ.)
0	0	0	0	0	6 dB
0	0	0	0	1	8 dB
0	0	0	1	0	10 dB
0	0	0	1	1	12 dB
0	0	1	0	0	14 dB
0	0	1	0	1	16 dB
0	0	1	1	0	18 dB
0	0	1	1	1	20 dB
0	1	0	0	0	22 dB
0	1	0	0	1	24 dB
0	1	0	1	0	26 dB
0	1	0	1	1	28 dB
0	1	1	0	0	30 dB
0	1	1	0	1	32 dB
0	1	1	1	0	34 dB
0	1	1	1	1	36 dB
1	0	0	0	0	38 dB
1	0	0	0	1	40 dB
Other than above					Setting prohibited

Table 4-6. Feedback Resistance of Configurable Amplifier Ch2 (Transimpedance Amplifier)

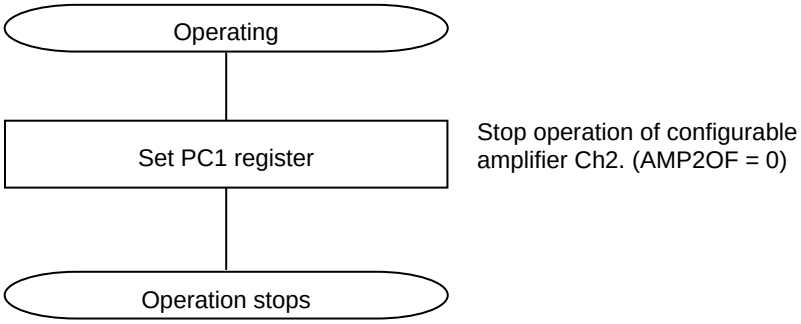
AMPG24	AMPG23	AMPG22	AMPG21	AMPG20	Feedback Resistance of Configurable Amplifier Ch2 (Typ.)
0	0	0	0	0	20 kΩ
0	0	0	0	1	
0	0	0	1	0	
0	0	0	1	1	40 kΩ
0	0	1	0	0	
0	0	1	0	1	
0	0	1	1	0	80 kΩ
0	0	1	1	1	
0	1	0	0	0	
0	1	0	0	1	160 kΩ
0	1	0	1	0	
0	1	0	1	1	
0	1	1	0	0	320 kΩ
0	1	1	0	1	
0	1	1	1	0	
0	1	1	1	1	640 kΩ
1	0	0	0	0	
1	0	0	0	1	
Other than above					Setting prohibited

Example of procedure for starting configurable amplifier Ch2 (transimpedance amplifier)



Remark *: don't care

Example of procedure for stopping configurable amplifier Ch2 (transimpedance amplifier)



(3) Power control register 2 (PC2)

This register is used to enable or disable operation of the gain adjustment amplifier, the low-pass filter, the high-pass filter, the variable output voltage regulator, the reference voltage generator, and the temperature sensor. Use this register to stop unused functions to reduce power consumption and noise.

When using the gain adjustment amplifier, be sure to set bit 4 to 1.

Reset signal input clears this register to 00H.

- **64-pin products**

Address: 12H After reset: 00H R/W

	7	6	5	4	3	2	1	0
PC2	0	0	0	GAINOF	LPFOF	0	LDOOF	TEMPOF

GAINOF	Operation of gain adjustment amplifier
0	Stop operation of the gain adjustment amplifier.
1	Enable operation of the gain adjustment amplifier.

Caution Be sure to clear bit 2 to "0".

Remark Bits 7 to 5 can be set to 1, but this has no effect on the function.

- **80-pin products**

Address: 12H After reset: 00H R/W

	7	6	5	4	3	2	1	0
PC2	0	0	0	GAINOF	LPFOF	HPFOF	LDOOF	TEMPOF

GAINOF	Operation of gain adjustment amplifier
0	Stop operation of the gain adjustment amplifier.
1	Enable operation of the gain adjustment amplifier.

Remark Bits 7 to 5 can be set to 1, but this has no effect on the function.

4. 6. 3 Registers controlling the temperature sensor

The temperature sensor is controlled by power control register 2 (PC2).

(1) Power control register 2 (PC2)

This register is used to enable or disable operation of the gain adjustment amplifier, the low-pass filter, the high-pass filter, the variable output voltage regulator, the reference voltage generator, and the temperature sensor. Use this register to stop unused functions to reduce power consumption and noise.

When selecting the signal to be input to the temperature sensor, be sure to set bit 0 to 1.

Reset signal input clears this register to 00H.

- 64-pin products

Address: 12H After reset: 00 R/W

	7	6	5	4	3	2	1	0
PC2	0	0	0	GAINOF	LPFOF	0	LDOOF	TEMPOF

TEMPOF	Operation of temperature sensor
0	Stop operation of the temperature sensor.
1	Enable operation of the temperature sensor.

Caution Be sure to clear bit 2 to “0”.

Remark Bits 7 to 5 can be set to 1, but this has no effect on the function.

- 80-pin products

Address: 12H After reset: 00 R/W

	7	6	5	4	3	2	1	0
PC2	0	0	0	GAINOF	LPFOF	HPFOF	LDOOF	TEMPOF

TEMPOF	Operation of temperature sensor
0	Stop operation of the temperature sensor.
1	Enable operation of the temperature sensor.

Remark Bits 7 to 5 can be set to 1, but this has no effect on the function.

<R> **(3) Communication between devices at same potenntial (CSI mode) (master mode, SCKp ... internal clock output)**

(T_A = –40 to +85°C, 1.6 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions	HS Note 1		LS Note 2		LV Note 3		Unit
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
SCKp cycle time	t_{KCY1}	2.7 V ≤ V_{DD} ≤ 5.5 V t_{KCY1} ≥ 4/f_{CLK}	125		500		1000		ns
		2.4 V ≤ V_{DD} ≤ 5.5 V t_{KCY1} ≥ 4/f_{CLK}	250		500		1000		ns
		1.8 V ≤ V_{DD} ≤ 5.5 V t_{KCY1} ≥ 4/f_{CLK}	500		500		1000		ns
		1.7 V ≤ V_{DD} ≤ 5.5 V t_{KCY1} ≥ 4/f_{CLK}	1000		1000		1000		ns
		1.6 V ≤ V_{DD} ≤ 5.5 V t_{KCY1} ≥ 4/f_{CLK}	–		1000		1000		ns
SCKp high-level width low-level width	t_{KH1}, t_{KL1}	4.0 V ≤ V_{DD} ≤ 5.5 V	t_{KCY1}/2 -12		t_{KCY1}/2 -50		t_{KCY1}/2 -50		ns
		2.7 V ≤ V_{DD} ≤ 5.5 V	t_{KCY1}/2 -18		t_{KCY1}/2 -50		t_{KCY1}/2 -50		ns
		2.4 V ≤ V_{DD} ≤ 5.5 V	t_{KCY1}/2 -38		t_{KCY1}/2 -50		t_{KCY1}/2 -50		ns
		1.8 V ≤ V_{DD} ≤ 5.5 V	t_{KCY1}/2 -50		t_{KCY1}/2 -50		t_{KCY1}/2 -50		ns
		1.7 V ≤ V_{DD} ≤ 5.5 V	t_{KCY1}/2 -100		t_{KCY1}/2 -100		t_{KCY1}/2 -100		ns
		1.6 V ≤ V_{DD} ≤ 5.5 V	–		t_{KCY1}/2 -100		t_{KCY1}/2 -100		ns
<R> Slp setup time (to SCKp↑) Note 4	t_{SIK1}	4.0 V ≤ V_{DD} ≤ 5.5 V	44		110		110		ns
		2.7 V ≤ V_{DD} ≤ 5.5 V	44		110		110		ns
		2.4 V ≤ V_{DD} ≤ 5.5 V	75		110		110		ns
		1.8 V ≤ V_{DD} ≤ 5.5 V	110		110		110		ns
		1.7 V ≤ V_{DD} ≤ 5.5 V	220		220		220		ns
		1.6 V ≤ V_{DD} ≤ 5.5 V	–		220		220		ns
Slp hold time (from SCKp↑) Note 4	t_{KSI1}	1.7 V ≤ V_{DD} ≤ 5.5 V	19		19		19		ns
		1.6 V ≤ V_{DD} ≤ 5.5 V	–		19		19		
Slp hold time (from SCKp↑) Note 5	t_{KSO1}	1.7 V ≤ V_{DD} ≤ 5.5 V C = 30 pF Note 6		25		25		25	ns
		1.6 V ≤ V_{DD} ≤ 5.5 V C = 30 pF Note 6		–		25		25	

(**Notes Caution** and **Remark** are listed on the next page.)

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Edition	Description	Chapter
Rev.1.00	Modification of the description in **5. 2. 8 Timing specs for switching flash memory programming modes**	**CHAPTER 5 ELECTRICAL SPECIFICATIONS**
	Addition of the specification depending on the products in **5. 3. 3. 2 Gain adjustment amplifier characteristics**	
	Addition of the specification for “CLK_SYNCH input voltage” in **5. 3. 3. 2 Gain adjustment amplifier characteristics (2) 80-pin products**	
	Error correction of the description and addition of the specification for “CLK_SYNCH input voltage” in **5. 3. 3. 4 Low-pass filter characteristics**	
	Error correction of the description and addition of the specification for “CLK_SYNCH input voltage” in **5. 3. 3. 5 High-pass filter characteristics**	
Rev.0.04	Change of the name for CS from “Slave Select” to “Chip Select”	Whole pages
	Deletion of the word “interface” from the name of SPI	
	Error correction of the figures in **1. 4 Pin Configuration (Top View)**	**CHAPTER 1 OUTLINE**
	Error correction of the description (deletion of “SCLA0”, “SCLA1”) in **1. 4. 3 Pin identification (Microcontroller Block)**	
	Error correction of the figures in **1. 5 Block Diagram**	
	Error correction of the function names and modification of the description for the function in **2. 2 Pin Functions in Analog Block**	**CHAPTER 2 PIN FUNCTIONS**
	Error correction of the description for the pin of ANI30 (D/A converter -> A/D converter) in **2. 3. 4 P40 to P42 (port 4)**	
	Modification of the description in **2. 3. 43 I.C**	
	Addition of “Remarks” on the tables in **3. 1 Differences in Functions between RL78/G1E and RL78/G1A**	**CHAPTER 3 MICROCONTROLLER FUNCTION**
	Modification of the description on the tables (deletion of the same registers as RL78/G1A) in **3. 2 Differences in (Expanded) Special-Function Registers between RL78/G1E and RL78/G1A**	
	Modification of the description and change of the sequence flow of the setting procedure (2) in **3. 3. 3 Connecting to an external device with different potential (1.8 V, 2.5 V, 3 V)**	
	Addition of **3. 4. 4 Resonator and Oscillator Constants**	
	Error correction of the description on **Table 3-14.**	
	Addition of **3. 13 Safety Functions**	
	Modification of the gain setting of non-inverting amplifier in **5. 1 Overview of Configurable Amplifier Features** and in **5. 3 Registers Controlling the Configurable Amplifiers**	**CHAPTER 5 CONFIGURABLE AMPLIFIERS**
	Modification of the description in **8. 1 Overview of Low-Pass Filter Features**	**CHAPTER 8 LOW-PASS FILTER**
	Modification of the description in **9. 1 Overview of High-Pass Filter Features**	**CHAPTER 8 HIGH-PASS FILTER**
	Addition of **Note** in **11. 3 Registers Controlling the Variable Output Voltage Regulator**	**CHAPTER 11 VARIABLE OUTPUT VOLTAGE REGULATOR**