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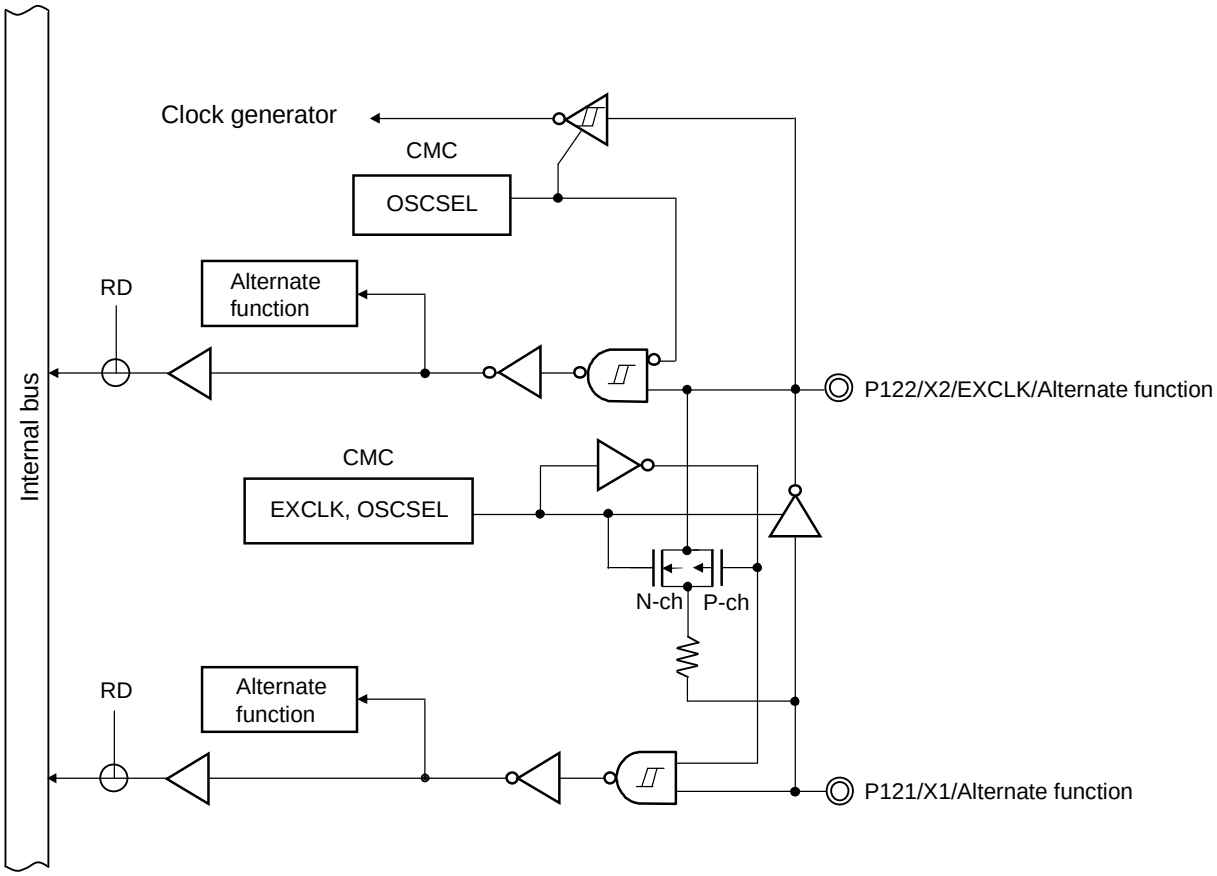
Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	RL78
Core Size	16-Bit
Speed	32MHz
Connectivity	CSI, I²C, LINbus, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	26
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	1.6V ~ 5.5V
Data Converters	A/D 17x8/12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	80-LQFP
Supplier Device Package	80-LFQFP (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f10fmedfb-x0

<R>

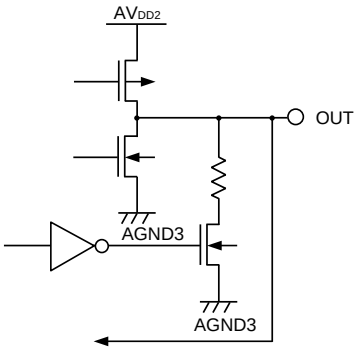
Figure 2-4. Pin Block Diagram for Pin Type 2-2-1



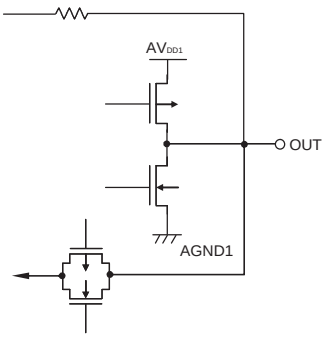
Remark For alternate functions, see **2. 1. 1 Port functions**.

Figure 2-13. Pin I/O Circuit List (2/2)

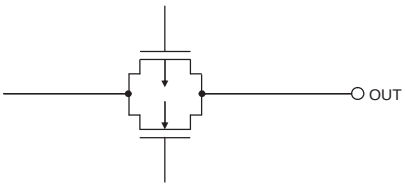
ANALOG9



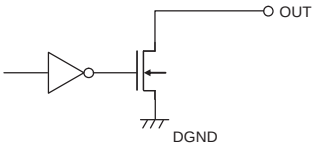
ANALOG10



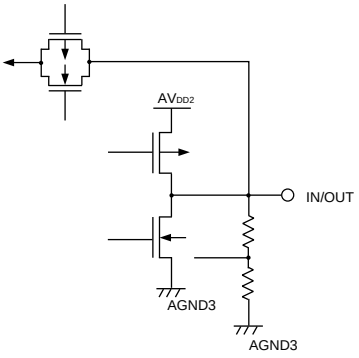
ANALOG11



ANALOG12



ANALOG13



(2/4)

Item		RL78/G1E		RL78/G1A (64-pin products)	Remarks
		64-pin products	80-pin products		
Low-speed on-chip oscillator		15 kHz (TYP.): V_{DD} = 1.6 to 5.5 V		15 kHz (TYP.): V_{DD} = 1.6 to 3.6 V	Some differences. See the section 3. 5 about details. Subsystem clock is not available for RL78/G1E.
Minimum instruction execution time		0.03125 μs (High-speed on-chip oscillator: f_{IH} = 32 MHz operation)		0.03125 μs (High-speed on-chip oscillator: f_{IH} = 32 MHz operation)	
		0.05 μs (High-speed system clock: f_{MX} = 20 MHz operation)		0.05 μs (High-speed system clock: f_{MX} = 20 MHz operation)	
		–		30.5 μs (Subsystem clock: f_{SUB} = 32.768 kHz operation)	
Timer	16-bit timer	8 channels		8 channels	Some differences. See the section 3. 6 about details.
	Watchdog Timer	1 channel		1 channel	See the section 3. 10 about details.
	Real-time clock (RTC)	–		1 channel	RTC is not provided in RL78/G1E. (See 3. 7)
	12-bit Interval timer (IT)	1 channel		1 channel	See the section 3. 8 about details.
	Timer output	3 channels (PWM outputs: 2 Note)		7 channels (PWM outputs: 6 Note)	See the section 3. 6 about details.
	RTC output	–		1 channel • 1 Hz (subsystem clock: f_{SUB} = 32.768 kHz)	RTC is not provided in RL78/G1E. (See 3. 7)

Note The number of PWM outputs varies depending on the setting of channels in use.

Table 3-2. List of Differences in Special Function Registers (SFRs) (3/4)

Address	RL78/G1E (80-pin products)		RL78/G1A (64-pin products)	
	SFRs Name	Symbol	SFRs Name	Symbol
FFF90H	Same as RL78/G1A (64-pin products)	ITMC	Interval timer control register	ITMC
FFF91H				
FFF92H			Second count register	SEC
FFF93H			Minute count register	MIN
FFF94H			Hour count register	HOUR
FFF95H			Week count register	WEEK
FFF96H			Day count register	DAY
FFF97H			Month count register	MONTH
FFF98H			Year count register	YEAR
FFF99H			Watch error correction register	SUBCUD
FFF9AH			Alarm minute register	ALARMWM
FFF9BH			Alarm hour register	ALARMWH
FFF9CH			Alarm week register	ALARMWW
FFF9DH			Real-time clock control register 0	RTCC0
FFF9EH			Real-time clock control register 1	RTCC1
FFFA0H	Clock operation mode control register Note	CMC	Clock operation mode control register	CMC
FFFA1H	Clock operation status control register Note	CSC	Clock operation status control register	CSC
FFFA2H	Same as RL78/G1A (64-pin products)	OSTC	Oscillation stabilization time counter status register	OSTC
FFFA3H	Same as RL78/G1A (64-pin products)	OSTS	Oscillation stabilization time select register	OSTS
FFFA4H	System clock control register Note	CKC	System clock control register	CKC
FFFA5H	Clock output select register 0 Note	CKS0	Clock output select register 0	CKS0
FFFA6H			Clock output select register 1	CKS1
FFFA8H	Same as RL78/G1A (64-pin products)	RESF	Reset control flag register	RESF
FFFA9H	Same as RL78/G1A (64-pin products)	LVIM	Voltage detection register	LVIM
FFFAAH	Same as RL78/G1A (64-pin products)	LVIS	Voltage detection level register	LVIS
FFFABH	Same as RL78/G1A (64-pin products)	WDTE	Watchdog timer enable register	WDTE
FFFACH	Same as RL78/G1A (64-pin products)	CRCIN	CRC input register	CRCIN

Note The bit setting is different from that of RL78/G1A (64-pin products).

Caution Do not write data to the registers which is in the row with painted gray.

- Format of Timer Mode Register mn (TMRmn) (2/4)

Address: F0190H, F0191H (TMR00) - F019EH, F019FH (TMR07) After reset: 0000H R/W

Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TMRmn (n = 2, 4, 6)	CKS mn1	CKS mn0	0	CCS mn	MASTER mn	STS mn2	STS mn1	STS mn0	CIS mn1	CIS mn0	0	0	MD mn3	MD mn2	MD mn1	MD mn0

Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TMRmn (n = 1, 3)	CKS mn1	CKS mn0	0	CCS mn	SPLIT mn	STS mn2	STS mn1	STS mn0	CIS mn1	CIS mn0	0	0	MD mn3	MD mn2	MD mn1	MD mn0

Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TMRmn (n = 0, 5, 7)	CKS mn1	CKS mn0	0	CCS mn	0[Note]	STS mn2	STS mn1	STS mn0	CIS mn1	CIS mn0	0	0	MD mn3	MD mn2	MD mn1	MD mn0

Bit 11 of TMRmn (n = 2, 4, 6)

MASTER mn	Selection between using channel n independently or simultaneously with another channel (as a slave or master)
0	Operates in independent channel operation function or as slave channel in simultaneous channel operation function.
1	Operates as master channel in simultaneous channel operation function.
Only the channel 2, 4, 6 can be set as a master channel (MASTERmn = 1). Be sure to use channel 0, 5, 7 are fixed to 0 (Regardless of the bit setting, channel 0 operates as master, because it is the highest channel). Clear the MASTERmn bit to 0 for a channel that is used with the independent channel operation function.	

Bit 11 of TMRmn (n = 1, 3)

SPLITmn	Selection of 8 or 16-bit timer operation for channels 1 and 3
0	Operates as 16-bit timer. (Operates in independent channel operation function or as slave channel in simultaneous channel operation function.)
1	Operates as 8-bit timer.

STS mn2	STS mn1	STS mn0	Setting of start trigger or capture trigger of channel n
0	0	0	Only software trigger start is valid (other trigger sources are unselected).
0	0	1	Valid edge of the TImn pin input is used as both the start trigger and capture trigger.
0	1	0	Both the edges of the TImn pin input are used as a start trigger and a capture trigger.
1	0	0	Interrupt signal of the master channel is used (when the channel is used as a slave channel with the simultaneous channel operation function).
Other than above			Setting prohibited

<R> **Note** Bit 11 is fixed at 0 of read only, write is ignored.

Remark m: Unit number (m = 0), n: Channel number (n = 0 to 7 (however, timer input pin (TImn), timer output pin (TOmn): n = 0, 4, 7))

3. 6. 3. 13 Input switch control register (ISC)

The bit setting is same as that of RL78/G1A (64-pin products). For details, see **6. 3. 13 Input switch control register (ISC)** in **RL78/G1A Hardware User's Manual (R01UH0305E)**.

3. 6. 3. 14 Noise filter enable register 1 (NFEN1)

Address: F0071H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
NFEN1	TNFEN07	0	0	TNFEN04	0	0	0	TNFEN00

TNFEN07	Enable/disable using noise filter of TI07/TO07/P41 pin or RxD2/P14 pin input signal[Note]
0	Noise filter OFF
1	Noise filter ON

TNFEN04	Enable/disable using noise filter of TI04/TO04/P42 pin input signal
0	Noise filter OFF
1	Noise filter ON

TNFEN00	Enable/disable using noise filter of TI00/P00 pin input signal
0	Noise filter OFF
1	Noise filter ON

Note The applicable pin can be switched by setting the ISC1 bit of the ISC register.
ISC1 = 0: Whether or not to use the noise filter of the TI07 pin can be selected.
ISC1 = 1: Whether or not to use the noise filter of the RxD2 pin can be selected.

Caution Be sure to clear bits 6, 5, 3 to 1 to "0".

Notes 1. The number of bits used as the shift register and buffer register differs depending on the unit and channel.

- mn = 00, 01: lower 9 bits
- Other than above: lower 8 bits

2. The lower 8 bits of serial data register mn (SDRmn) can be read or written as the following SFR, depending on the communication mode.

- CSIp communication … SIOp (CSIp data register)
- UARTq reception … RXDq (UARTq receive data register)
- UARTq transmission … TXDq (UARTq transmit data register)
- IICr communication … SIOr (IICr data register)

Remark m: Unit number (m = 0, 1)
n: Channel number (n = 0 to 3)
p: CSI number (80-pin products: p = 00, 10, 20, 21 64-pin products: p = 00, 21)
q: UART number (q = 0 to 2)
r: IIC number (80-pin products: r = 00, 10, 20 64-pin products: r = 00)

Address: FFFD8H After reset: FFH R/W

Symbol	7	6	5	4	3	<2>	<1>	<0>
PR02L	1	1	1	1	1	TMPR007	TMPR006	TMPR005

Address: FFFDCH After reset: FFH R/W

Symbol	7	6	5	4	3	<2>	<1>	<0>
PR12L	1	1	1	1	1	TMPR107	TMPR106	TMPR105

Address: FFFD9H After reset: FFH R/W

Symbol	<7>	6	<5>	4	3	2	1	0
PR02H	FLPR0	1	MDPR0	1	1	1	1	1

Address: FFFDDH After reset: FFH R/W

Symbol	<7>	6	<5>	4	3	2	1	0
PR12H	FLPR1	1	MDPR1	1	1	1	1	1

Cautions 1. Be sure to set bits 3 to 7 of the PR00L register to “1”.

2. Be sure to set bits 3 to 7 of the PR10L register to “1”.

3. Be sure to set bit 3 of the PR01L register to “1”.

4. Be sure to set bit 3 of the PR11L register to “1”.

5. Be sure to set bits 1 and 4 to 6 of the PR01H register to “1”.

6. Be sure to set bits 1 and 4 to 6 of the PR11H register to “1”.

7. Be sure to set bits 3 to 7 of the PR02L register to “1”.

8. Be sure to set bits 3 to 7 of the PR12L register to “1”.

9. Be sure to set bits 0 to 4 and 6 of the PR02H register to “1”.

10. Be sure to set bits 0 to 4 and 6 of the PR12H register to “1”.

3. 17 Key Interrupt Function

The number of key interrupt input channels differs, depending on the product.

	64-pin products	80-pin products
Key interrupt input channels	4 ch (7 ch)	4 ch (8 ch)

Remarks 1. Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR).

2. Most of the following descriptions in this section use the case of 80-pin products as an example.

3. 17. 1 Functions of key interrupt

A key interrupt (INTKR) can be generated by inputting a rising/falling edge to the key interrupt input pins (KR0 to KR7).

There are two ways to identify the channel(s) to which a valid edge has been input:

- Identify the channel(s) (KR0 to KR7) by using the port input level.
- Identify the channel(s) (KR0 to KR5) by using the key interrupt flag.

Table 3-16. Assignment of Key Interrupt Detection Pins

Key Interrupt Pins	Key return mode register (KRM0)	Key return flag register (KRF)
KR0	KRM00	KRF0
KR1	KRM01	KRF1
KR2	KRM02	KRF2
KR3	KRM03	KRF3
KR4	KRM04	KRF4
KR5	KRM05	KRF5
KR6	KRM06	–
KR7	KRM07	–

Remark KR0 to KR3 (KR0 to KR6): 64-pin products
KR0 to KR3 (KR0 to KR7): 80-pin products
Functions in parentheses can be assigned via settings in the peripheral I/O redirection register (PIOR)

3. 20 Power-On-Reset Circuit

See **CHAPTER 20 POWER-ON-RESET CIRCUIT** in **RL78/G1A Hardware User's Manual (R01UH0305E)**.

3. 22. 3. 7 Frequency detection function

For details of each register, see **22. 3. 7 Frequency detection function** in **RL78/G1A Hardware User's Manual (R01UH0305E)**.

The bit settings which are different from that of RL78/G1A (64-pin products) are shown below.

(1) Timer input select register 0 (TIS0)

Address: F0074H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
TIS0	0	0	0	0	0	TIS02	TIS01	TIS00

TIS02	TIS01	TIS00	Selection of timer input used with channel 5
0	0	0	Default value
1	0	0	Low-speed on-chip oscillator clock (f_{IL})
Other than above			Setting prohibited

Caution High-level width, low-level width of timer input is selected, will require more than 1/f_{MCK} +10 ns. Therefore, when selecting f_{SUB} to f_{CLK} (CSS bit of CKS register = 1), can not TIS02 bit set to 1.

3. 22. 3. 8 A/D test function

See **22. 3. 8 A/D test function** in **RL78/G1A Hardware User's Manual (R01UH0305E)**.

(2) Power control register 2 (PC2)

This register is used to enable or disable operation of the gain adjustment amplifier, the low-pass filter, the high-pass filter, the variable output voltage regulator, the reference voltage generator, and the temperature sensor. Use this register to stop unused functions to reduce power consumption and noise.

When using the high-pass filter, be sure to set bit 2 to 1.

Reset signal input clears this register to 00H.

- 80-pin products

Address: 12H After reset: 00H R/W

	7	6	5	4	3	2	1	0
PC2	0	0	0	GAINOF	LPFOF	HPFOF	LDOOF	TEMPOF

HPFOF	Operation of high-pass filter
0	Stop operation of the high-pass filter.
1	Enable operation of the high-pass filter.

Remark Bits 7 to 5 can be set to 1, but this has no effect on the function.

5. 2. 3 AC characteristics

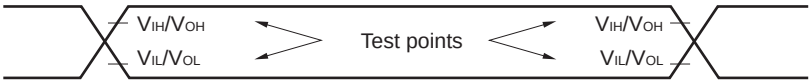
(T_A = –40 to +85°C, 1.6 V ≤ AV_{DD} ≤ 3.6 V, 1.6 V ≤ V_{DD} ≤ 5.5 V, AV_{DD} ≤ V_{DD}, V_{SS} = 0 V)

Parameter	Symbol	Conditions			MIN.	TYP.	MAX.	Unit
Instruction cycle (minimum instruction execution time)	T_{CY}	Main system clock (f_{MAIN}) operation	HS (high-speed main) mode	2.7 V ≤ V_{DD} ≤ 5.5 V	0.03125		1	μs
				2.4 V ≤ V_{DD} < 2.7 V	0.0625		1	μs
			LV (Low-voltage main) mode	1.6 V ≤ V_{DD} ≤ 5.5 V	0.25		1	μs
			LS (Low-speed main) mode	1.8 V ≤ V_{DD} ≤ 5.5 V	0.125		1	μs
		In the self programming mode	HS (high-speed main) mode	2.7 V ≤ V_{DD} ≤ 5.5 V	0.03125		1	μs
				2.4 V ≤ V_{DD} < 2.7 V	0.0625		1	μs
			LV (Low-voltage main) mode	1.8 V ≤ V_{DD} ≤ 5.5 V	0.25		1	μs
			LS (Low-speed main) mode	1.8 V ≤ V_{DD} ≤ 5.5 V	0.125		1	μs
External main system clock frequency	f_{EX}	2.7 V ≤ V_{DD} ≤ 5.5 V			1.0		20.0	MHz
		2.4 V ≤ V_{DD} < 2.7 V			1.0		16.0	
		1.8 V ≤ V_{DD} < 2.4 V			1.0		8.0	
		1.6 V ≤ V_{DD} < 1.8 V			1.0		4.0	
External main system clock input high-level width, low-level width	t_{EXH}, t_{EXL}	2.7 V ≤ V_{DD} ≤ 5.5 V			24			ns
		2.4 V ≤ V_{DD} < 2.7 V			30			
		1.8 V ≤ V_{DD} < 2.4 V			60			
		1.6 V ≤ V_{DD} < 1.8 V			120			
TI00, TI04, TI07 input high/low level width	t_{TIH}, t_{TIL}				1/f_{MCK} + 10			ns
TO00, TO04, TO07 output frequency	f_{TO}	HS (high-speed main) mode		4.0 V ≤ V_{DD} ≤ 5.5 V			16	MHz
				2.7 V ≤ V_{DD} < 4.0 V			8	
				1.8 V ≤ V_{DD} < 2.7 V			4	
				1.6 V ≤ V_{DD} < 1.8 V			2	
		LV (Low-voltage main) mode		1.6 V ≤ V_{DD} < 5.5 V			2	
		LS (Low-speed main) mode		1.8 V ≤ V_{DD} ≤ 5.5 V			4	
				1.6 V ≤ V_{DD} < 1.8 V			2	
PCLBUZ0 output frequency	f_{PCL}	HS (high-speed main) mode		4.0 V ≤ V_{DD} ≤ 5.5 V			16	MHz
				2.7 V ≤ V_{DD} < 4.0 V			8	
				1.8 V ≤ V_{DD} < 2.7 V			4	
				1.6 V ≤ V_{DD} < 1.8 V			2	
		LV (Low-voltage main) mode		1.8 V ≤ V_{DD} ≤ 5.5 V			4	
				1.6 V ≤ V_{DD} < 1.8 V			2	
		LS (Low-speed main) mode		1.8 V ≤ V_{DD} ≤ 5.5 V			4	
				1.6 V ≤ V_{DD} < 1.8 V			2	
Interrupt input high level width, low level width	t_{INIH}, t_{INIL}	INTP0, INTP1, INTP2, INTP6		1.6 V ≤ V_{DD} ≤ 5.5 V	1			μs
<R> Key interrupt input high level width, low level width	t_{KR}	KR0 to KR7		1.8 V ≤ V_{DD} ≤ 5.5 V 1.8 V ≤ AV_{DD} ≤ 3.6 V	250			ns
				1.6 V ≤ V_{DD} < 1.8 V 1.6 V ≤ AV_{DD} < 1.8 V	1			μs
$\overline{\text{RESET}}$ low level width	t_{RSL}				10			μs

Remark f_{MCK}: Timer array unit operation clock frequency. (Operation clock to be set by the timer clock select register 0 (TPS0) and CKS0n bit of timer mode register 0n (TMR0n). n: Channel number (n = 0 to 7))

<R> 5. 2. 4 Peripheral functions characteristics

AC Timing Test Points



<R> 5. 2. 4. 1 Serial array unit

(1) Communication between devices at same potential (UART mode) (dedicated baud rate generator output)

(T_A = –40 to +85°C, 1.6 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions	HS Note 1		LS Note 2		LV Note 3		Unit
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Transfer rate Note 4		2.4 V ≤ V_{DD} ≤ 5.5 V		f_{MCK}/6		f_{MCK}/6		f_{MCK}/6	bps
		Theoretical value of the maximum transfer rate: f_{MCK} = f_{CLK} Note 6		5.3 Note 5		1.3		0.6	Mbps
		1.8 V ≤ V_{DD} ≤ 5.5 V		f_{MCK}/6		f_{MCK}/6		f_{MCK}/6	bps
		Theoretical value of the maximum transfer rate: f_{MCK} = f_{CLK} Note 6		5.3 Note 5		1.3		0.6	Mbps
		1.7 V ≤ V_{DD} ≤ 5.5 V		f_{MCK}/6		f_{MCK}/6		f_{MCK}/6	bps
		Theoretical value of the maximum transfer rate: f_{MCK} = f_{CLK} Note 6		5.3 Note 5		1.3 Note 5		0.6	Mbps
		1.6 V ≤ V_{DD} ≤ 5.5 V		–		f_{MCK}/6		f_{MCK}/6	bps
		Theoretical value of the maximum transfer rate: f_{MCK} = f_{CLK} Note 6		–		1.3 Note 5		0.6	Mbps

Notes 1. HS is condition of HS (high-speed main) mode.

2. LS is condition of LS (low-speed main) mode.

3. LV is condition of LV (low-voltage main) mode.

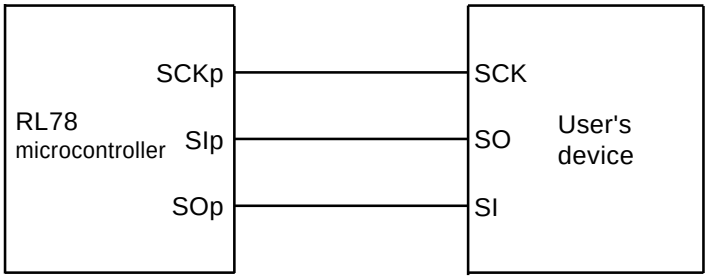
4. Transfer rate in the SNOOZE mode is 4800 bps.

5. The following conditions are required for low voltage interface.
2.4 V ≤ V_{DD} < 2.7 V: 2.6 Mbps max.
1.8 V ≤ V_{DD} < 2.4 V: 1.3 Mbps max.
1.6 V ≤ V_{DD} < 1.8 V: 0.6 Mbps max.

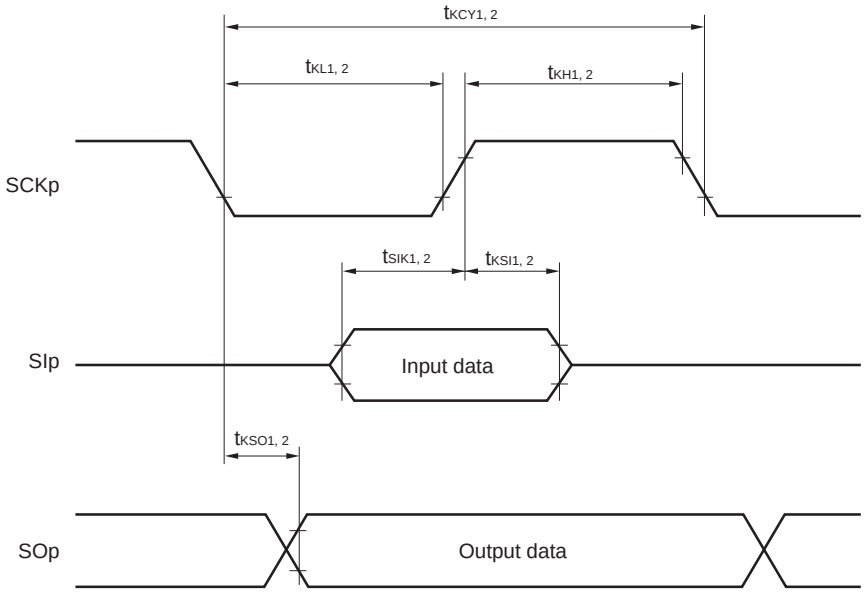
6. f_{CLK} in each operating mode is as below.
HS (high-speed main) mode : f_{CLK} = 32 MHz
LS (low-speed main) mode : f_{CLK} = 8 MHz
LV (low-voltage main) mode : f_{CLK} = 4 MHz

Caution Select the normal input buffer for the RxDq pin and the normal output mode for the TxDq pin by using port input mode register g (PIMg) and port output mode register g (POMg).

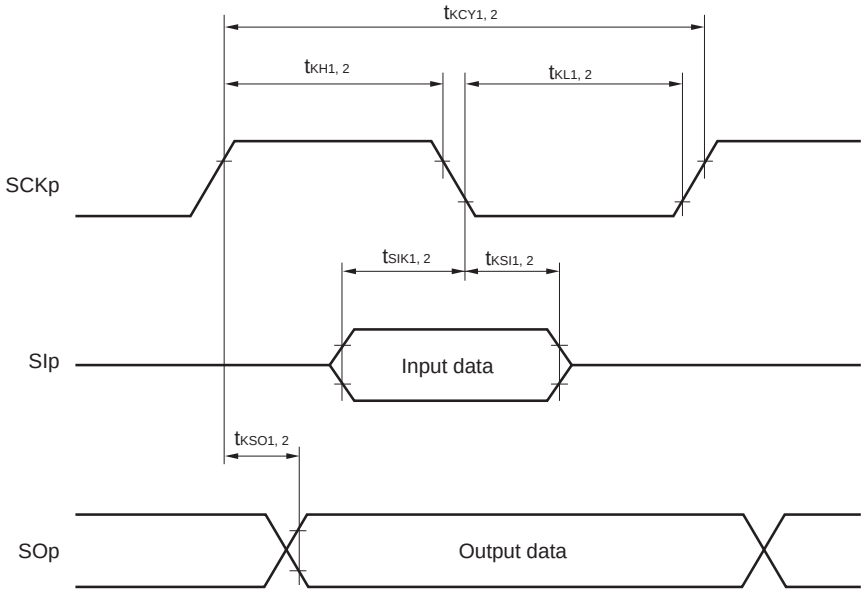
CSI mode connection diagram (during communication between devices with the same voltage)



CSI mode serial transfer timing (during communication between devices with the same voltage)
(when DAPmn = 0 and CKPmn = 0 or DAPmn = 1 and CKPmn = 1)



CSI mode serial transfer timing (during communication between devices with the same voltage)
(when DAPmn = 0 and CKPmn = 1 or DAPmn = 1 and CKPmn = 0)



Remarks 1. p: CSI number (p = 00, 10, 20, 21)

2. m: Unit number, n: Channel number (mn = 00 to 03, 10, 11)

<R> **(8) Communication between devices at different potential (1.8 V, 2.5 V or 3 V) (CSI mode) (master mode, SCKp ... internal clock output) (2/2)**

(T_A = –40 to +85°C, 1.8 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V) (2/2)

Parameter	Symbol	Conditions	HS Note 1		LS Note 2		LV Note 3		Unit
			MIN	MAX	MIN	MAX	MIN	MAX	
SIp setup time (to SCKp↑) Note 4	t_{SIK1}	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ Vb ≤ 4.0 V, Cb = 30 pF, Rb = 1.4 kΩ	81		479		479		ns
		2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ Vb ≤ 2.7 V, Cb = 30 pF, Rb = 2.7 kΩ	177		479		479		ns
		1.8 V ≤ V_{DD} < 3.3 V, 1.6 V ≤ Vb ≤ 2.0 V, Note 6 Cb = 30 pF, Rb = 5.5 kΩ	479		479		479		ns
SIp hold time (from SCKp↑) Note 4	t_{KSI1}	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ Vb ≤ 4.0 V, Cb = 30 pF, Rb = 1.4 kΩ	19		19		19		ns
		2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ Vb ≤ 2.7 V, Cb = 30 pF, Rb = 2.7 kΩ	19		19		19		ns
		1.8 V ≤ V_{DD} < 3.3 V, 1.6 V ≤ Vb ≤ 2.0 V, Note 6 Cb = 30 pF, Rb = 5.5 kΩ	19		19		19		ns
Delay time from SCKp↓ to SOp output Note 4	t_{KSO1}	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ Vb ≤ 4.0 V, Cb = 30 pF, Rb = 1.4 kΩ		100		100		100	ns
		2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ Vb ≤ 2.7 V, Cb = 30 pF, Rb = 2.7 kΩ		195		195		195	ns
		1.8 V ≤ V_{DD} < 3.3 V, 1.6 V ≤ Vb ≤ 2.0 V, Note 6 Cb = 30 pF, Rb = 5.5 kΩ		483		483		483	ns
SIp setup time (to SCKp↓) Note 5	t_{SIK1}	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ Vb ≤ 4.0 V, Cb = 30 pF, Rb = 1.4 kΩ	44		110		110		ns
		2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ Vb ≤ 2.7 V, Cb = 30 pF, Rb = 2.7 kΩ	44		110		110		ns
		1.8 V ≤ V_{DD} < 3.3 V, 1.6 V ≤ Vb ≤ 2.0 V, Note 6 Cb = 30 pF, Rb = 5.5 kΩ	110		110		110		ns
SIp hold time (from SCKp↓) Note 5	t_{KSI1}	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ Vb ≤ 4.0 V, Cb = 30 pF, Rb = 1.4 kΩ	19		19		19		ns
		2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ Vb ≤ 2.7 V, Cb = 30 pF, Rb = 2.7 kΩ	19		19		19		ns
		1.8 V ≤ V_{DD} < 3.3 V, 1.6 V ≤ Vb ≤ 2.0 V, Note 6 Cb = 30 pF, Rb = 5.5 kΩ	19		19		19		ns
Delay time from SCKp↑ to SOp output Note 5	t_{KSO1}	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ Vb ≤ 4.0 V, Cb = 30 pF, Rb = 1.4 kΩ		25		25		25	ns
		2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ Vb ≤ 2.7 V, Cb = 30 pF, Rb = 2.7 kΩ		25		25		25	ns
		1.8 V ≤ V_{DD} < 4.0 V, 1.6 V ≤ Vb ≤ 2.0 V, Note 6 Cb = 30 pF, Rb = 5.5 kΩ		25		25		25	ns

(**Notes**, **Caution** and **Remarks** are listed on the next page.)

<R> (5) When reference voltage (+) = AV_{DD} (ADREFP1 = 0, ADREFP0 = 0), reference voltage (–) = AV_{SS} (ADREFM = 0), target for conversion: ANI16 to ANI18, ANI20 to ANI26, ANI28, and ANI30 (ANI pins that use V_{DD} as their power source), interanal reference voltage, temperature sensor output voltage

(T_A = –40 to +85°C, 1.6 V ≤ V_{DD} ≤ 5.5 V, 1.6 V ≤ AV_{DD} ≤ 3.6 V, AV_{DD} ≤ V_{DD}, V_{SS} = 0 V, AV_{SS} = 0 V, reference voltage (+) = AV_{DD}, reference voltage (–) = AV_{SS} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Resolution	R_{ES}		2.4 V ≤ AV_{DD} ≤ 3.6 V	8		12	bit
			1.8 V ≤ AV_{DD} ≤ 3.6 V	8		10 Note 1	
			1.6 V ≤ AV_{DD} ≤ 3.6 V	8 Note 2			
Overall error Note 3	AINL	12-bit resolution	2.4 V ≤ AV_{DD} ≤ 3.6 V			±8.5	LSB
		10-bit resolution	1.8 V ≤ AV_{DD} ≤ 3.6 V			±6.0	
		8-bit resolution	1.6 V ≤ AV_{DD} ≤ 3.6 V			±3.5	
Conversion time	t_{CONV}	ADTYP = 0, 12-bit resolution	2.4 V ≤ AV_{DD} ≤ 3.6 V	4.125			μs
		ADTYP = 0, 10-bit resolution Note 1	1.8 V ≤ AV_{DD} ≤ 3.6 V	9.5			
		ADTYP = 0, 8-bit resolution Note 2	1.6 V ≤ AV_{DD} ≤ 3.6 V	57.5			
		ADTYP = 1, 8-bit resolution	2.4 V ≤ AV_{DD} ≤ 3.6 V	3.3125			
			1.8 V ≤ AV_{DD} ≤ 3.6 V	7.875			
			1.6 V ≤ AV_{DD} ≤ 3.6 V	54.25			
Zero-scale error Notes 3	EZS	12-bit resolution	2.4 V ≤ AV_{DD} ≤ 3.6 V			±8.0	LSB
		10-bit resolution	1.8 V ≤ AV_{DD} ≤ 3.6 V			±5.5	
		8-bit resolution	1.6 V ≤ AV_{DD} ≤ 3.6 V			±3.0	
Full-scale error Notes 3	EFS	12-bit resolution	2.4 V ≤ AV_{DD} ≤ 3.6 V			±8.0	LSB
		10-bit resolution	1.8 V ≤ AV_{DD} ≤ 3.6 V			±5.5	
		8-bit resolution	1.6 V ≤ AV_{DD} ≤ 3.6 V			±3.0	
Integral linearity error Note 3	ILE	12-bit resolution	2.4 V ≤ AV_{DD} ≤ 3.6 V			±3.5	LSB
		10-bit resolution	1.8 V ≤ AV_{DD} ≤ 3.6 V			±2.5	
		8-bit resolution	1.6 V ≤ AV_{DD} ≤ 3.6 V			±1.5	
Differential linearity error Note 3	DLE	12-bit resolution	2.4 V ≤ AV_{DD} ≤ 3.6 V			±2.5	LSB
		10-bit resolution	1.8 V ≤ AV_{DD} ≤ 3.6 V			±2.5	
		8-bit resolution	1.6 V ≤ AV_{DD} ≤ 3.6 V			±2.0	
Analog input voltage	V_{AIN}			0		AV_{DD} and V_{DD}	V
		Intenal reference voltage (2.4 V ≤ V_{DD} ≤ 5.5 V, HS (high-speed main) mode)		V_{BGR} Note 4			V
		Temperature sensor output voltage (2.4 V ≤ V_{DD} ≤ 5.5 V, HS (high-speed main) mode)		V_{TMPS25} Note 4			V

Notes 1. The lower 2 bits of the ADCR register cannot be used.

2. The lower 4 bits of the ADCR register cannot be used.

3. Excludes quantization error (±1/2 LSB).

4. Refer to **5. 2. 5. 2 Temperature sensor, internal reference voltage output characteristics**.

<R> (6) When reference voltage (+) = internal reference voltage (1.45 V) (ADREFP1 = 1, ADREFP0 = 0), reference voltage (–) = AV_{SS} (ADREFM = 0), target for conversion: ANI0 to ANI4, ANI16 to ANI18, ANI20 to ANI26, ANI28, and ANI30

(T_A = –40 to +85°C, 2.4 V ≤ V_{DD} ≤ 5.5 V, 1.6 V ≤ AV_{DD} ≤ 3.6 V, AV_{DD} ≤ V_{DD}, V_{SS} = 0 V, AV_{SS} = 0 V, reference voltage (+) = internal reference voltage, reference voltage (–) = AV_{SS} = 0 V, HS (high-speed main) mode)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Resolution	R_{ES}			8		bit
Conversion time	t_{CONV}	8-bit resolution	16			μs
Zero-scale error[Notes]	EZS	8-bit resolution			±4.0	LSB
Integral linearity error[Note]	ILE	8-bit resolution			±2.0	LSB
Differential linearity error[Note]	DLE	8-bit resolution			±2.5	LSB
Reference voltage (+)	AV_{REF}(+)	= internal reference voltage (V_{BGR})	1.38	1.45	1.5	V
Analog input voltage	V_{AIN}		0		V_{BGR}	V

Note Excludes quantization error (±1/2 LSB).

5. 2. 5. 5 Supply voltage rise slope characteristics

(T_A = –40 to +85°C, V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Supply voltage rise	SVDD				54	V/ms

Caution Be sure to maintain the internal reset state until V_{DD} reaches the operating voltage range specified in 5. 2. 3 AC Characteristics, by using the LVD circuit or external reset pin.

(-40°C ≤ T_A ≤ 85°C, AV_{DD1} = AV_{DD2} = AV_{DD3} = DV_{DD} = 5.0 V, VREFIN1 = VREFIN2 = VREFIN3 = 1.7 V, AMP1OF = AMP2OF = AMP3OF = 1, DAC1OF = DAC2OF = DAC3OF = 0, inverting amplifier) (2/2)

Parameter	Symbol	Conditions	Ratings			Unit
			MIN	TYP	MAX	
Input conversion offset voltage	VOFF00	CC1, CC0 = 0, 0, T_A = 25°C GCn = 07H (20 dB)	-7	–	7	mV
	VOFF01	CC1, CC0 = 0, 1, T_A = 25°C GCn = 07H (20 dB)	-10	–	10	mV
	VOFF10	CC1, CC0 = 1, 0, T_A = 25°C GCn = 07H (20 dB)	-10	–	10	mV
	VOFF11	CC1, CC0 = 1, 1, T_A = 25°C GCn = 07H (20 dB)	-12	–	12	mV
Input conversion offset voltage temperature coefficient	VOTC		–	±6	–	μV/°C
Slew rate	SR00	CC1, CC0 = 0, 0, CL = 30 pF, GCn = 00H (6 dB)	–	0.68	–	V/μs
	SR01	CC1, CC0 = 0, 1, CL = 30 pF, GCn = 00H (6 dB)	–	0.35	–	V/μs
	SR10	CC1, CC0 = 1, 0, CL = 30 pF, GCn = 00H (6 dB)	–	0.25	–	V/μs
	SR11	CC1, CC0 = 1, 1, CL = 30 pF, GCn = 00H (6 dB)	–	0.09	–	V/μs
Power supply rejection ratio	PSRR00	CC1, CC0 = 0, 0 GCn = 00H (6 dB), f = 1 kHz	–	70	–	dB
	PSRR01	CC1, CC0 = 0, 1 GCn = 00H (6 dB), f = 1 kHz	–	68	–	dB
	PSRR10	CC1, CC0 = 1, 0 GCn = 00H (6 dB), f = 1 kHz	–	62	–	dB
	PSRR11	CC1, CC0 = 1, 1 GCn = 00H (6 dB), f = 1 kHz	–	50	–	dB
Gain setting error	GAIN_Accu1	T_A = 25°C	-0.6	–	0.6	dB
	GAIN_Accu2	T_A = –40 to 85°C	-1.0	–	1.0	dB

Remark n = 1 to 3