Renesas Electronics America Inc - R5F10FMEDFB#YB1 Datasheet

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	RL78
Core Size	16-Bit
Speed	32MHz
Connectivity	CSI, I²C, LINbus, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	26
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	1.6V ~ 5.5V
Data Converters	A/D 17x8/12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	80-LQFP
Supplier Device Package	80-LFQFP (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f10fmedfb-yb1

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2. 5. 5 Port 5 (P50, P51)

(1) Port mode

P50 and P51 function as an I/O port. P50 and P51 can be set to input or output port in 1-bit units using port mode register 5 (PM5).

(2) Control mode

P50 and P51 function as A/D converter analog input, and external interrupt request input.

(a) ANI25, ANI26

These are the analog input pins of A/D converter.

(b) INTP1, INTP2

These are the external interrupt request input pins for which the valid edge (rising edge, falling edge, or both rising and falling edges) can be specified.

3. 3. 2. 4 Special function registers (SFRs)

The differences in special function registers (SFRs) between RL78/G1E (64-pin products, 80-pin products) and RL78/G1A (64-pin products) are shown in the tables below.

(1) 64-pin products

Table 3-1. List of Differences in Special Function Registers (SFRs) (1/4)

Address	RL78/G1E (64-pin products)			RL78/G1A (64-pin products)		
	SFRs Name	Symbol		SFRs Name	Symbol	
FFF00H	Port register 0 Note	P0		Port register 0	P0	
FFF01H	Port register 1 Note	P1		Port register 1	P1	
FFF02H	Port register 2 Note	P2		Port register 2	P2	
FFF03H				Port register 3	P3	
FFF04H	Port register 4 Note	P4		Port register 4	P4	
FFF05H				Port register 5	P5	
FFF06H				Port register 6	P6	
FFF07H	Port register 7 Note	P7		Port register 7	P7	
FFF0CH	Port register 12 Note	P12		Port register 12	P12	
FFF0DH	Same as RL78/G1A (64-pin products)	P13		Port register 13	P13	
FFF0EH				Port register 14	P14	
FFF0FH				Port register 15	P15	
FFF10H	Same as RL78/G1A (64-pin products)	TXD0/ SIO00	SDR00	Serial data register 00	TXD0/ SIO00	SDR00
FFF11H		—			—	
FFF12H	Same as RL78/G1A (64-pin products)	RXD0/ SIO01	SDR01	Serial data register 01	RXD0/ SIO01	SDR01
FFF13H		—			—	
FFF18H	Same as RL78/G1A (64-pin products)	TDR00		Timer data register 00	TDR00	
FFF19H						
FFF1AH	Same as RL78/G1A (64-pin products)	TDR01L	TDR01	Timer data register 01	TDR01L	TDR01
FFF1BH		TDR01H			TDR01H	
FFF1EH	Same as RL78/G1A (64-pin products)	ADCR		12-bit A/D conversion result register	ADCR	
FFF1FH	Same as RL78/G1A (64-pin)	ADCRH		8-bit A/D conversion result register	ADCRH	
FFF20H	Port mode register 0 Note	PM0		Port mode register 0	PM0	
FFF21H	Port mode register 1 Note	PM1		Port mode register 1	PM1	
FFF22H	Port mode register 2 Note	PM2		Port mode register 2	PM2	
FFF23H				Port mode register 3	PM3	
FFF24H	Port mode register 4 Note	PM4		Port mode register 4	PM4	
FFF25H				Port mode register 5	PM5	
FFF26H	Port mode register 6 Note	PM6		Port mode register 6	PM6	
FFF27H	Port mode register 7 Note	PM7		Port mode register 7	PM7	
FFF2CH				Port mode register 12	PM12	
FFF2EH	Port mode register 14 Note	PM14		Port mode register 14	PM14	
FFF2FH	Port mode register 15 Note	PM15		Port mode register 15	PM15	
FFF30H	Same as RL78/G1A (64-pin products)	ADM0		A/D converter mode register 0	ADM0	
FFF31H	Analog input channel specification register Note	ADS		Analog input channel specification register	ADS	
FFF32H	A/D converter mode register 1 Note	ADM1		A/D converter mode register 1	ADM1	

Note The bit setting is different from that of RL78/G1A (64-pin products).

Caution Do not write data to the registers which is in the row with painted gray.

3. 4. 2. 4 Port 3

Port 3 is not available for RL78/G1E.

3. 4. 2. 5 Port 4

Port 4 is an I/O port with an output latch. Port 4 can be set to the input mode or output mode in 1-bit units using port mode register 4 (PM4). When the P40 to P42 pins are used as an input port, use of an on-chip pull-up resistor can be
<R> specified in 1-bit units by pull-up resistor option register 4 (PU4). The P41 pin can be specified as digital input/output or analog input, using port mode control register 4 (PMC4). This port can be also used for A/D converter analog input, data I/O for a flash memory programmer/debugger, and timer I/O. Be sure to connect an external pull-up resistor to the P40 pins when on-chip debugging is enabled to P40 (by using an option byte).

When reset signal is generated, the P40 to P42 pins will be set to input mode.

3. 4. 2. 6 Port 5

Port 5 is an I/O port with an output latch. Port 5 can be set to the input mode or output mode in 1-bit units using port mode register 5 (PM5). When the P50 and P51 pins are used as an input port, use of an on-chip pull-up resistor can be
<R> specified in 1-bit units by pull-up resistor option register 5 (PU5). Output from the P50 pins can be specified as normal CMOS output or N-ch open-drain output (V_{DD} tolerance) in 1-bit units using port output mode register 5 (POM5). The P50 and P51 pins can be specified as digital input/output or analog input in 1-bit units, using port mode control register 5 (PMC5). This port can be also used for A/D converter analog input, and external interrupt request input.

When reset signal is generated, the P50 and P51 pins will be set to input mode.

3. 4. 2. 7 Port 6

Port 6 is not available for RL78/G1E.

3. 4. 2. 8 Port 7

Port 7 is an I/O port with an output latch. Port 7 can be set to the input mode or output mode in 1-bit units using port mode register 7 (PM7). When the P70 to P73 pins are used as an input port, use of an on-chip pull-up resistor can be
<R> specified in 1-bit units by pull-up resistor option register 7 (PU7). The P70 pin can be specified as digital input/output or analog input, using port mode control register 7 (PMC7). This port can be also used for A/D converter analog input, serial interface data I/O, and clock I/O.

When reset signal is generated, the P70 to P73 pins will be set to input mode.

<R> 3. 6. 3. 15 Registers controlling port functions of pins to be used for timer I/O

Using port pins for the timer array unit functions requires setting of the registers that control the port functions multiplexed on the target pins (port mode register (PMxx), port register (Pxx), and port mode control register (PMCxx)). For details, see **3. 4. 3. 1 Port mode registers (PMxx)**, **3. 4. 3. 2 Port registers (Pxx)**, and **3. 4. 3. 6 Port mode control registers (PMCxx)**.

For details of setting example, see **6. 3. 15 Registers controlling port functions of pins to be used for timer I/O** in **RL78/G1A Hardware User's Manual (R01UH0305E)**.

3. 8. 3. 3 Interval timer control register (ITMC)

The bit setting is same as that of RL78/G1A (64-pin products). For details, see **8. 3. 3 Interval timer control register (ITMC)** in **RL78/G1A Hardware User's Manual (R01UH0305E)**.

3. 8. 4 12- bit interval timer operation

See **8. 4 12- bit Interval Timer Operation** in **RL78/G1A Hardware User's Manual (R01UH0305E)**.

<R> **3. 9. 3. 2 Registers controlling port functions of pins to be used for clock or buzzer output**

Using a port pin for clock or buzzer output requires setting of the registers that control the port functions multiplexed on the target pin (port mode register (PMxx), port register (Pxx)). For details, see **3. 4. 3. 1 Port mode registers (PMxx)** and **3. 4. 3. 2 Port registers (Pxx)**.

For details of setting example, see **9. 3. 2 Registers controlling port functions of pins to be used for clock or buzzer output** in **RL78/G1A Hardware User's Manual (R01UH0305E)**.

3. 9. 4 Operations of clock output/buzzer output controller

See **9. 4 Operations of Clock Output/Buzzer Output Controller** in **RL78/G1A Hardware User's Manual (R01UH0305E)**.

3. 9. 5 Cautions of clock output/buzzer output controller

See **9. 5 Cautions of Clock Output/Buzzer Output Controller** in **RL78/G1A Hardware User's Manual (R01UH0305E)**.

3. 12. 2 Configuration of serial array unit

The serial array unit includes the following hardware.

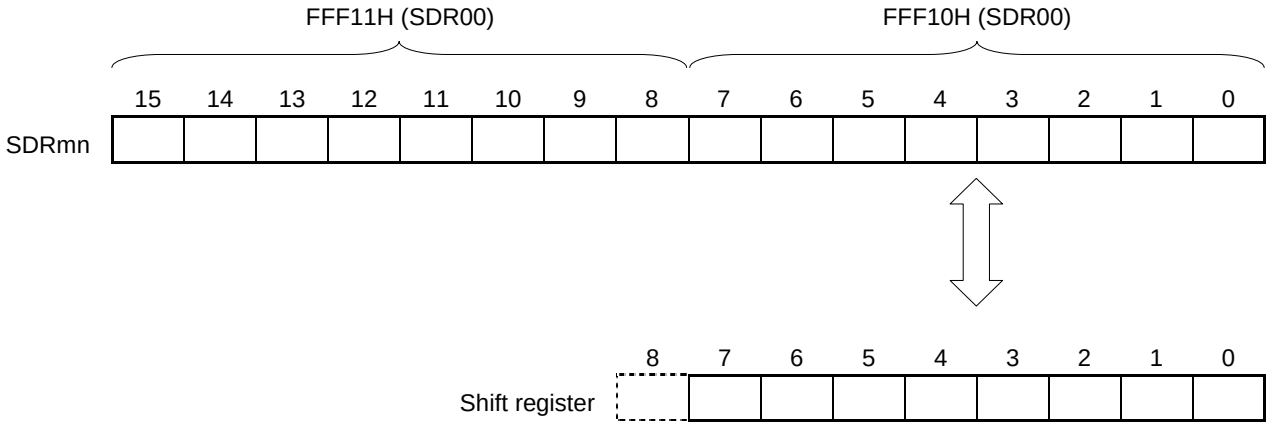
Table 3-12. Configuration of Serial Array Unit

Item	Configuration
Shift register	8 bits or 9 bits[Note 1]
Buffer register	Lower 8 bits or 9 bits of serial data register mn (SDRmn)[Notes 1, 2]
<R> Serial clock I/O	SCK00, SCK10, SCK20, SCK21 pins (for 3-wire serial I/O), SCL00, SCL10, SCL20, SCL21 pins (for simplified I^2C)
Serial data input	SI00, SI10, SI20, SI21 pins (for 3-wire serial I/O), RxD0, RxD1 pins (for UART), RxD2 pin (for UART supporting LIN-bus)
Serial data output	SO00, SO10, SO20, SO21 pins (for 3-wire serial I/O), TxD0, TxD1 pins (for UART), TxD2 pin (for UART supporting LIN-bus), output controller
Serial data I/O	SDA00, SDA10, SDA20 pins (for simplified I^2C)
Control registers	<Registers of unit setting block> • Peripheral enable register 0 (PER0) • Serial clock select register m (SPSm) • Serial channel enable status register m (SEm) • Serial channel start register m (SSm) • Serial channel stop register m (STm) • Serial output enable register m (SOEm) • Serial output register m (SOm) • Serial output level register m (SOLm) • Serial standby control register m (SSCm) • Input switch control register (ISC) • Noise filter enable register 0 (NFEN0)
	<Registers of each channel> • Serial data register mn (SDRmn) • Serial mode register mn (SMRmn) • Serial communication operation setting register mn (SCRmn) • Serial status register mn (SSRmn) • Serial flag clear trigger register mn (SIRmn)
	• Port input mode registers 0, 1 (PIM0, PIM1) • Port output mode registers 0, 1 (POM0, POM1) • Port mode registers 0, 1, 7 (PM0, PM1, PM7) • Port registers 0, 1, 7 (P0, P1, P7)

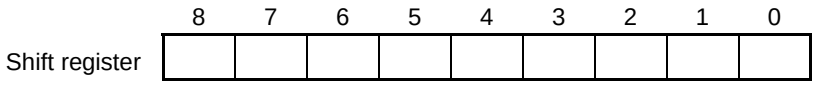
(**Notes** and **Remark** are on the next page.)

<R> **Figure 3-11. Format of Serial Data Register mn (SDRmn) (mn = 00, 01, 02, 03, 10, 11)**

Address: FFF10H, FFF11H (SDR00), FFF12H, FFF13H (SDR01) After reset: 0000H R/W
FFF44H, FFF45H (SDR02), FFF46H, FFF47H (SDR03),
FFF48H, FFF49H (SDR10)Note, FFF4AH, FFF4BH (SDR11)Note



- For 9-bit data communication with UART0 (mn = 00, 01)



Caution For 9-bit data communication, be sure to clear bit 8 of the SDRmn register to "0".

Notes 1. The SCR00, SCR02, and SCR10 registers only.

2. The SCR00 and SCR01 registers only. Others are fixed to 1.

3. 0 is always added regardless of the data contents.

Caution Be sure to clear bits 3, 6, and 11 to "0". (Also clear bit 5 of the SCR01, SCR03, or SCR11 register to 0, as well as bit 1 of the SCR02, SCR03, SCR10, SCR11 registers). Be sure to set bit 2 to "1".

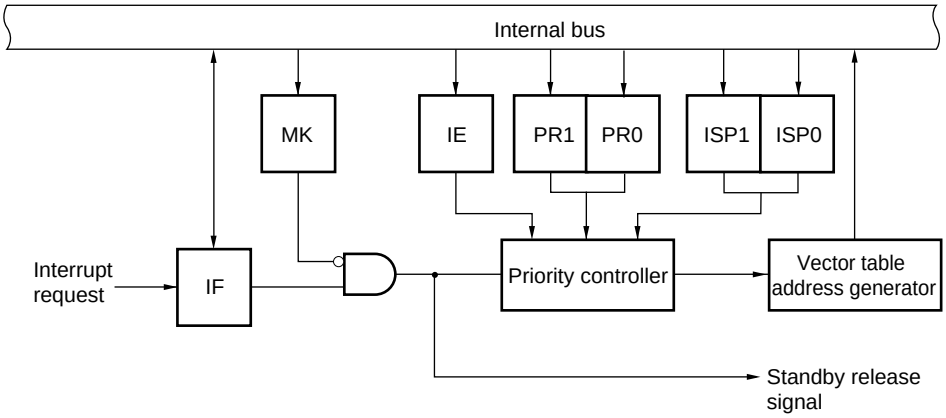
Remark m: Unit number (m = 0, 1)

n: Channel number (n = 0 to 3)

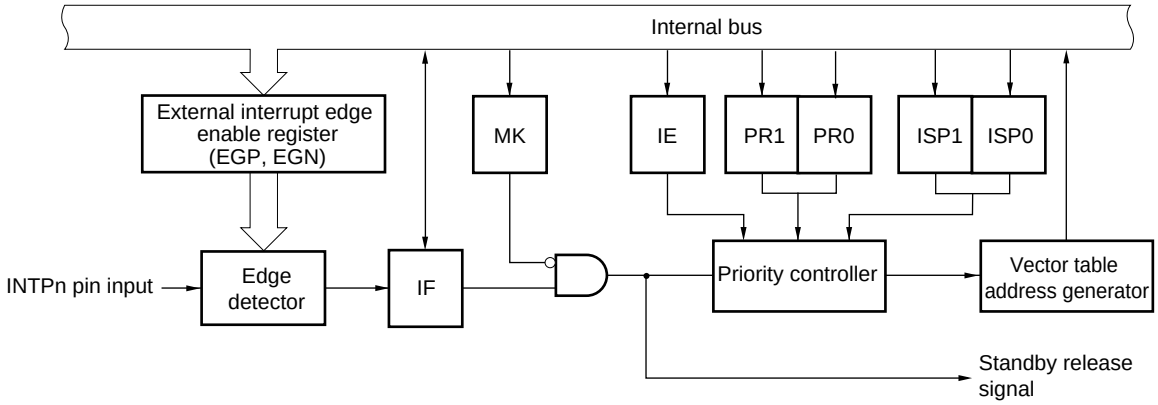
p: CSI number (80-pin products: p = 00, 10, 20, 21 64-pin products: p = 00, 21)

Figure 3-13. Basic Configuration of Interrupt Function (1/2)

(a) Internal maskable interrupt



(b) External maskable interrupt (INTPn)



IF: Interrupt request flag
IE: Interrupt enable flag
ISP0: In-service priority flag 0
ISP1: In-service priority flag 1
MK: Interrupt mask flag
PR0: Priority specification flag 0
PR1: Priority specification flag 1

Remark 64-pin products: n = 0
80-pin products: n = 0 to 3, 6

- 80-pin products

Address: FFFE4H After reset: FFH R/W

Symbol	7	6	5	<4>	<3>	<2>	<1>	<0>
MK0L	1	1	1	PMK2	PMK1	PMK0	LVIMK	WDTIMK

Address: FFFE5H After reset: FFH R/W

Symbol	<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>
MK0H	TMMK01H SREMK0	SRMK0	STMK0 CSIMK00 IICMK00	DMAMK1	DMAMK0	SREMK2	SRMK2 CSIMK21	STMK2 CSIMK20 IICMK20

Address: FFFE6H After reset: FFH R/W

Symbol	<7>	<6>	<5>	<4>	3	<2>	<1>	<0>
MK1L	TMMK03	TMMK02	TMMK01	TMMK00	1	SREMK1 TMMK03H	SRMK1	STMK1 CSIMK10 IICMK10

Address: FFFE7H After reset: FFH R/W

Symbol	<7>	6	5	4	<3>	<2>	1	<0>
MK1H	TMMK04	1	1	1	KRMK	ITMK	1	ADMK

Address: FFFD4H After reset: FFH R/W

Symbol	7	6	5	4	<3>	<2>	<1>	<0>
MK2L	1	1	1	1	PMK6	TMMK07	TMMK06	TMMK05

Address: FFFD5H After reset: FFH R/W

Symbol	<7>	6	<5>	4	3	2	1	0
MK2H	FLMK	1	MDMK	1	1	1	1	1

Cautions 1. Be sure to set bits 5 to 7 of the MK0L register to “1”.

2. Be sure to set bit 3 of the MK1L register to “1”.

3. Be sure to set bits 1 and 4 to 6 of the MK1H register to “1”.

4. Be sure to set bits 4 to 7 of the MK2L register to “1”.

5. Be sure to set bits 0 to 4 and 6 of the MK2H register to “1”.

4. 2. 3 Registers controlling the gain adjustment amplifier

The gain adjustment amplifier is controlled by the following 3 registers:

- MPX setting register 3 (MPX3)
- Gain control register 4 (GC4)
- Power control register 2 (PC2)

(1) MPX setting register 3 (MPX3)

This register is used to control MPX7, MPX9, MPX10, and MPX11.

When selecting the signal to be input to the gain adjustment amplifier, use bits 2 to 0.

Reset signal input clears this register to 00H.

- **64-pin products**

Address: 05H After reset: 00H R/W

	7	6	5	4	3	2	1	0
MPX3	0	0	SCF2	SCF1	0	MPX72	MPX71	MPX70

MPX72	MPX71	MPX70	Source of gain adjustment amplifier input
0	0	0	–
0	0	1	Configurable amplifier Ch1 output signal
0	1	0	Configurable amplifier Ch2 output signal
0	1	1	Configurable amplifier Ch3 output signal
1	0	0	D/A converter Ch4 output signal or VREFIN4 pin
Other than above			Setting prohibited

Caution Be sure to clear bit 3 to "0".

<R> **Remark** Bits 7 and 6 are fixed at 0 of read only.

- **80-pin products**

Address: 05H After reset: 00H R/W

	7	6	5	4	3	2	1	0
MPX3	0	0	SCF2	SCF1	SCF0	MPX72	MPX71	MPX70

MPX72	MPX71	MPX70	Source of gain adjustment amplifier input
0	0	0	GAINAMP_IN pin
0	0	1	Configurable amplifier Ch1 output signal
0	1	0	Configurable amplifier Ch2 output signal
0	1	1	Configurable amplifier Ch3 output signal
1	0	0	D/A converter Ch4 output signal or VREFIN4 pin
Other than above			Setting prohibited

<R> **Remark** Bits 7 and 6 are fixed at 0 of read only.

4. 5 High-Pass Filter

The RL78/G1E (80-pin products) has one on-chip switched-capacitor high-pass filter channel [Note].

Note The high-pass filter is not provided in the RL78/G1E (64-pin products).

4. 5. 1 Overview of high-pass filter features

The features of high-pass filter are described below.

- Butterworth characteristics (Q value = 0.702)
- Cutoff frequency (f_C) range: 8 Hz to 800 Hz
- External input clock frequency (f_{CLK_HPF}) range: $f_C \times 2 / 0.008$ = 2 kHz to 200 kHz
<R> - Includes a power-off function.

And also, the DAC4_OUT output signals can be used as the reference voltage for high-pass filter.

If D/A converter is powered off, the external reference voltage is to be input to DAC4_OUT/VREFIN4 pin.

For details about use of D/A converter, see **4. 3 D/A Converter**.

Remarks 1. The internal control clock (f_S) of the high-pass filter has a duty of 50%, so the external input clock is divided by two at the internal D flip-flop before being used for the low-pass filter. If the internal control clock frequency (f_S) is 100 kHz, therefore, input a 200 kHz clock signal to the CLK_HPF pin.

2. The phase of the signal input to the high-pass filter inverts after passing the high-pass filter.

(T_A = –40 to +85°C, 1.6 V ≤ AV_{DD} ≤ 3.6 V, 1.6 V ≤ V_{DD} ≤ 5.5 V, AV_{DD} ≤ V_{DD}, V_{SS} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Output voltage, low	V_{OL1}	P00 to P04, P10 to P15, P40 to P42, P50, P51, P130, P140	4.0 V ≤ V_{DD} ≤ 5.5 V, I_{OL1} = 20.0 mA			1.5	V
			4.0 V ≤ V_{DD} ≤ 5.5 V, I_{OL1} = 8.5 mA			0.7	V
			2.7 V ≤ V_{DD} ≤ 5.5 V, I_{OL1} = 3.0 mA			0.6	V
			2.7 V ≤ V_{DD} ≤ 5.5 V, I_{OL1} = 1.5 mA			0.4	V
			1.8 V ≤ V_{DD} ≤ 5.5 V, I_{OL1} = 0.6 mA			0.4	V
			1.6 V ≤ V_{DD} < 5.5 V, I_{OL1} = 0.3 mA			0.4	V
	V_{OL2}	P20 to P24	1.6 V ≤ AV_{DD} ≤ 3.6 V, I_{OL2} = 400 μA			0.4	V
	V_{OL4}	P70 to P73	2.7 V ≤ V_{DD} ≤ 5.5 V, I_{OL4} = -3.0 mA			1.0	V
			2.7 V ≤ V_{DD} ≤ 5.5 V, I_{OL4} = -1.5 mA			0.6	V
			1.8 V ≤ V_{DD} ≤ 5.5 V, I_{OL4} = -0.6 mA			0.5	V
			1.6 V ≤ V_{DD} ≤ 5.5 V, I_{OL4} = -0.3 mA			0.5	V

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

<R> **(4) Communication between devices at same potential (CSI mode)**
(slave mode, SCKp ... External clock input) (1/2)

(T_A = –40 to +85°C, 1.6 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V) (1/2)

Parameter	Symbol	Conditions		HS Note 1		LS Note 2		LV Note 3		Unit
				MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
SCKp cycle time Note 4	t_{KCY2}	4.0V ≤ V_{DD} ≤ 5.5V	20MHz < f_{MCK}	8/f_{MCK}		–		–		ns
			f_{MCK} ≤ 20MHz	6/f_{MCK}		6/f_{MCK}		6/f_{MCK}		ns
		2.7V ≤ V_{DD} ≤ 5.5V	16MHz < f_{MCK}	8/f_{MCK}		–		–		ns
			f_{MCK} ≤ 16MHz	6/f_{MCK}		6/f_{MCK}		6/f_{MCK}		ns
		2.4 V ≤ V_{DD} ≤ 5.5 V		6/f_{MCK} and 500ns		6/f_{MCK} and 500ns		6/f_{MCK} and 500ns		ns
		1.8 V ≤ V_{DD} ≤ 5.5 V		6/f_{MCK} and 750ns		6/f_{MCK} and 750ns		6/f_{MCK} and 750ns		ns
		1.7 V ≤ V_{DD} ≤ 5.5 V		6/f_{MCK} and 1500ns		6/f_{MCK} and 1500ns		6/f_{MCK} and 1500ns		ns
		1.6 V ≤ V_{DD} ≤ 5.5 V		–		6/f_{MCK} and 1500ns		6/f_{MCK} and 1500ns		ns
SCKp high-level width low-level width	t_{KH2}, t_{KL2}	4.0 V ≤ V_{DD} ≤ 5.5 V		t_{KCY2}/2 -7		t_{KCY2}/2 -7		t_{KCY2}/2 -7		ns
		2.7 V ≤ V_{DD} ≤ 5.5 V		t_{KCY2}/2 -8		t_{KCY2}/2 -8		t_{KCY2}/2 -8		ns
		1.8 V ≤ V_{DD} ≤ 5.5 V		t_{KCY2}/2 -18		t_{KCY2}/2 -18		t_{KCY2}/2 -18		ns
		1.7 V ≤ V_{DD} ≤ 5.5 V		t_{KCY2}/2 -66		t_{KCY2}/2 -66		t_{KCY2}/2 -66		ns
		1.6 V ≤ V_{DD} ≤ 5.5 V		–		t_{KCY2}/2 -66		t_{KCY2}/2 -66		ns

Notes 1. HS is condition of HS (high-speed main) mode.

2. LS is condition of LS (low-speed main) mode.

3. LV is condition of LV (low-voltage main) mode.

4. Transfer rate in the SNOOZE mode: MAX. 1 Mbps

Caution Select the normal input buffer for the SIp pin and SCKp pin and the normal output mode for the SOp pin by using port input mode register g (PIMg) and port output mode register g (POMg).

Remarks 1. p: CSI number (p = 00, 10, 20, 21), m: Unit number (m = 0, 1), n: Channel number (n = 0 to 2), g: PIM and POM numbers (g = 0, 1)

2. f_{MCK}: Serial array unit operating clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn).
m: Unit number, n: Channel number (mn = 00 to 03, 10, 11))

<R> **(7) Communication between devices at different potential (2.5 V or 3 V) (CSI mode) (master mode, SCKp ... internal clock output corresponding CSI00 only) (2/2)**

(T_A = –40 to +85°C, 2.7 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V) (2/2)

Parameter	Symbol	Conditions	HS Note 1		LS Note 2		LV Note 3		Unit
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
SIp setup time (to SCKp↓) Note 5	t_{SIK1}	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ Vb ≤ 4.0 V, Cb = 20 pF, Rb = 1.4 kΩ	23		110		110		ns
		2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ Vb ≤ 2.7 V, Cb = 20 pF, Rb = 2.7 kΩ	33		110		110		
SIp hold time (from SCKp↓) Note 5	t_{KSI1}	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ Vb ≤ 4.0 V, Cb = 20 pF, Rb = 1.4 kΩ	10		10		10		ns
		2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ Vb ≤ 2.7 V, Cb = 20 pF, Rb = 2.7 kΩ	10		10		10		
Delay time from SCKp↑ to SOp output Note 5	t_{KSO1}	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ Vb ≤ 4.0 V, Cb = 20 pF, Rb = 1.4 kΩ		10		10		10	ns
		2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ Vb ≤ 2.7 V, Cb = 20 pF, Rb = 2.7 kΩ		10		10		10	

Notes 1. HS is condition of HS (high-speed main) mode.

2. LS is condition of LS (low-speed main) mode.

3. LV is condition of LV (low-voltage main) mode.

4. This indicates the time when DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.

5. This indicates the time when DAPmn = 0 and CKPmn = 1 or DAPmn = 1 and CKPmn = 0.

Caution Select the TTL input buffer for the SIp pin and the N-ch open drain output (V_{DD} tolerance) mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V_{IH} and V_{IL}, see the DC characteristics with TTL input buffer selected.

Remarks 1. Rb [Ω]: Communication line (SCKp, SOp) pull-up resistance, Cb [F]: Communication line (SCKp, SOp) load capacitance, Vb [V]: Communication line voltage

2. p: CSI number (p = 00), m: Unit number (m = 0), n: Channel number (n = 0), g: PIM and POM numbers (g = 1)

3. The AC characteristics of serial array units communicating with a device at different potential in CSI mode is observed at V_{IH} and V_{IL} below.

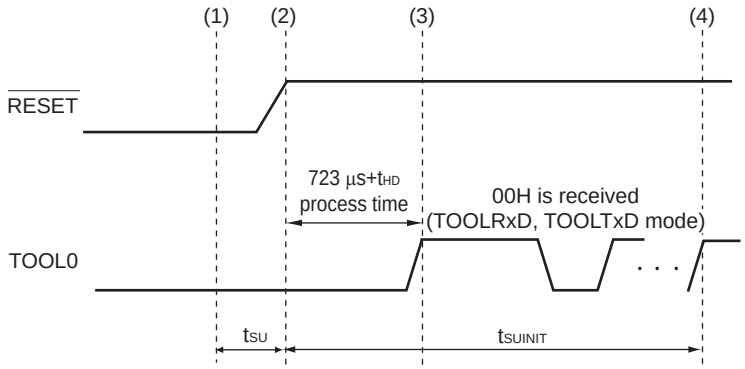
4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ Vb ≤ 4.0 V: V_{IH} = 2.2 V, V_{IL} = 0.8 V

2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ Vb ≤ 2.7 V: V_{IH} = 2.0 V, V_{IL} = 0.5 V

<R> **5. 2. 9 Timing specs for switching flash memory programming modes**

(T_A = –40 to +85°C, 1.8 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
How long from when a external reset ends until the initial communication settings are specified	t_{SUINIT}	POR and LVD resets must end before the external reset ends.			100	ms
How long from when the TOOL0 pin is placed at the low level until a external reset ends	t_{SU}	POR and LVD resets must end before the external reset ends.	10			μs
How long the TOOL0 pin must be kept at the low level after a reset ends (except flash firmware processing time)	t_{HD}	POR and LVD resets must end before the external reset ends.	1			ms



<1> The low level is input to the TOOL0 pin.

<2> The external reset ends (POR and LVD resets must end before the external reset ends.).

<3> The TOOL0 pin is set to the high level.

<4> The flash memory programming mode is set by UART reception and the baud rate setting completes.

Remark t_{SUINIT}: The segment shows that it is necessary to finish specifying the initial communication settings within 100 ms from when the resets end.

t_{SU}: How long from when the TOOL0 pin is placed at the low level until a external reset ends.

t_{HD}: How long to keep the TOOL0 pin at the low level from when the external or internal resets end (except flash firmware processing time).

($-40°C \le T_A \le 85°C$, $AV_{DD1} = AV_{DD2} = AV_{DD3} = DV_{DD} = 5.0$ V, VREFIN1 = VREFIN2 = VREFIN3 = 1.7 V, AMP1OF = AMP2OF = AMP3OF = 1, DAC1OF = DAC2OF = DAC3OF = 0, GC1 = GC2 = 03H, instrumentation amplifier) (1/2)

Parameter	Symbol	Conditions	Ratings			Unit
			MIN	TYP	MAX	
Current consumption	Icc00	AMP1OF = AMP2OF = AMP3OF = 1, CC1, CC0 = 0, 0	–	970	2,150	μA
	Icc01	AMP1OF = AMP2OF = AMP3OF = 1, CC1, CC0 = 0, 1	–	510	1,150	μA
	Icc10	AMP1OF = AMP2OF = AMP3OF = 1, CC1, CC0 = 1, 0	–	350	780	μA
	Icc11	AMP1OF = AMP2OF = AMP3OF = 1, CC1, CC0 = 1, 1	–	140	330	μA
Input voltage	VINL		AGND1 - 0.1	–	–	V
	VINH		–	–	AV_{DD1} - 1.5	V
Output voltage	VOUTL	IOL = -200 μA	–	AGND1 + 0.02	AGND1 + 0.06	V
	VOUTH	IOH = 200 μA	AV_{DD1}- 0.06	AV_{DD1} - 0.02	–	V
Settling time	t_{SET_AMP00}	GC3 = 00H (20 dB), CC1, CC0 = 0, 0, CL = 30 pF, output voltage = $1V_{PP}$, output convergence voltage V_{PP} = 999 mV	–	–	9	μs
	t_{SET_AMP01}	GC3 = 00H (20 dB), CC1, CC0 = 0, 1, CL = 30 pF, output voltage = $1V_{PP}$, output convergence voltage V_{PP} = 999 mV	–	–	18	μs
	t_{SET_AMP10}	GC3 = 00H (20 dB), CC1, CC0 = 1, 0, CL = 30 pF, output voltage = $1V_{PP}$, output convergence voltage V_{PP} = 999 mV	–	–	28	μs
	t_{SET_AMP11}	GC3 = 00H (20 dB), CC1, CC0 = 1, 1, CL = 30 pF, output voltage = $1V_{PP}$, output convergence voltage V_{PP} = 999 mV	–	–	71	μs
Gain bandwidth	GBW00	CL = 30 pF, CC1, CC0 = 0, 0 GC3 = 11H (54 dB)	–	1.82	–	MHz
	GBW01	CL = 30 pF, CC1, CC0 = 0, 1 GC3 = 11H (54 dB)	–	1.03	–	MHz
	GBW10	CL = 30 pF, CC1, CC0 = 1, 0 GC3 = 11H (54 dB)	–	0.69	–	MHz
	GBW11	CL = 30 pF, CC1, CC0 = 1, 1 GC3 = 11H (54 dB)	–	0.22	–	MHz
Equivalent input noise	En00	CC1, CC0 = 0, 0 GC3 = 11H (54 dB) f = 1 kHz	–	90	–	nV/√ Hz
	En01	CC1, CC0 = 0, 1 GC3 = 11H (54 dB) f = 1 kHz	–	119	–	nV/√ Hz
	En10	CC1, CC0 = 1, 0 GC3 = 11H (54 dB) f = 1 kHz	–	150	–	nV/√ Hz
<R>	En11	CC1, CC0 = 1, 1 GC3 = 11H (54 dB) f = 1 kHz	–	260	–	nV/√ Hz

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p.98	Modification of **3. 4. 3. 5 Port output mode register (POMxx)**	(c)
p.98	Modification of **3. 4. 3. 6 Port mode control register (PMCxx)**	(c)
p.101	Addition of **Remark** in **3. 4. 3. 8 Peripheral I/O redirection register (PIOR)**	(c)
p.102	Addition of **3. 4. 4. 4 Handling different potential (1.8 V,2.5 V or 3 V) by using EVDD ≤ VDD**	(c)
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p.105	Modification of **3. 4. 5 Register settings when using alternate function**	(c)
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Remark "Classification" in the above table classifies revisions as follows.

(a): Error correction, (b): Addition/change of specifications, (c): Addition/change of description or note, (d): Addition/change of package, part number, or management division, (e): Addition/change of related documents