Renesas Electronics America Inc - R5F10FMEDFB#YK1 Datasheet

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	RL78
Core Size	16-Bit
Speed	32MHz
Connectivity	CSI, I²C, LINbus, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	26
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	1.6V ~ 5.5V
Data Converters	A/D 17x8/12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	80-LQFP
Supplier Device Package	80-LFQFP (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f10fmedfb-yk1

How to Read This Manual

It is assumed that the readers of this manual have general knowledge of electrical engineering, logic circuits, and microcontrollers.

- To gain a general understanding of functions:
  → Read this manual in the order of the **CONTENTS**. The mark "<R>" shows major revised points. The revised points can be easily searched by copying an "<R>" in the PDF file and specifying it in the "Find what:" field.

- How to interpret the register format:
  → For a bit number enclosed in angle brackets, the bit name is defined as a reserved word in the assembler, and is defined as an sfr variable using the #pragma sfr directive in the compiler.

- To know details of the microcontroller block:
  →Refer to the separate document **RL78/G1A Hardware User's Manual (R01UH0305E)**.

- To know details of the RL78 microcontroller instructions:
  → Refer to the separate document **RL78 family User's Manual Software (R01US0015E)**.

Conventions

Data significance:	Higher digits on the left and lower digits on the right	
Active low representations:	$\overline{\times\times\times}$ (overscore over pin and signal name)	
Note:	Footnote for item marked with **Note** in the text	
Caution:	Information requiring particular attention	
Remark:	Supplementary information	
Numerical representations:	Binary	···×××× or ××××B
	Decimal	···××××
	Hexadecimal	···××××H

(2/2)

<R>	P121	2-2-1	Input	Input port	X1	Port 12. 2-bit input port.
	P122				X2/EXCLK	
	P130	1-1-1	Output	Output port	–	Port 13. 1-bit output port and 1-bit input port.
	P137	2-1-2	Input	Input port	INTP0	
	RESET	2-1-1	Input	–	–	Input only pin for external reset. When external reset is not used, connect this pin to V_{DD} directly or via a resistor.

(2/2)

<R>

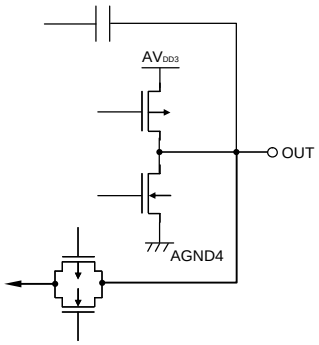
Pin Name	I/O	Recommended Connection of Unused Pins
SC_IN	Input	Connect to AGND4.
CLK_SYNCH	Input	Leave open
SYNCH_OUT	Output	
GAINAMP_OUT	Output	
GAINAMP_IN	Input	Connect to AGND2.
MPXIN61	Input	Connect to AGND1.
MPXIN51	Input	
MPXIN60	Input	
MPXIN50	Input	
AMP3_OUT	Output	Leave open
DAC3_OUT/ VREFIN3	I/O	Leave open
AMP2_OUT	Output	Leave open
AMP1_OUT	Output	Connect to AGND1.
DAC2_OUT/ VREFIN2	I/O	Leave open
DAC1_OUT/VREFIN1	I/O	
MPXIN41	Input	Connect to AGND1.
MPXIN31	Input	
MPXIN40	Input	
MPXIN30	Input	
MPXIN21	Input	
MPXIN11	Input	
MPXIN20	Input	
MPXIN10	Input	
TEMP_OUT	Output	Leave open
$\overline{\text{SCLK}}$	Input	
SDO	Output	
SDI	Input	
$\overline{\text{CS}}$	Input	
DAC4_OUT/ VREFIN4	I/O	
HPF_OUT	Output	
CLK_HPF	Input	
CLK_LPF	Input	
LPF_OUT	Output	
LDO_OUT	Output	
BGR_OUT	Output	
I.C	–	
$\overline{\text{ARESET}}$	Input	– Note

<R> **Note** When the resource pin for $\overline{\text{ARESET}}$ is to be Hi-Z, connect $\overline{\text{ARESET}}$ to DGND via a resistor.
For details of functions, see **2. 5. 31 $\overline{\text{ARESET}}$**.

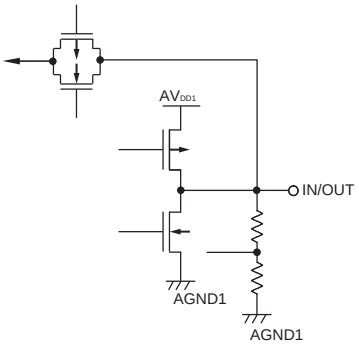
Figure 2-13. Pin I/O Circuit List (1/2)

<R>

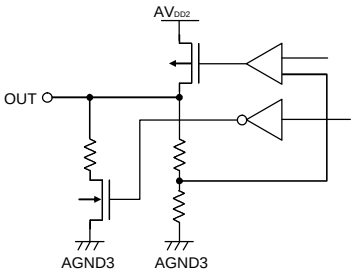
ANALOG1



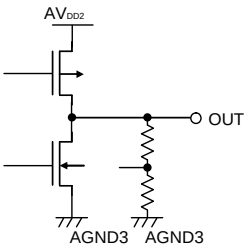
ANALOG2



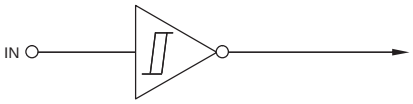
ANALOG3



ANALOG4

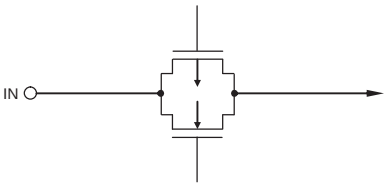


ANALOG5

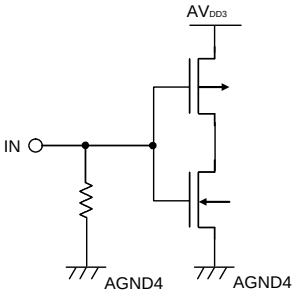


Schmitt-triggered input with hysteresis characteristics

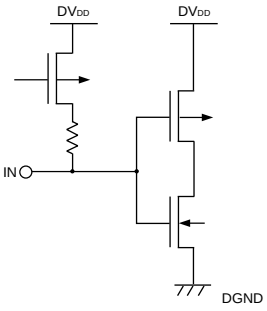
ANALOG6



ANALOG7



ANALOG8



CHAPTER 3 MICROCONTROLLER BLOCK

3. 1 Outline of This Chapter

The 16-bit microcontroller block in the RL78/G1E corresponds to the RL78/G1A (64-pin products). For the details of each function in microcontroller block, see the **RL78/G1A Hardware User's Manual (R01UH0305E)**.

Not all of the functions of the RL78/G1A are available to be used in the RL78/G1E package because not all pins of function are drawn out of the package. In this chapter, the differences in functions and registers between the RL78/G1A and the RL78/G1E are described.

3. 4. 3. 5 Port output mode register (POMxx)

(1) 64-pin products

Symbol	7	6	5	4	3	2	1	0	Address	After Reset	R/W
POM0	0	0	0	0	POM03	POM02	0	0	F0050H	00H	R/W
POM1	0	0	0	POM14	POM13	POM12	POM11	POM10	F0051H	00H	R/W

<R> **Caution Be sure to clear bits 0, 1 and 4 to 7 of the POM0 register, and bits 5 to 7 of the POM1 register to "0".**

<R> **(2) 80-pin products**

Symbol	7	6	5	4	3	2	1	0	Address	After Reset	R/W
POM0	0	0	0	POM04	POM03	POM02	0	0	F0050H	00H	R/W
POM1	0	0	POM15	POM14	POM13	POM12	POM11	POM10	F0051H	00H	R/W
POM5	0	0	0	0	0	0	0	POM50	F0055H	00H	R/W

Caution Be sure to clear bits 0, 1 and 5 to 7 of the POM0 register, bits 6 and 7 of the POM1 register, and bits 1 to 7 of the POM5 register to "0".

3. 4. 3. 6 Port mode control register (PMCxx)

<R> **(1) 64-pin products**

Symbol	7	6	5	4	3	2	1	0	Address	After Reset	R/W
PMC0	1	1	1	1	PMC03	PMC02	1	1	F0060H	FFH	R/W
PMC1	1	1	1	PMC14	PMC13	PMC12	PMC11	PMC10	F0061H	FFH	R/W
PMC4	1	1	1	1	1	1	PMC41	1	F0064H	FFH	R/W
PMC7	1	1	1	1	1	1	1	PMC70	F0067H	FFH	R/W

Caution Be sure to set bits 0, 1 and 4 to 7 of the PMC0 register, bits 5 to 7 of the PMC1 register, bits 0 and 2 to 7 of the PMC4 register, and bits 1 to 7 of the PMC7 register to "0".

<R> **(2) 80-pin products**

Symbol	7	6	5	4	3	2	1	0	Address	After Reset	R/W
PMC0	1	1	1	1	PMC03	PMC02	1	1	F0060H	FFH	R/W
PMC1	1	1	PMC15	PMC14	PMC13	PMC12	PMC11	PMC10	F0061H	FFH	R/W
PMC4	1	1	1	1	1	1	PMC41	1	F0064H	FFH	R/W
PMC5	1	1	1	1	1	1	PMC51	PMC50	F0065H	FFH	R/W
PMC7	1	1	1	1	1	1	1	PMC70	F0067H	FFH	R/W

Caution Be sure to set bits 0, 1 and 4 to 7 of the PMC0 register, bits 6 and 7 of the PMC1 register, bits 0 and 2 to 7 of the PMC4 register, bits 2 to 7 of the PMC5 register, and bits 1 to 7 of the PMC7 register to "0".

3. 6. 1. 4 LIN-bus supporting function (channel 7 of unit 0 only)

Timer array unit is used to check whether signals received in LIN-bus communication match the LIN-bus communication format.

<1> Detection of wakeup signal

The timer starts counting at the falling edge of a signal input to the serial data input pin (RxD2) of UART2 and the count value of the timer is captured at the rising edge. In this way, a low-level width can be measured. If the low-level width is greater than a specific value, it is recognized as a wakeup signal.

<2> Detection of break field

The timer starts counting at the falling edge of a signal input to the serial data input pin (RxD2) of UART2 after a wakeup signal is detected, and the count value of the timer is captured at the rising edge. In this way, a low-level width is measured. If the low-level width is greater than a specific value, it is recognized as a break field.

<3> Measurement of pulse width of sync field

After a break field is detected, the low-level width and high-level width of the signal input to the serial data input pin (RxD2) of UART2 are measured. From the bit interval of the sync field measured in this way, a baud rate is calculated.

Remark For details about setting up the operations used to implement the LIN-bus, see **3. 6. 3. 13 Input switch control register (ISC)** and **3. 6. 8 Independent channel operation function of timer array unit.**

3. 6. 2. 1 Timer count register mn (TCRmn)

The bit setting is same as that of RL78/G1A (64-pin products). For details, see **6. 2. 1 Timer count register mn (TCRmn)** in **RL78/G1A Hardware User's Manual (R01UH0305E)**.

3. 6. 2. 2 Timer data register mn (TDRmn)

The bit setting is same as that of RL78/G1A (64-pin products). For details, see **6. 2. 2 Timer data register mn (TDRmn)** in **RL78/G1A Hardware User's Manual (R01UH0305E)**.

3. 11. 3. 8 Conversion result comparison upper limit setting register (ADUL)

The bit setting is same as that of RL78/G1A (64-pin products). For details, see **11. 3. 8 Conversion result comparison upper limit setting register (ADUL)** in **RL78/G1A Hardware User's Manual (R01UH0305E)**.

3. 11. 3. 9 Conversion result comparison lower limit setting register (ADLL)

The bit setting is same as that of RL78/G1A (64-pin products). For details, see **11. 3. 9 Conversion result comparison lower limit setting register (ADLL)** in **RL78/G1A Hardware User's Manual (R01UH0305E)**.

3. 11. 3. 10 A/D test register (ADTES)

The bit setting is same as that of RL78/G1A (64-pin products). For details, see **11. 3. 10 A/D test register (ADTES)** in **RL78/G1A Hardware User's Manual (R01UH0305E)**.

<R> 3. 11. 3. 11 Registers controlling port function of analog input pins

Set up the registers for controlling the functions of the ports shared with the analog input pins of the A/D converter (port mode registers (PMxx), port mode control registers (PMCxx), and A/D port configuration register (ADPC)).

For details, see as follows.

- **3. 4. 3. 1 Port mode registers (PMxx)**
- **3. 4. 3. 6 Port mode control registers (PMCxx)**
- **3. 4. 3. 7 A/D port configuration register (ADPC)**

For details of setting example, see **11. 3. 11 Registers controlling port function of analog input pins** in **RL78/G1A Hardware User's Manual (R01UH0305E)**.

3. 12. 1. 3 Simplified I²C (IIC00, IIC10, IIC20)

This is a clocked communication function to communicate with two or more devices by using two lines: serial clock (SCL) and serial data (SDA). This simplified I²C is designed for single communication with a device such as EEPROM, flash memory, or A/D converter, and therefore, it functions only as a master.

Make sure by using software, as well as operating the control registers, that the AC specifications of the start and stop conditions are observed.

For details about the settings, see **3. 12. 8 Operation of simplified I²C (IIC00, IIC10, IIC20)**.

[Data transmission/reception]

- Master transmission, master reception (only master function with a single master)
- ACK output function Note and ACK detection function
- Data length of 8 bits

(When an address is transmitted, the address is specified by the higher 7 bits, and the least significant bit is used for R/W control.)

- Manual generation of start condition and stop condition

[Interrupt function]

- Transfer end interrupt

[Error detection flag]

- Parity error (ACK error), or overrun error

[Functions not supported by simplified I²C]

- Slave transmission, slave reception
- Arbitration loss detection function
- Wait detection functions

Note When receiving the last data, ACK will not be output if 0 is written to the SOEmn bit (serial output enable register m (SOEm)) and serial communication data output is stopped. For details, see **3. 12. 8 Operation of simplified I²C (IIC00, IIC10, IIC20)**.

- Setting of serial mode register mn (SMRmn) (2/2)

<R> Address: F0110H, F0111H (SMR00) - F0116H, F0117H (SMR03), After reset: 0020H R/W
F0150H, F0151H (SMR10), F0152H, F0153H (SMR11)

Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SMRmn	CKS mn	CCS mn	0	0	0	0	0	STS mn[Note]	0	SIS mn0[Note]	1	0	0	MD mn2	MD mn1	MD mn0

SISmn0[Note]	Controls inversion of level of receive data of channel n in UART mode
0	Falling edge is detected as the start bit. The input communication data is captured as is.
1	Rising edge is detected as the start bit. The input communication data is inverted and captured.

MDmn2	MDmn1	Setting of operation mode of channel n
0	0	CSI mode
0	1	UART mode
1	0	Simplified I^2C mode
1	1	Setting prohibited

MDmn0	Selection of interrupt source of channel n
0	Transfer end interrupt
1	Buffer empty interrupt (Occurs when data is transferred from the SDRmn register to the shift register.)
For successive transmission, the next transmit data is written by setting the MDmn0 bit to 1 when SDRmn data has run out.	

Note The SMR01, SMR03, and SMR11 registers only.

Caution Be sure to clear bits 13 to 9, 7, 4, and 3 (or bits 13 to 6, 4, and 3 for the SMR00, SMR02, or SMR10 register) to "0". Be sure to set bit 5 to "1".

Remark m: Unit number (m = 0, 1)
n: Channel number (n = 0 to 3)
p: CSI number (80-pin products: p = 00, 10, 20, 21 64-pin products: p = 00, 21)
q: UART number (q = 0 to 2)
r: IIC number (80-pin products: r = 00, 10, 20 64-pin products: r = 00)

Format of User Option Byte (000C1H/010C1H) (1/2)

Address: 000C1H/010C1H[Note]

7	6	5	4	3	2	1	0
VPOC2	VPOC1	VPOC0	1	LVIS1	LVIS0	LVIMDS1	LVIMDS0

- LVD setting (interrupt & reset mode)

<R>

Detection voltage			Option byte setting value						
V_{LVDH}		V_{LVDL}	VPOC2	VPOC1	VPOC0	LVIS1	LVIS0	Mode setting	
Rising edge	Falling edge	Falling edge						LVIMDS1	LVIMDS0
3.13	3.06	1.84	0	0	1	0	0	1	0
3.75	3.67	2.45	0	1	0	0	0		
4.06	3.98	2.75	0	1	1	0	0		
–			Value other than above is setting prohibited.						

- LVD setting (reset mode)

<R>

Detection voltage		Option byte setting value						
V_{LVDH}		VPOC2	VPOC1	VPOC0	LVIS1	LVIS0	Mode setting	
Rising edge	Falling edge						LVIMDS1	LVIMDS0
3.13	3.06	0	0	1	0	0	1	1
3.75	3.67	0	1	0	0	0		
4.06	3.98	0	1	1	0	0		
–		Value other than above is setting prohibited.						

Note Set the same value as 000C1H to 010C1H when the boot swap operation is used because 000C1H is replaced by 010C1H.

<R> **Remarks 1.** For details on the LVD circuit, see **3. 21 Voltage Detector**.

2. The detection voltage is a TYP. value. For details, see **5. 2. 5. 4 LVD circuit characteristics.**

(**Cautions** are listed on the next page.)

(7) Gain control register 3 (GC3)

This register is used to specify the gain and feedback resistance of configurable amplifier Ch3.

The value to specify depends on the configuration of configurable amplifier Ch3.

When using configurable amplifiers Ch1 to Ch3 together as an instrumentation amplifier, be sure to set gain control register 1 (GC1) and gain control register 2 (GC2) to 03H, respectively.

Reset signal input clears this register to 00H.

Address: 08H After reset: 00H R/W

	7	6	5	4	3	2	1	0
GC3	0	0	0	AMPG34	AMPG33	AMPG32	AMPG31	AMPG30

Table 4-7. Gain of Configurable Amplifier Ch3 (Non-Inverting Amplifier)

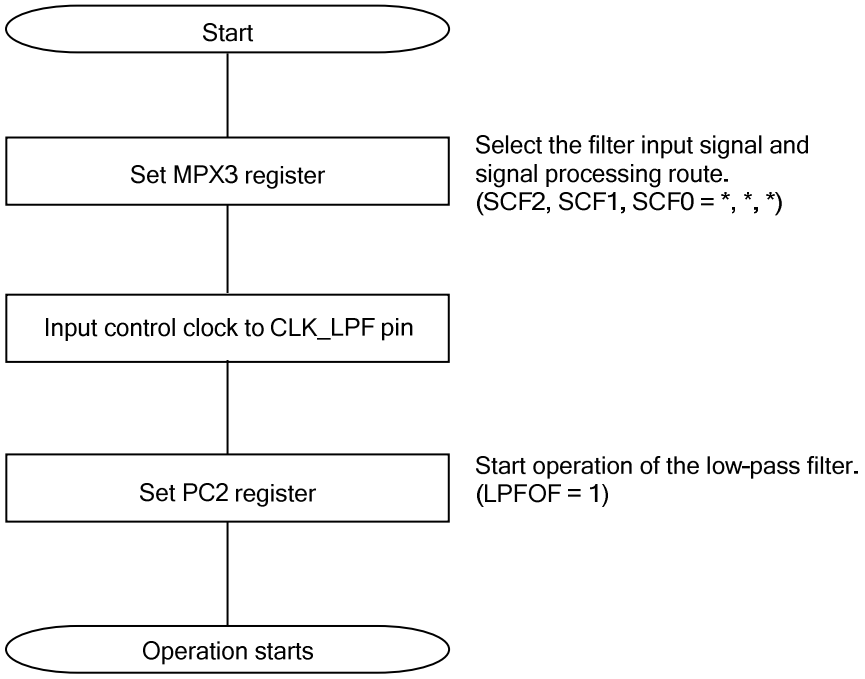
AMPG34	AMPG33	AMPG32	AMPG31	AMPG30	Gain of Configurable Amplifier Ch3 (Typ.)
0	0	0	0	0	9.5 dB
0	0	0	0	1	10.9 dB
0	0	0	1	0	12.4 dB
0	0	0	1	1	14.0 dB
0	0	1	0	0	15.6 dB
0	0	1	0	1	17.3 dB
0	0	1	1	0	19.0 dB
0	0	1	1	1	20.8 dB
0	1	0	0	0	22.7 dB
0	1	0	0	1	24.5 dB
0	1	0	1	0	26.4 dB
0	1	0	1	1	28.3 dB
0	1	1	0	0	30.3 dB
0	1	1	0	1	32.2 dB
0	1	1	1	0	34.2 dB
0	1	1	1	1	36.1 dB
1	0	0	0	0	38.1 dB
1	0	0	0	1	40.1 dB
Other than above					Setting prohibited

<R> **Remark** Bits 7 to 5 are fixed at 0 of read only.

4. 4. 4 Procedure for operating the low-pass filter

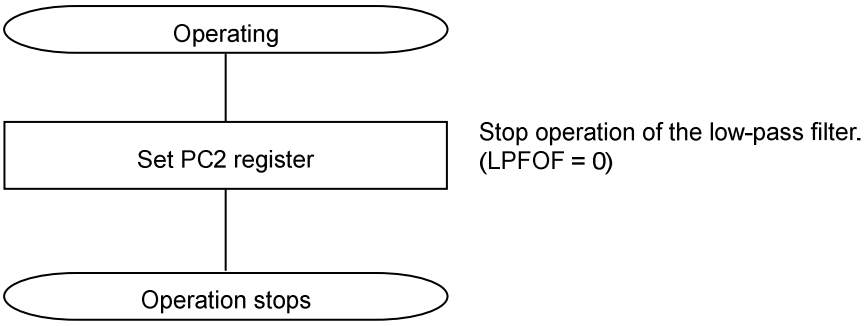
Follow the procedures below to start and stop the low-pass filter.

Example of procedure for starting the low-pass filter



Remark *: don't care

Example of procedure for stopping the low-pass filter



4. 7. 3 Registers controlling the variable output voltage regulator

The variable output voltage regulator is controlled by the following 2 registers:

- LDO control register (LDOC)
- Power control register 2 (PC2)

(1) LDO control register (LDOC)

This register is used to specify the output voltage of the variable output voltage regulator.

Reset signal input sets this register to 0DH.

Address: 0BH After reset: 0DH R/W

	7	6	5	4	3	2	1	0
LDOC	0	0	0	0	LDO3	LDO2	LDO1	LDO0

LDO3	LDO2	LDO1	LDO0	Output Voltage of Variable Output Voltage Regulator (Typ.)
0	0	0	0	2.0 V
0	0	0	1	2.1 V
0	0	1	0	2.2 V
0	0	1	1	2.3 V
0	1	0	0	2.4 V
0	1	0	1	2.5 V
0	1	1	0	2.6 V
0	1	1	1	2.7 V
1	0	0	0	2.8 V
1	0	0	1	2.9 V
1	0	1	0	3.0 V
1	0	1	1	3.1 V
1	1	0	0	3.2 V
1	1	0	1	3.3 V Note
Other than above				Setting prohibited

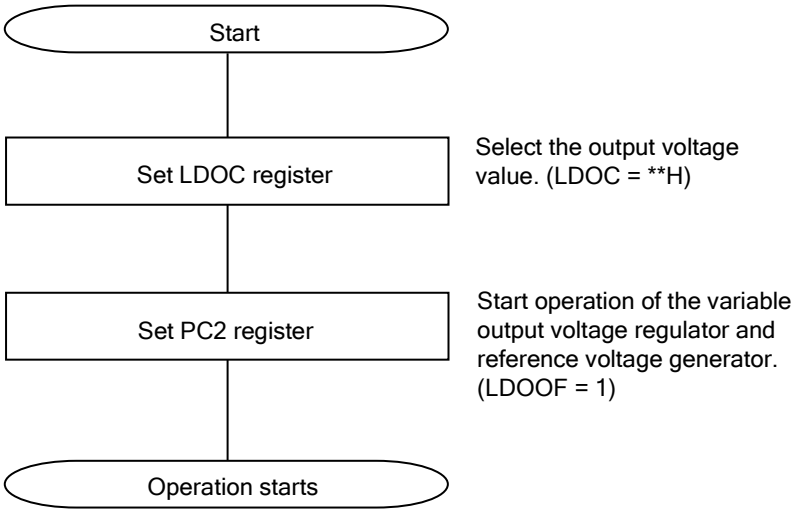
Note Output voltage of 3.3 V is available when the power supply voltage is more than 4 V.

<R> **Remark** Bits 7 to 4 are fixed at 0 of read only.

4. 7. 4 Procedure for operating the variable output voltage regulator

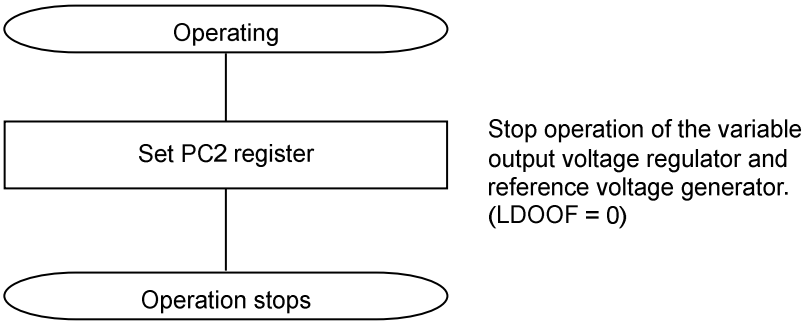
Follow the procedures below to start and stop the variable output voltage regulator and reference voltage generator.

Example of procedure for starting the variable output voltage regulator and reference voltage generator



Remark *: don't care

Example of procedure for stopping the variable output voltage regulator and reference voltage generator



4. 10. 2 Registers controlling the analog reset

(1) Reset control register (RC)

This register is used to control the reset feature in the analog block.

<R> An internal reset can be generated by writing 1 to the RESET bit. The reset control register (RC) is not initialized by generating internal reset of the reset control register, but it can be done by generating external reset from $\overline{\text{ARESET}}$ pin. External reset from $\overline{\text{ARESET}}$ pin clears this register to 00H.

Address: 13H After reset: 00H Note R/W

	7	6	5	4	3	2	1	0
RC	0	0	0	0	0	0	0	RESET

RESET	Reset request by internal reset signal
0	Do not make a reset request by using the internal reset signal, or cancel the reset.
1	Make a reset request by using the internal reset signal, or the reset signal is currently being input.

<R> **Note** The reset control register is not initialized by generating internal reset of the reset control register, but it can be done to 00H by generating external reset from $\overline{\text{ARESET}}$ pin or by writing 0 to the RESET bit of the reset control register (RC).

Caution When the RESET bit is 1, writing to any register other than the reset control register (RC) is ignored. Initializing the reset control register (RC) to 00H by external reset, or writing 0 to the RESET bit enables writing to all the registers.

<R> **Remark** Bits 7 to 1 are fixed at 0 of read only.

<R> **(9) Communication between devices at different potential (1.8 V, 2.5 V or 3 V) (CSI mode) (slave mode, SCKp ... External clock input) (2/2)**

(T_A = –40 to +85°C, 1.8 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V) (2/2)

Parameter	Symbol	Conditions	HS Note 1		LS Note 2		LV Note 3		Unit
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
SCKp high-level width SCKp low-level width	t_{KH2}, t_{KL2}	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ Vb ≤ 4.0 V	t_{KCY2}/2 -12		t_{KCY2}/2 -50		t_{KCY2}/2 -50		ns
		2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ Vb ≤ 2.7 V	t_{KCY2}/2 -18		t_{KCY2}/2 -50		t_{KCY2}/2 -50		ns
		1.8 V ≤ V_{DD} < 3.3 V, 1.6 V ≤ Vb ≤ 2.0 V Note 4	t_{KCY2}/2 -50		t_{KCY2}/2 -50		t_{KCY2}/2 -50		ns
SIp setup time (to SCKp↑) Note 5	t_{SIK2}	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ Vb ≤ 4.0 V	1/f_{MCK} +20		1/f_{MCK} +30		1/f_{MCK} +30		ns
		2.7 V ≤ V_{DD} ≤ 4.0 V, 2.3 V ≤ Vb ≤ 2.7 V	1/f_{MCK} +20		1/f_{MCK} +30		1/f_{MCK} +30		ns
		1.8 V ≤ V_{DD} < 3.3 V, 1.6 V ≤ Vb ≤ 2.0 V Note 4	1/f_{MCK} +30		1/f_{MCK} +30		1/f_{MCK} +30		ns
SIp hold time (from SCKp↑) Note 5	t_{KSI2}		1/f_{MCK} +31		1/f_{MCK} +31		1/f_{MCK} +31		ns
Delay time from SCKp↓ to SOp output Note 6	t_{KSO2}	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ Vb ≤ 4.0 V, Cb = 30 pF, Rb = 1.4 kΩ		2/f_{MCK} +120		2/f_{MCK} +573		2/f_{MCK} +573	ns
		2.7 V ≤ V_{DD} ≤ 4.0 V, 2.3 V ≤ Vb ≤ 2.7 V, Cb = 30 pF, Rb = 2.7 kΩ		2/f_{MCK} +214		2/f_{MCK} +573		2/f_{MCK} +573	ns
		1.8 V ≤ V_{DD} < 3.3 V, 1.6 V ≤ Vb ≤ 2.0 V Note 4, Cb = 30 pF, Rb = 5.5 kΩ		2/f_{MCK} +573		2/f_{MCK} +573		2/f_{MCK} +573	ns

Notes 1. HS is condition of HS (high-speed main) mode.

2. LS is condition of LS (low-speed main) mode.

3. LV is condition of LV (low-voltage main) mode.

4. Specify a value so as to satisfy V_{DD} ≥ Vb.

5. This indicates the time when DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. When DAPmn = 0 and CKPmn = 1 or DAPmn = 1 and CKPmn = 0, this specification refers to SCKp↓.

6. This indicates the time when DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. When DAPmn = 0 and CKPmn = 1 or DAPmn = 1 and CKPmn = 0, this specification refers to SCKp↑.

Caution Select the TTL input buffer for the SIp pin and SCKp pin and the N-ch open drain output (V_{DD} tolerance) mode for the SOp pin by using port input mode register g (PIMg) and port output mode register g (POMg).For V_{IH} and V_{IL}, see the DC characteristics with TTL input buffer selected.

(**Remarks** are listed on the next page.)

5. 3 Electrical Specifications of Analog Block

<R> 5. 3. 1 Operating conditions of analog block

Parameter	Symbol	Conditions	Ratings			Unit
			MIN	TYP.	MAX.	
Power supply voltage range	V_{DDOP}	AV_{DD1}, AV_{DD2}, AV_{DD3}, DV_{DD}	3.0	–	5.5	V

(2) 80-pin products

(–40°C ≤ T_A ≤ 85°C, AV_{DD1} = AV_{DD2} = AV_{DD3} = DV_{DD} = 5.0 V, VREFIN4 = 1.7 V, GAINOF = 1, DAC4OF = 0)

Parameter	Symbol	Conditions	Ratings			Unit
			MIN	TYP	MAX	
Current consumption	IccA		–	530	1,300	μA
Input voltage	VINL		AGND2 - 0.1	–	–	V
	VINH		–	–	AV_{DD1} - 0.05	V
Output voltage	VOUTL1	IOL = -100 μA, GAINAMP_OUT pin	–	AGND2 + 0.02	AGND2 + 0.05	V
	VOUTH1	IOH = 100 μA, GAINAMP_OUT pin	AV_{DD1} - 0.05	AV_{DD1} - 0.02	–	V
	VOUTL2	IOL = -100 μA, SYNCH_OUT pin	–	AGND2 + 0.03	AGND2 + 0.06	V
	VOUTH2	IOH = 100 μA, SYNCH_OUT pin	AV_{DD1} - 0.06	AV_{DD1} - 0.03	–	V
Gain bandwidth	GBW1	CLK_SYNCH = H, SYNCH_OUT pin CL = 30 pF, GC4 = 11H (40 dB)	–	1.38	–	MHz
	GBW2	CLK_SYNCH = L, SYNCH_OUT or GAINAMP_OUT pin CL = 30 pF, GC4 = 11H (40 dB)	–	0.86	–	MHz
Input conversion offset voltage	VOFF	GC4 = 00H (6 dB), T_A = 25°C, GAINAMP_IN = 2.5 V	-30	–	30	mV
Input conversion offset voltage temperature coefficient	VOTC1	CLK_SYNCH = H, SYNCH_OUT pin	–	±6	–	μV/°C
	VOTC2	CLK_SYNCH = L, GAINAMP_OUT pin	–	±18	–	μV/°C
Slew rate	SR	CL = 30 pF	–	0.9	–	V/μs
Equivalent input noise	En_Gain	f = 1 kHz, GC4 = 11H (40 dB) GAINAMP_OUT pin	–	700	–	nV/√ Hz
Power supply rejection ratio	PSRR1	CLK_SYNCH = H, SYNCH_OUT pin, f = 1 kHz, GC4 = 00H (6 dB)	–	60	–	dB
	PSRR2	CLK_SYNCH = L, SYNCH_OUT or GAINAMP_OUT pin, f = 1 kHz, GC4 = 00H (6 dB)	–	45	–	dB
Gain setting error	GAIN_Accu1	T_A = 25°C	-0.6	–	0.6	dB
	GAIN_Accu2	T_A = –40 to 85°C	-1.0	–	1.0	dB
CLK_SYNCH low-level input voltage	V_{ILCLK_SYNCH}				0.3 × AV_{DD1}	V
CLK_SYNCH high-level input voltage	V_{IHCLK_SYNCH}		0.7 × AV_{DD1}			V