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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Active
Core Processor	ARM® Cortex®-M0+
Core Size	32-Bit Single-Core
Speed	48MHz
Connectivity	I ² C, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, LVD, POR, PWM, WDT
Number of I/O	28
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 3.6V
Data Converters	A/D 9x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount, Wettable Flank
Package / Case	32-VFQFN Exposed Pad
Supplier Device Package	32-HVQFN (5x5)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mkl14z32vfm4

Ordering Information

Part Number	Memory		Maximum number of I/O's
	Flash (KB)	SRAM (KB)	
MKL14Z32VFM4	32	4	28
MKL14Z64VFM4	64	8	28
MKL14Z32VFT4	32	4	40
MKL14Z64VFT4	64	8	40
MKL14Z32VLH4	32	4	54
MKL14Z64VLH4	64	8	54
MKL14Z32VLK4	32	4	70
MKL14Z64VLK4	64	8	70

Related Resources

Type	Description	Resource
Selector Guide	The Freescale Solution Advisor is a web-based tool that features interactive application wizards and a dynamic product selector.	Solution Advisor
Product Brief	The Product Brief contains concise overview/summary information to enable quick evaluation of a device for design suitability.	KL1 Family Product Brief ¹
Reference Manual	The Reference Manual contains a comprehensive description of the structure and function (operation) of a device.	KL14P80M48SF0RM ¹
Data Sheet	The Data Sheet includes electrical characteristics and signal connections.	KL14P80M48SF0 ¹
Chip Errata	The chip mask set Errata provides additional or corrective information for a particular device mask set.	KINETIS_L_xN97F ²
Package drawing	Package dimensions are provided in package drawings.	QFN 32-pin: 98ASA00473D ¹ QFN 48-pin: 98ASA00466D ¹ LQFP 64-pin: 98ASS23234W ¹ LQFP 80-pin: 98ASS23174W ¹

1. To find the associated resource, go to <http://www.freescale.com> and perform a search using this term.
2. To find the associated resource, go to <http://www.freescale.com> and perform a search using this term with the "x" replaced by the revision of the device you are using.

Figure 1 shows the functional modules in the chip.

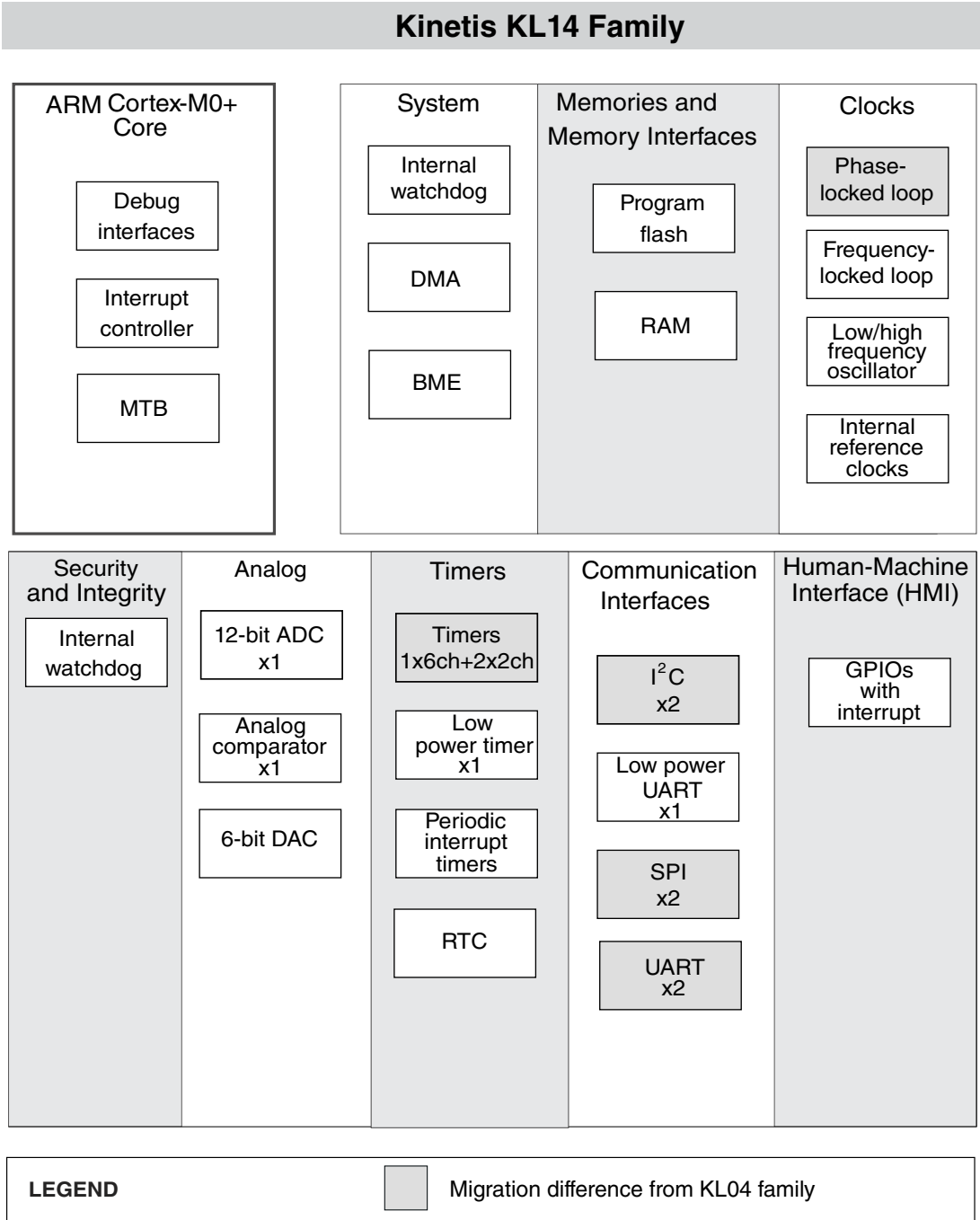


Figure 1. Functional block diagram

1.4 Voltage and current operating ratings

Table 4. Voltage and current operating ratings

Symbol	Description	Min.	Max.	Unit
V_{DD}	Digital supply voltage	-0.3	3.8	V
I_{DD}	Digital supply current	—	120	mA
V_{IO}	IO pin input voltage	-0.3	$V_{DD} + 0.3$	V
I_D	Instantaneous maximum current single pin limit (applies to all port pins)	-25	25	mA
V_{DDA}	Analog supply voltage	$V_{DD} - 0.3$	$V_{DD} + 0.3$	V

2 General

2.1 AC electrical characteristics

Unless otherwise specified, propagation delays are measured from the 50% to the 50% point, and rise and fall times are measured at the 20% and 80% points, as shown in the following figure.

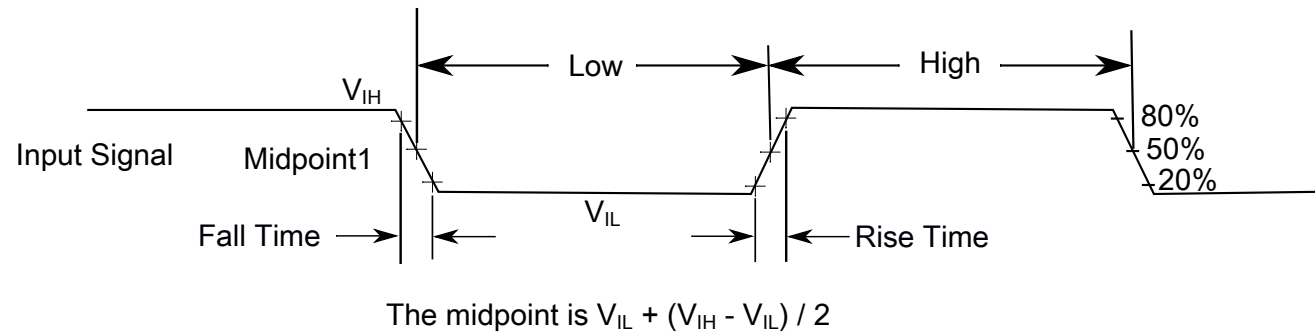


Figure 2. Input signal measurement reference

All digital I/O switching characteristics, unless otherwise specified, assume the output pins have the following characteristics.

- $C_L=30$ pF loads
- Slew rate disabled
- Normal drive strength

2.2 Nonswitching electrical specifications

Table 7. Voltage and current operating behaviors (continued)

Symbol	Description	Min.	Max.	Unit	Notes
V_{OL}	Output low voltage — High drive pad				1
	<ul style="list-style-type: none"> $2.7\text{ V} \leq V_{DD} \leq 3.6\text{ V}$, $I_{OL} = 18\text{ mA}$ $1.71\text{ V} \leq V_{DD} \leq 2.7\text{ V}$, $I_{OL} = 6\text{ mA}$ 	—	0.5	V	
I_{OLT}	Output low current total for all ports	—	100	mA	—
I_{IN}	Input leakage current (per pin) for full temperature range	—	1	μA	3
I_{IN}	Input leakage current (per pin) at 25 °C	—	0.025	μA	3
I_{IN}	Input leakage current (total all pins) for full temperature range	—	65	μA	3
I_{OZ}	Hi-Z (off-state) leakage current (per pin)	—	1	μA	—
R_{PU}	Internal pullup resistors	20	50	k Ω	4
R_{PD}	Internal pulldown resistors	20	50	k Ω	5

1. PTB0, PTB1, PTD6, and PTD7 I/O have both high drive and normal drive capability selected by the associated PTx_PCRn[DSE] control bit. All other GPIOs are normal drive only.
2. The reset pin only contains an active pull down device when configured as the RESET signal or as a GPIO. When configured as a GPIO output, it acts as a pseudo open drain output.
3. Measured at $V_{DD} = 3.6\text{ V}$
4. Measured at V_{DD} supply voltage = V_{DD} min and $V_{input} = V_{SS}$
5. Measured at V_{DD} supply voltage = V_{DD} min and $V_{input} = V_{DD}$

2.2.4 Power mode transition operating behaviors

All specifications except t_{POR} and $VLLSx \rightarrow \text{RUN}$ recovery times in the following table assume this clock configuration:

- CPU and system clocks = 48 MHz
- Bus and flash clock = 24 MHz
- FEI clock mode

POR and $VLLSx \rightarrow \text{RUN}$ recovery use FEI clock mode at the default CPU and system frequency of 21 MHz, and a bus and flash clock frequency of 10.5 MHz.

Table 8. Power mode transition operating behaviors

Symbol	Description	Min.	Typ.	Max.	Unit	
t_{POR}	After a POR event, amount of time from the point V_{DD} reaches 1.8 V to execution of the first instruction across the operating temperature range of the chip.	—	—	300	μs	1
	<ul style="list-style-type: none"> $VLLS0 \rightarrow \text{RUN}$ 	—	95	115	μs	

Table continues on the next page...

Table 9. Power consumption operating behaviors (continued)

Symbol	Description	Temp.	Typ.	Max	Unit	Note
I_{DD_WAIT}	Wait mode current - core disabled / 48 MHz system / 24 MHz bus / flash disabled (flash doze enabled), all peripheral clocks disabled, at 3.0 V	—	3.1	3.8	mA	3
I_{DD_WAIT}	Wait mode current - core disabled / 24 MHz system / 24 MHz bus / flash disabled (flash doze enabled), all peripheral clocks disabled • at 3.0 V	—	2.4	3.2	mA	3
I_{DD_PSTOP2}	Stop mode current with partial stop 2 clocking option - core and system disabled / 10.5 MHz bus, at 3.0 V	—	1.6	2	mA	3
$I_{DD_VLPRCO_CM}$	Very-low-power run mode current in compute operation - 4 MHz core / 0.8 MHz flash / bus clock disabled, LPTMR running with 4 MHz internal reference clock, CoreMark benchmark code executing from flash, at 3.0 V	—	777	—	μA	5
I_{DD_VLPRCO}	Very low power run mode current in compute operation - 4 MHz core / 0.8 MHz flash / bus clock disabled, code executing from flash, at 3.0 V	—	171	420	μA	6
I_{DD_VLPR}	Very low power run mode current - 4 MHz core / 0.8 MHz bus and flash, all peripheral clocks disabled, code executing from flash, at 3.0 V	—	204	449	μA	6
I_{DD_VLPR}	Very low power run mode current - 4 MHz core / 0.8 MHz bus and flash, all peripheral clocks enabled, code executing from flash, at 3.0 V	—	262	509	μA	4, 6
I_{DD_VLPW}	Very low power wait mode current - core disabled / 4 MHz system / 0.8 MHz bus / flash disabled (flash doze enabled), all peripheral clocks disabled, at 3.0 V	—	123	366	μA	6
I_{DD_STOP}	Stop mode current at 3.0 V	at 25 °C	319	343	μA	—
		at 50 °C	333	365	μA	
		at 70 °C	353	400	μA	
		at 85 °C	380	450	μA	
		at 105 °C	444	572	μA	
I_{DD_VLPS}	Very-low-power stop mode current at 3.0 V	at 25 °C	3.75	8.46	μA	—
		at 50 °C	6.66	13.41	μA	
		at 70 °C	12.9	25.71	μA	
		at 85 °C	22.7	44.06	μA	
		at 105 °C	48.4	90.1	μA	
I_{DD_LLS}	Low leakage stop mode current at 3.0 V	at 25 °C	1.68	2.09	μA	—
		at 50 °C	3.05	4.04	μA	

Table continues on the next page...

Table 9. Power consumption operating behaviors (continued)

Symbol	Description	Temp.	Typ.	Max	Unit	Note
		at 70 °C	5.71	7.75	μA	
		at 85 °C	10	13.54	μA	
		at 105 °C	22.4	30.41	μA	
I _{DD_VLLS3}	Very low-leakage stop mode 3 current at 3.0 V	at 25 °C	1.22	1.6	μA	—
		at 50 °C	2.25	2.31	μA	
		at 70 °C	4.21	5.44	μA	
		at 85 °C	7.37	9.44	μA	
		at 105 °C	16.6	21.76	μA	
I _{DD_VLLS1}	Very low-leakage stop mode 1 current at 3.0 V	at 25 °C	0.58	0.94	μA	—
		at 50 °C	1.26	1.31	μA	
		at 70 °C	2.53	3.33	μA	
		at 85 °C	4.74	6.1	μA	
		at 105 °C	11.4	15.27	μA	
I _{DD_VLLS0}	Very low-leakage stop mode 0 current (SMC_STOPCTRL[PORPO] = 0) at 3.0 V	at 25 °C	0.31	0.65	μA	—
		at 50 °C	0.99	1.43	μA	
		at 70 °C	2.25	3.01	μA	
		at 85 °C	4.46	5.83	μA	
		at 105 °C	11.13	14.99	μA	
I _{DD_VLLS0}	Very low-leakage stop mode 0 current (SMC_STOPCTRL[PORPO] = 1) at 3.0 V	at 25 °C	0.12	0.47	μA	7
		at 50 °C	0.8	1.24	μA	
		at 70 °C	2.06	2.81	μA	
		at 85 °C	4.27	5.62	μA	
		at 105 °C	10.93	14.78	μA	

1. The analog supply current is the sum of the active or disabled current for each of the analog modules on the device. See each module's specification for its supply current.
2. MCG configured for PEE mode. CoreMark benchmark compiled using Keil 4.54 with optimization level 3, optimized for time.
3. MCG configured for FEI mode.
4. Incremental current consumption from peripheral activity is not included.
5. MCG configured for BLPI mode. CoreMark benchmark compiled using IAR 6.40 with optimization level high, optimized for balanced.
6. MCG configured for BLPI mode.
7. No brownout.

Table 10. Low power mode peripheral adders — typical value

Symbol	Description	Temperature (°C)						Unit
		-40	25	50	70	85	105	
I _{IREFSTEN4MHz}	4 MHz internal reference clock (IRC) adder. Measured by entering STOP or VLPS mode with 4 MHz IRC enabled.	56	56	56	56	56	56	μA

Table continues on the next page...

Table 10. Low power mode peripheral adders — typical value

Symbol	Description	Temperature (°C)						Unit
		-40	25	50	70	85	105	
	the device in STOP or VLPS mode. ADC is configured for low power mode using the internal clock and continuous conversions.							

2.2.5.1 Diagram: Typical IDD_RUN operating behavior

The following data was measured under these conditions:

- MCG in FBE for run mode, and BLPE for VLPR mode
- No GPIOs toggled
- Code execution from flash with cache enabled
- For the ALLOFF curve, all peripheral clocks are disabled except FTFA

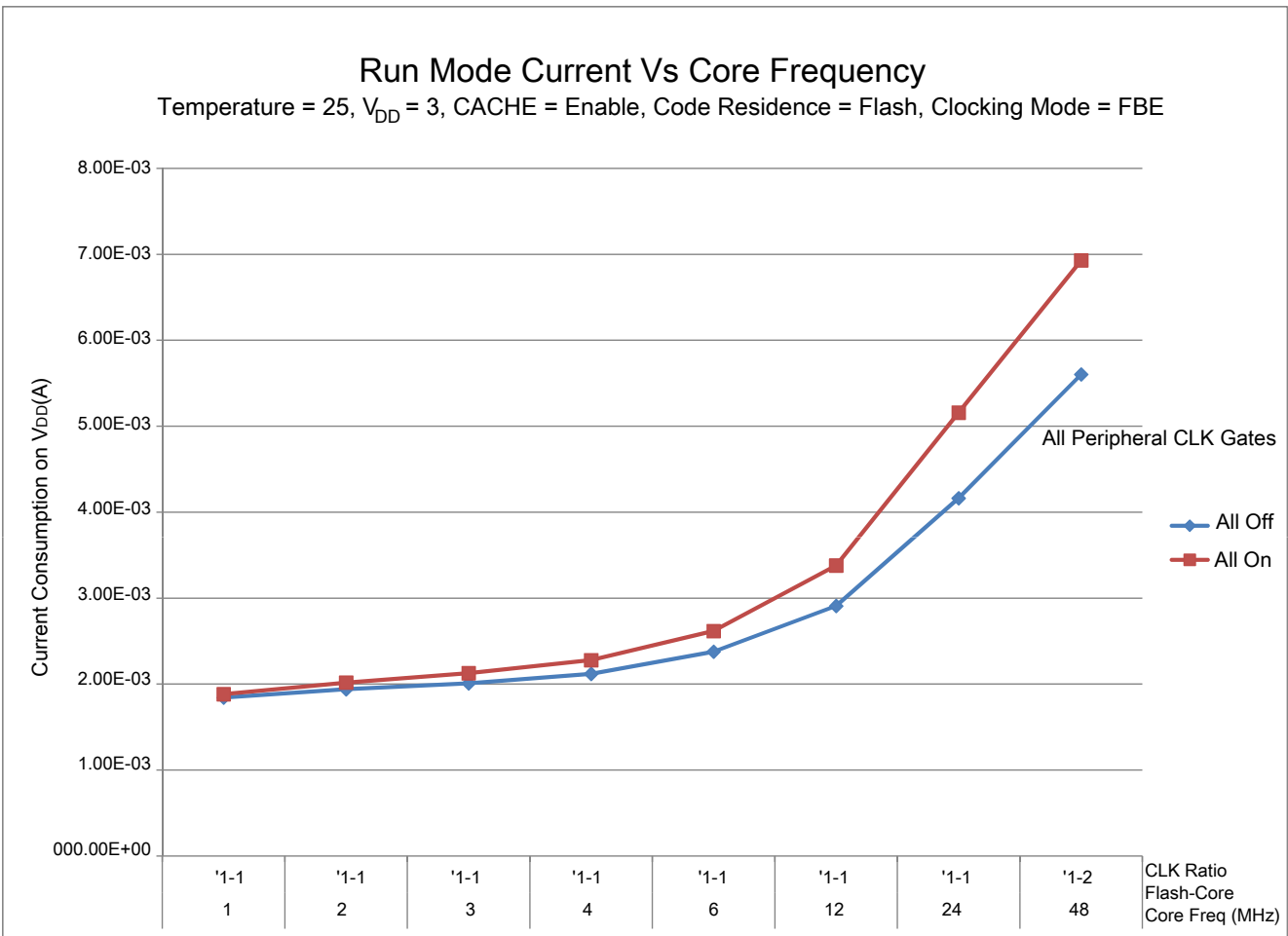


Figure 3. Run mode supply current vs. core frequency

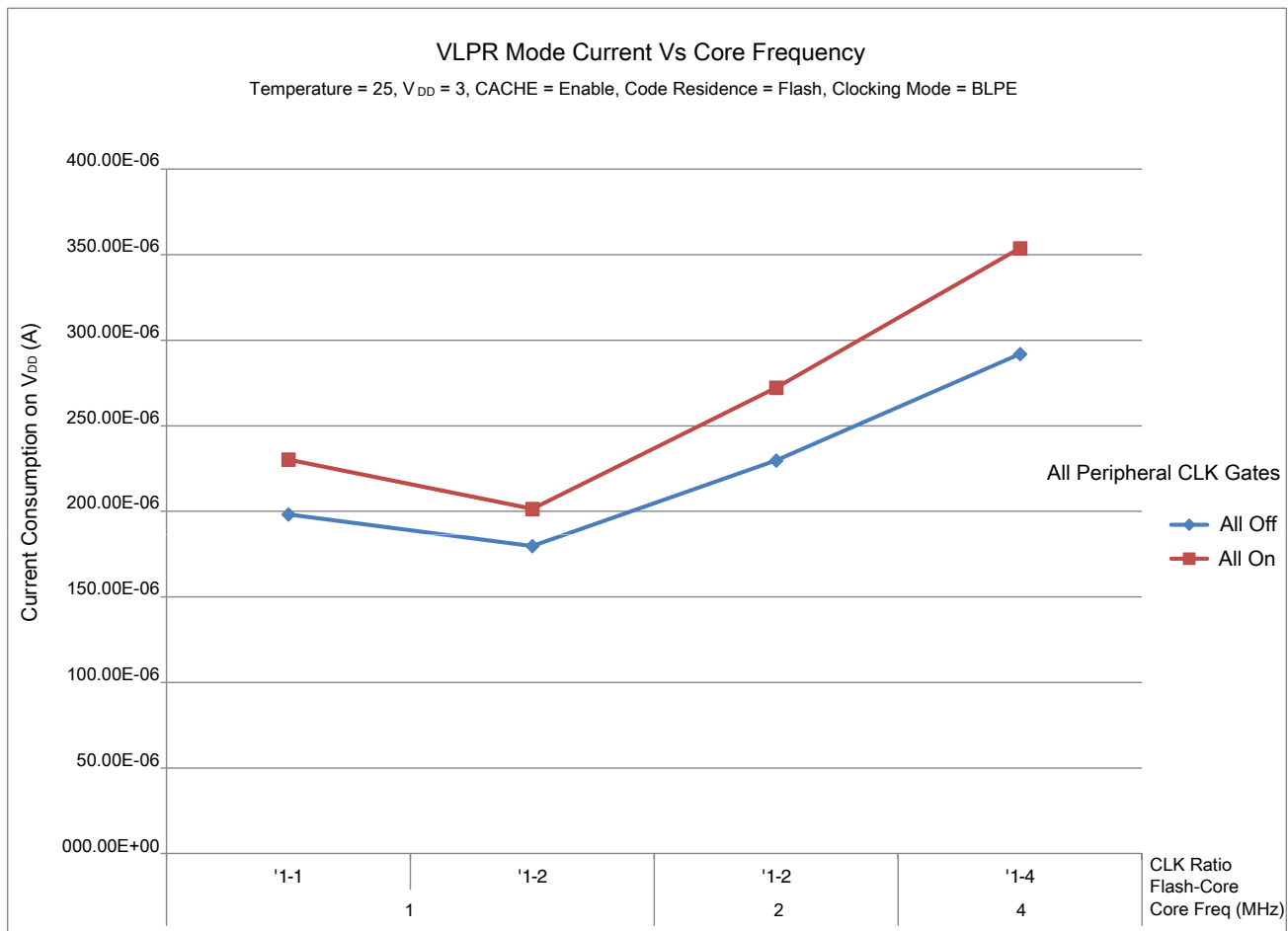


Figure 4. VLPR mode current vs. core frequency

2.2.6 EMC radiated emissions operating behaviors

Table 11. EMC radiated emissions operating behaviors for 64-pin LQFP package

Symbol	Description	Frequency band (MHz)	Typ.	Unit	Notes
V _{RE1}	Radiated emissions voltage, band 1	0.15–50	13	dBμV	1, 2
V _{RE2}	Radiated emissions voltage, band 2	50–150	15	dBμV	
V _{RE3}	Radiated emissions voltage, band 3	150–500	12	dBμV	
V _{RE4}	Radiated emissions voltage, band 4	500–1000	7	dBμV	
V _{RE_IEC}	IEC level	0.15–1000	M	—	2, 3

1. Determined according to IEC Standard 61967-1, *Integrated Circuits - Measurement of Electromagnetic Emissions, 150 kHz to 1 GHz Part 1: General Conditions and Definitions* and IEC Standard 61967-2, *Integrated Circuits - Measurement of Electromagnetic Emissions, 150 kHz to 1 GHz Part 2: Measurement of Radiated Emissions—TEM Cell and Wideband TEM Cell Method*. Measurements were made while the microcontroller was running basic

Table 13. Device clock specifications (continued)

Symbol	Description	Min.	Max.	Unit
f _{LPTMR_ERCLK}	LPTMR external reference clock	—	16	MHz
f _{osc_hi_2}	Oscillator crystal or resonator frequency — high frequency mode (high range) (MCG_C2[RANGE]=1x)	—	16	MHz
f _{TPM}	TPM asynchronous clock	—	8	MHz
f _{UART0}	UART0 asynchronous clock	—	8	MHz

1. The frequency limitations in VLPR and VLPS modes here override any frequency specification listed in the timing specification for any other module. These same frequency limits apply to VLPS, whether VLPS was entered from RUN or from VLPR.
2. The LPTMR can be clocked at this speed in VLPR or VLPS only when the source is an external pin.

2.3.2 General switching specifications

These general-purpose specifications apply to all signals configured for GPIO and UART signals.

Table 14. General switching specifications

Description	Min.	Max.	Unit	Notes
GPIO pin interrupt pulse width (digital glitch filter disabled) — Synchronous path	1.5	—	Bus clock cycles	1
External RESET and NMI pin interrupt pulse width — Asynchronous path	100	—	ns	2
GPIO pin interrupt pulse width — Asynchronous path	16	—	ns	2
Port rise and fall time	—	36	ns	3

1. The greater synchronous and asynchronous timing must be met.
2. This is the shortest pulse that is guaranteed to be recognized.
3. 75 pF load

2.4 Thermal specifications

2.4.1 Thermal operating requirements

Table 15. Thermal operating requirements

Symbol	Description	Min.	Max.	Unit
T _J	Die junction temperature	−40	125	°C
T _A	Ambient temperature	−40	105	°C

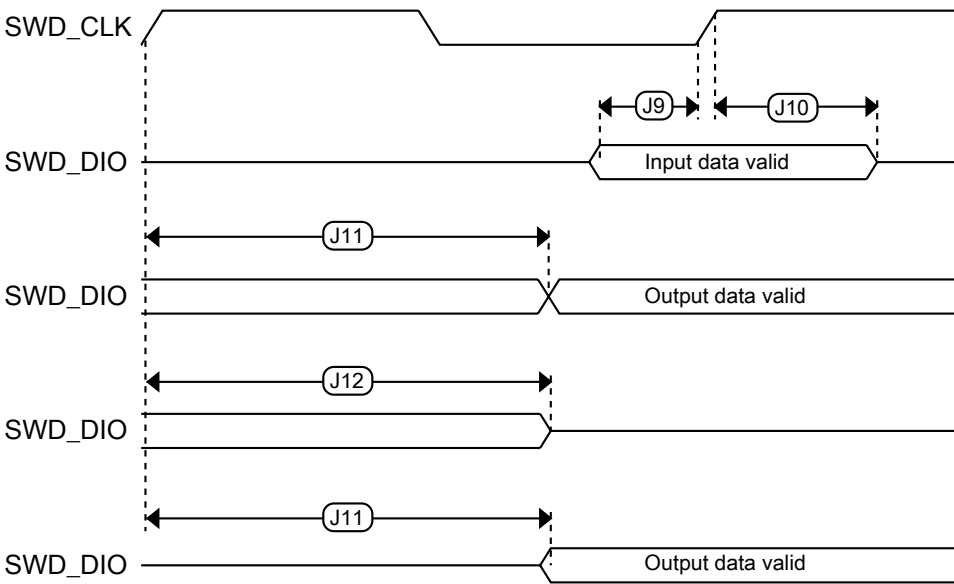


Figure 6. Serial wire data timing

3.2 System modules

There are no specifications necessary for the device's system modules.

3.3 Clock modules

3.3.1 MCG specifications

Table 18. MCG specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
f_{ints_ft}	Internal reference frequency (slow clock) — factory trimmed at nominal V_{DD} and 25 °C	—	32.768	—	kHz	
f_{ints_t}	Internal reference frequency (slow clock) — user trimmed	31.25	—	39.0625	kHz	
$\Delta f_{dco_res_t}$	Resolution of trimmed average DCO output frequency at fixed voltage and temperature — using C3[SCTTRIM] and C4[SCFTRIM]	—	± 0.3	± 0.6	% f_{dco}	1

Table continues on the next page...

Table 19. Oscillator DC electrical specifications (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
	<ul style="list-style-type: none"> 24 MHz 32 MHz 	—	1.5	—	mA	
I_{DDOSC}	Supply current — high gain mode (HGO=1) <ul style="list-style-type: none"> 32 kHz 4 MHz 8 MHz (RANGE=01) 16 MHz 24 MHz 32 MHz 	—	25	—	μ A	1
		—	400	—	μ A	
		—	500	—	μ A	
		—	2.5	—	mA	
		—	3	—	mA	
		—	4	—	mA	
C_x	EXTAL load capacitance	—	—	—		2, 3
C_y	XTAL load capacitance	—	—	—		2, 3
R_F	Feedback resistor — low-frequency, low-power mode (HGO=0)	—	—	—	M Ω	2, 4
	Feedback resistor — low-frequency, high-gain mode (HGO=1)	—	10	—	M Ω	
	Feedback resistor — high-frequency, low-power mode (HGO=0)	—	—	—	M Ω	
	Feedback resistor — high-frequency, high-gain mode (HGO=1)	—	1	—	M Ω	
R_S	Series resistor — low-frequency, low-power mode (HGO=0)	—	—	—	k Ω	
	Series resistor — low-frequency, high-gain mode (HGO=1)	—	200	—	k Ω	
	Series resistor — high-frequency, low-power mode (HGO=0)	—	—	—	k Ω	
	Series resistor — high-frequency, high-gain mode (HGO=1)	—	0	—	k Ω	
V_{pp} ⁵	Peak-to-peak amplitude of oscillation (oscillator mode) — low-frequency, low-power mode (HGO=0)	—	0.6	—	V	
	Peak-to-peak amplitude of oscillation (oscillator mode) — low-frequency, high-gain mode (HGO=1)	—	V_{DD}	—	V	
	Peak-to-peak amplitude of oscillation (oscillator mode) — high-frequency, low-power mode (HGO=0)	—	0.6	—	V	
	Peak-to-peak amplitude of oscillation (oscillator mode) — high-frequency, high-gain mode (HGO=1)	—	V_{DD}	—	V	

1. V_{DD} =3.3 V, Temperature =25 °C

2. See crystal or resonator manufacturer's recommendation

3.4.1.1 Flash timing specifications — program and erase

The following specifications represent the amount of time the internal charge pumps are active and do not include command overhead.

Table 21. NVM program/erase timing specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
$t_{hvp\text{gm}4}$	Longword Program high-voltage time	—	7.5	18	μs	—
$t_{h\text{versscr}}$	Sector Erase high-voltage time	—	13	113	ms	1
$t_{h\text{versall}}$	Erase All high-voltage time	—	52	452	ms	1

1. Maximum time based on expectations at cycling end-of-life.

3.4.1.2 Flash timing specifications — commands

Table 22. Flash command timing specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
$t_{rd1\text{sec}1k}$	Read 1s Section execution time (flash sector)	—	—	60	μs	1
t_{pgmchk}	Program Check execution time	—	—	45	μs	1
$t_{rd\text{rsrc}}$	Read Resource execution time	—	—	30	μs	1
t_{pgm4}	Program Longword execution time	—	65	145	μs	—
$t_{er\text{sscr}}$	Erase Flash Sector execution time	—	14	114	ms	2
$t_{rd1\text{all}}$	Read 1s All Blocks execution time	—	—	1.8	ms	—
$t_{rd\text{once}}$	Read Once execution time	—	—	25	μs	1
$t_{pgm\text{once}}$	Program Once execution time	—	65	—	μs	—
$t_{er\text{all}}$	Erase All Blocks execution time	—	88	650	ms	2
$t_{vfy\text{key}}$	Verify Backdoor Access Key execution time	—	—	30	μs	1

1. Assumes 25 MHz flash clock frequency.
2. Maximum times for erase parameters based on expectations at cycling end-of-life.

3.4.1.3 Flash high voltage current behaviors

Table 23. Flash high voltage current behaviors

Symbol	Description	Min.	Typ.	Max.	Unit
I_{DD_PGM}	Average current adder during high voltage flash programming operation	—	2.5	6.0	mA
I_{DD_ERS}	Average current adder during high voltage flash erase operation	—	1.5	4.0	mA

3.6.1.2 12-bit ADC electrical characteristics

Table 26. 12-bit ADC characteristics ($V_{REFH} = V_{DDA}$, $V_{REFL} = V_{SSA}$)

Symbol	Description	Conditions ¹	Min.	Typ. ²	Max.	Unit	Notes
I_{DDA_ADC}	Supply current		0.215	—	1.7	mA	3
f_{ADACK}	ADC asynchronous clock source	<ul style="list-style-type: none"> ADLPC = 1, ADHSC = 0 ADLPC = 1, ADHSC = 1 ADLPC = 0, ADHSC = 0 ADLPC = 0, ADHSC = 1 	1.2 2.4 3.0 4.4	2.4 4.0 5.2 6.2	3.9 6.1 7.3 9.5	MHz MHz MHz MHz	$t_{ADACK} = 1/f_{ADACK}$
	Sample Time	See Reference Manual chapter for sample times					
TUE	Total unadjusted error	<ul style="list-style-type: none"> 12-bit modes <12-bit modes 	— —	± 4 ± 1.4	± 6.8 ± 2.1	LSB ⁴	5
DNL	Differential non-linearity	<ul style="list-style-type: none"> 12-bit modes <12-bit modes 	— —	± 0.7 ± 0.2	–1.1 to +1.9 –0.3 to 0.5	LSB ⁴	5
INL	Integral non-linearity	<ul style="list-style-type: none"> 12-bit modes <12-bit modes 	— —	± 1.0 ± 0.5	–2.7 to +1.9 –0.7 to +0.5	LSB ⁴	5
E_{FS}	Full-scale error	<ul style="list-style-type: none"> 12-bit modes <12-bit modes 	— —	–4 –1.4	–5.4 –1.8	LSB ⁴	$V_{ADIN} = V_{DDA}$ ⁵
E_Q	Quantization error	<ul style="list-style-type: none"> 12-bit modes 	—	—	± 0.5	LSB ⁴	
E_{IL}	Input leakage error		$I_{in} \times R_{AS}$			mV	I_{in} = leakage current (refer to the MCU's voltage and current operating ratings)
	Temp sensor slope	Across the full temperature range of the device	1.55	1.62	1.69	mV/°C	6
V_{TEMP25}	Temp sensor voltage	25 °C	706	716	726	mV	6

1. All accuracy numbers assume the ADC is calibrated with $V_{REFH} = V_{DDA}$

2. Typical values assume $V_{DDA} = 3.0$ V, Temp = 25 °C, $f_{ADCK} = 2.0$ MHz unless otherwise stated. Typical values are for reference only and are not tested in production.

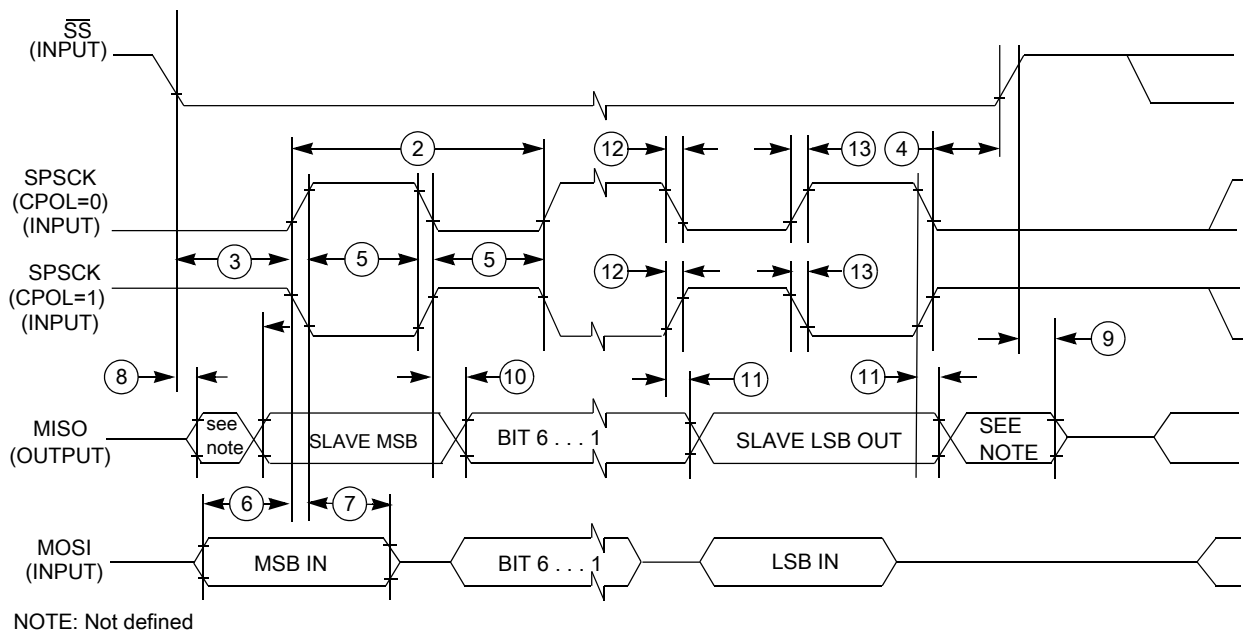


Figure 13. SPI slave mode timing (CPHA = 0)

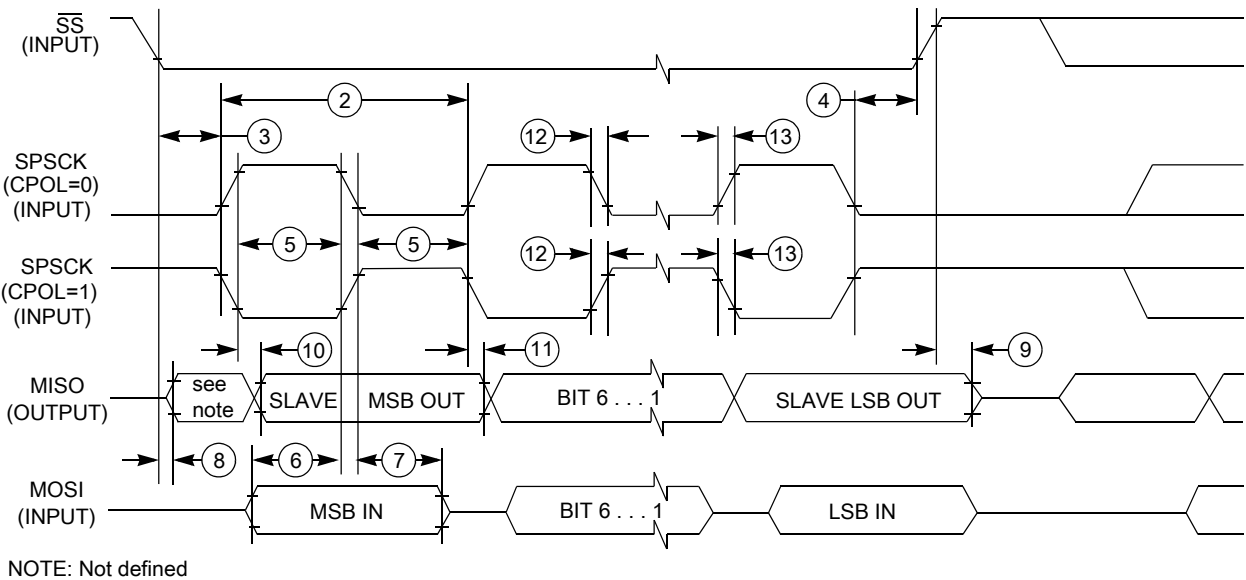


Figure 14. SPI slave mode timing (CPHA = 1)

Pinout

80 LQFP	64 LQFP	48 QFN	32 QFN	Pin Name	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7
6	—	—	—	PTE5	DISABLED		PTE5						
7	3	1	—	VDD	VDD	VDD							
8	4	2	—	VSS	VSS	VSS							
9	5	3	3	PTE16	ADC0_SE1	ADC0_SE1	PTE16	SPI0_PCS0	UART2_TX	TPM_CLKIN0			
10	6	4	4	PTE17	ADC0_SE5a	ADC0_SE5a	PTE17	SPI0_SCK	UART2_RX	TPM_CLKIN1		LPTMR0_ALT3	
11	7	5	5	PTE18	ADC0_SE2	ADC0_SE2	PTE18	SPI0_MOSI		I2C0_SDA	SPI0_MISO		
12	8	6	6	PTE19	ADC0_SE6a	ADC0_SE6a	PTE19	SPI0_MISO		I2C0_SCL	SPI0_MOSI		
13	9	7	—	PTE20	ADC0_SE0	ADC0_SE0	PTE20		TPM1_CH0	UART0_TX			
14	10	8	—	PTE21	ADC0_SE4a	ADC0_SE4a	PTE21		TPM1_CH1	UART0_RX			
15	11	—	—	PTE22	ADC0_SE3	ADC0_SE3	PTE22		TPM2_CH0	UART2_TX			
16	12	—	—	PTE23	ADC0_SE7a	ADC0_SE7a	PTE23		TPM2_CH1	UART2_RX			
17	13	9	7	VDDA	VDDA	VDDA							
18	14	10	—	VREFH	VREFH	VREFH							
19	15	11	—	VREFL	VREFL	VREFL							
20	16	12	8	VSSA	VSSA	VSSA							
21	17	13	—	PTE29	CMP0_IN5/ ADC0_SE4b	CMP0_IN5/ ADC0_SE4b	PTE29		TPM0_CH2	TPM_CLKIN0			
22	18	14	9	PTE30	ADC0_SE23/ CMP0_IN4	ADC0_SE23/ CMP0_IN4	PTE30		TPM0_CH3	TPM_CLKIN1			
23	19	—	—	PTE31	DISABLED		PTE31		TPM0_CH4				
24	20	15	—	PTE24	DISABLED		PTE24		TPM0_CH0		I2C0_SCL		
25	21	16	—	PTE25	DISABLED		PTE25		TPM0_CH1		I2C0_SDA		
26	22	17	10	PTA0	SWD_CLK		PTA0		TPM0_CH5				SWD_CLK
27	23	18	11	PTA1	DISABLED		PTA1	UART0_RX	TPM2_CH0				
28	24	19	12	PTA2	DISABLED		PTA2	UART0_TX	TPM2_CH1				
29	25	20	13	PTA3	SWD_DIO		PTA3	I2C1_SCL	TPM0_CH0				SWD_DIO
30	26	21	14	PTA4	NMI_b		PTA4	I2C1_SDA	TPM0_CH1				NMI_b
31	27	—	—	PTA5	DISABLED		PTA5		TPM0_CH2				
32	28	—	—	PTA12	DISABLED		PTA12		TPM1_CH0				
33	29	—	—	PTA13	DISABLED		PTA13		TPM1_CH1				
34	—	—	—	PTA14	DISABLED		PTA14	SPI0_PCS0	UART0_TX				
35	—	—	—	PTA15	DISABLED		PTA15	SPI0_SCK	UART0_RX				
36	—	—	—	PTA16	DISABLED		PTA16	SPI0_MOSI			SPI0_MISO		
37	—	—	—	PTA17	DISABLED		PTA17	SPI0_MISO			SPI0_MOSI		
38	30	22	15	VDD	VDD	VDD							
39	31	23	16	VSS	VSS	VSS							
40	32	24	17	PTA18	EXTAL0	EXTAL0	PTA18		UART1_RX	TPM_CLKIN0			

80 LQFP	64 LQFP	48 QFN	32 QFN	Pin Name	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7
41	33	25	18	PTA19	XTAL0	XTAL0	PTA19		UART1_TX	TPM_CLKIN1		LPTMR0_ALT1	
42	34	26	19	RESET_b	RESET_b		PTA20						
43	35	27	20	PTB0/ LLWU_P5	ADC0_SE8	ADC0_SE8	PTB0/ LLWU_P5	I2C0_SCL	TPM1_CH0				
44	36	28	21	PTB1	ADC0_SE9	ADC0_SE9	PTB1	I2C0_SDA	TPM1_CH1				
45	37	29	—	PTB2	ADC0_SE12	ADC0_SE12	PTB2	I2C0_SCL	TPM2_CH0				
46	38	30	—	PTB3	ADC0_SE13	ADC0_SE13	PTB3	I2C0_SDA	TPM2_CH1				
47	—	—	—	PTB8	DISABLED		PTB8		EXTRG_IN				
48	—	—	—	PTB9	DISABLED		PTB9						
49	—	—	—	PTB10	DISABLED		PTB10	SPI1_PCS0					
50	—	—	—	PTB11	DISABLED		PTB11	SPI1_SCK					
51	39	31	—	PTB16	DISABLED		PTB16	SPI1_MOSI	UART0_RX	TPM_CLKIN0	SPI1_MISO		
52	40	32	—	PTB17	DISABLED		PTB17	SPI1_MISO	UART0_TX	TPM_CLKIN1	SPI1_MOSI		
53	41	—	—	PTB18	DISABLED		PTB18		TPM2_CH0				
54	42	—	—	PTB19	DISABLED		PTB19		TPM2_CH1				
55	43	33	—	PTC0	ADC0_SE14	ADC0_SE14	PTC0		EXTRG_IN		CMP0_OUT		
56	44	34	22	PTC1/ LLWU_P6/ RTC_CLKIN	ADC0_SE15	ADC0_SE15	PTC1/ LLWU_P6/ RTC_CLKIN	I2C1_SCL		TPM0_CH0			
57	45	35	23	PTC2	ADC0_SE11	ADC0_SE11	PTC2	I2C1_SDA		TPM0_CH1			
58	46	36	24	PTC3/ LLWU_P7	DISABLED		PTC3/ LLWU_P7		UART1_RX	TPM0_CH2	CLKOUT		
59	47	—	—	VSS	VSS	VSS							
60	48	—	—	VDD	VDD	VDD							
61	49	37	25	PTC4/ LLWU_P8	DISABLED		PTC4/ LLWU_P8	SPI0_PCS0	UART1_TX	TPM0_CH3			
62	50	38	26	PTC5/ LLWU_P9	DISABLED		PTC5/ LLWU_P9	SPI0_SCK	LPTMR0_ALT2			CMP0_OUT	
63	51	39	27	PTC6/ LLWU_P10	CMP0_IN0	CMP0_IN0	PTC6/ LLWU_P10	SPI0_MOSI	EXTRG_IN		SPI0_MISO		
64	52	40	28	PTC7	CMP0_IN1	CMP0_IN1	PTC7	SPI0_MISO			SPI0_MOSI		
65	53	—	—	PTC8	CMP0_IN2	CMP0_IN2	PTC8	I2C0_SCL	TPM0_CH4				
66	54	—	—	PTC9	CMP0_IN3	CMP0_IN3	PTC9	I2C0_SDA	TPM0_CH5				
67	55	—	—	PTC10	DISABLED		PTC10	I2C1_SCL					
68	56	—	—	PTC11	DISABLED		PTC11	I2C1_SDA					
69	—	—	—	PTC12	DISABLED		PTC12			TPM_CLKIN0			
70	—	—	—	PTC13	DISABLED		PTC13			TPM_CLKIN1			
71	—	—	—	PTC16	DISABLED		PTC16						

80 LQFP	64 LQFP	48 QFN	32 QFN	Pin Name	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7
72	—	—	—	PTC17	DISABLED		PTC17						
73	57	41	—	PTD0	DISABLED		PTD0	SPI0_PCS0		TPM0_CH0			
74	58	42	—	PTD1	ADC0_SE5b	ADC0_SE5b	PTD1	SPI0_SCK		TPM0_CH1			
75	59	43	—	PTD2	DISABLED		PTD2	SPI0_MOSI	UART2_RX	TPM0_CH2	SPI0_MISO		
76	60	44	—	PTD3	DISABLED		PTD3	SPI0_MISO	UART2_TX	TPM0_CH3	SPI0_MOSI		
77	61	45	29	PTD4/ LLWU_P14	DISABLED		PTD4/ LLWU_P14	SPI1_PCS0	UART2_RX	TPM0_CH4			
78	62	46	30	PTD5	ADC0_SE6b	ADC0_SE6b	PTD5	SPI1_SCK	UART2_TX	TPM0_CH5			
79	63	47	31	PTD6/ LLWU_P15	ADC0_SE7b	ADC0_SE7b	PTD6/ LLWU_P15	SPI1_MOSI	UART0_RX		SPI1_MISO		
80	64	48	32	PTD7	DISABLED		PTD7	SPI1_MISO	UART0_TX		SPI1_MOSI		

5.2 KL14 pinouts

The following figures show the pinout diagrams for the devices supported by this document. Many signals may be multiplexed onto a single pin. To determine what signals can be used on which pin, see [KL14 Signal Multiplexing and Pin Assignments](#).

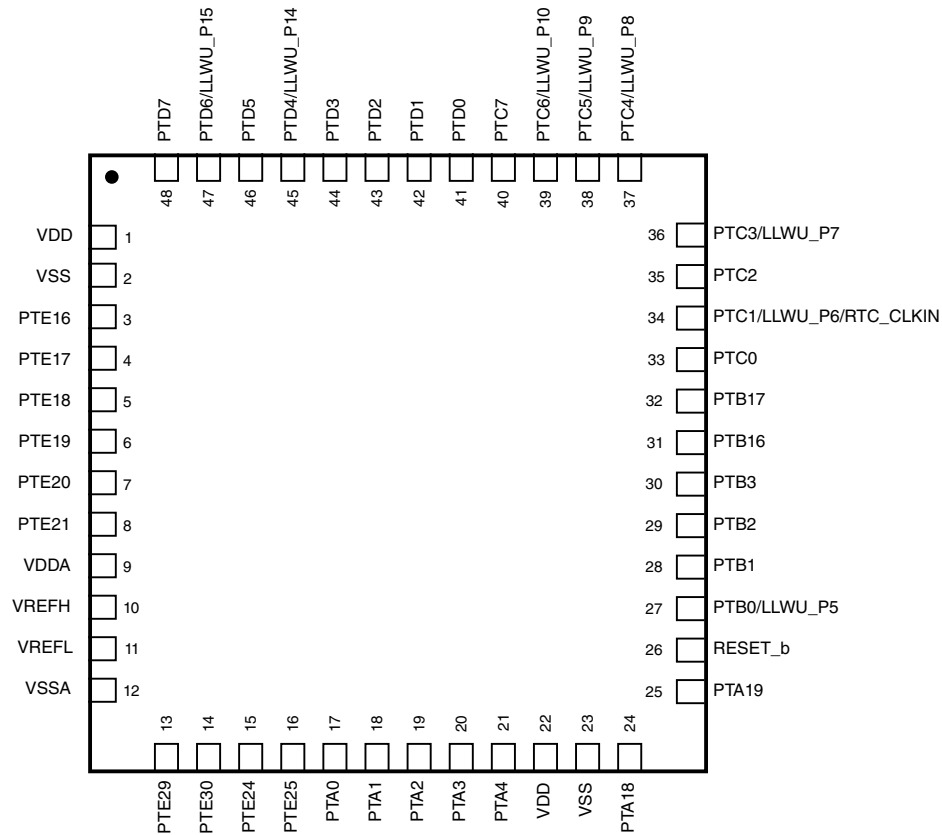
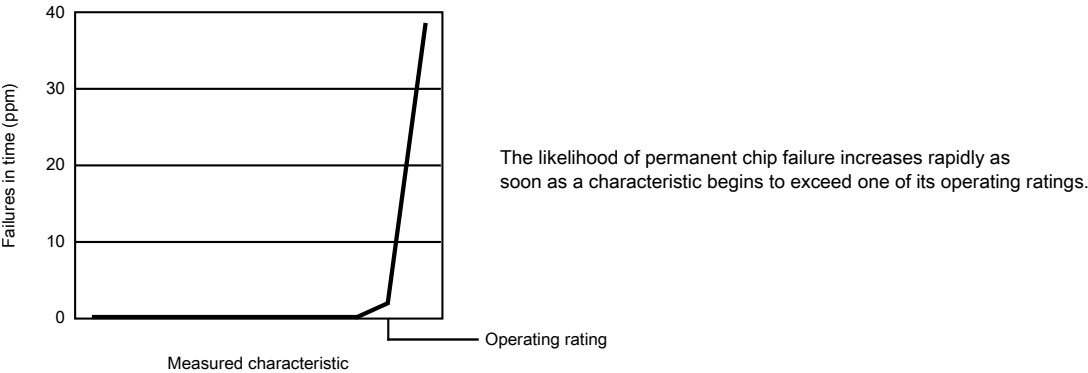
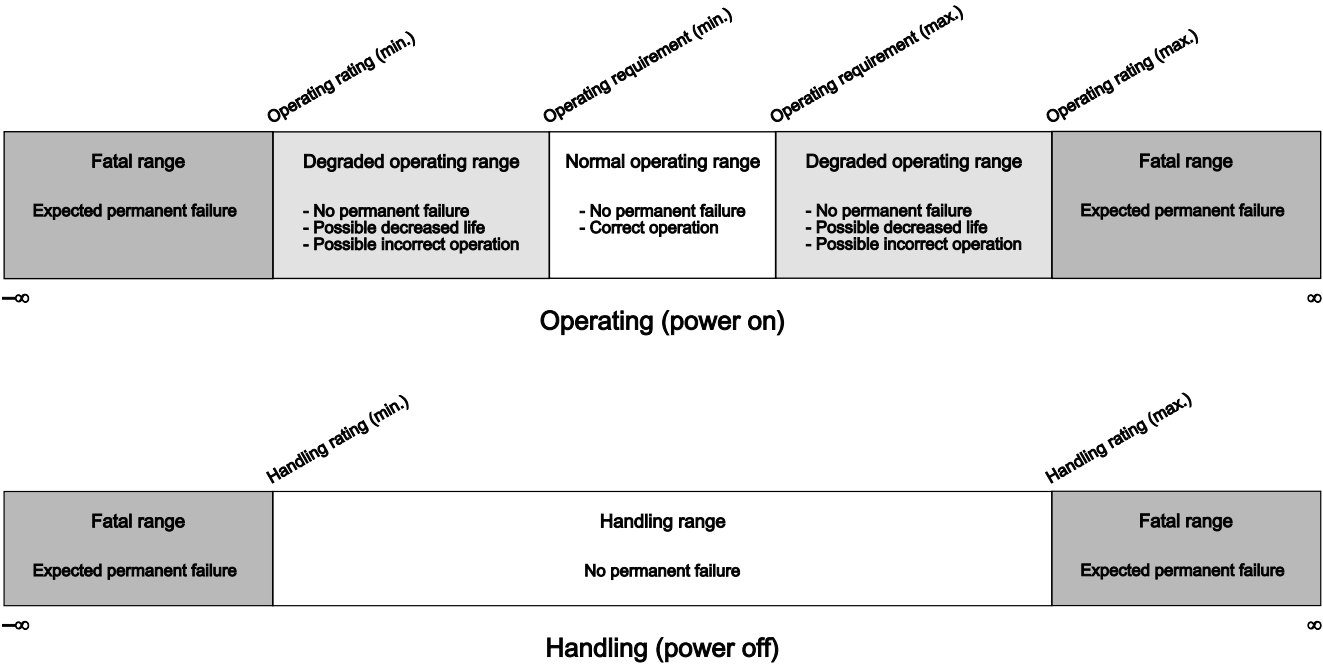


Figure 18. KL14 48-pin QFN pinout diagram

8.5 Result of exceeding a rating



8.6 Relationship between ratings and operating requirements



8.7 Guidelines for ratings and operating requirements

Follow these guidelines for ratings and operating requirements:

- Never exceed any of the chip’s ratings.
- During normal operation, don’t exceed any of the chip’s operating requirements.
- If you must exceed an operating requirement at times other than during normal operation (for example, during power sequencing), limit the duration as much as possible.

8.8 Definition: Typical value

A *typical value* is a specified value for a technical characteristic that:

- Lies within the range of values specified by the operating behavior
- Given the typical manufacturing process, is representative of that characteristic during operation when you meet the typical-value conditions or other specified conditions

Typical values are provided as design guidelines and are neither tested nor guaranteed.

8.8.1 Example 1

This is an example of an operating behavior that includes a typical value:

Symbol	Description	Min.	Typ.	Max.	Unit
I _{WP}	Digital I/O weak pullup/pulldown current	10	70	130	μA

8.8.2 Example 2

This is an example of a chart that shows typical values for various voltage and temperature conditions: