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Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

Product Status	Active
Core Processor	ARM® Cortex®-M0+
Core Size	32-Bit Single-Core
Speed	48MHz
Connectivity	I ² C, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, LVD, POR, PWM, WDT
Number of I/O	40
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 3.6V
Data Converters	A/D 15x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	48-VFQFN Exposed Pad
Supplier Device Package	48-QFN (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mkl14z32vft4

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong



Ordering Information

Part Number	Mer	nory	Maximum number of I\O's
	Flash (KB)	SRAM (KB)	
MKL14Z32VFM4	32	4	28
MKL14Z64VFM4	64	8	28
MKL14Z32VFT4	32	4	40
MKL14Z64VFT4	64	8	40
MKL14Z32VLH4	32	4	54
MKL14Z64VLH4	64	8	54
MKL14Z32VLK4	32	4	70
MKL14Z64VLK4	64	8	70

Related Resources

Туре	Description	Resource
Selector Guide	The Freescale Solution Advisor is a web-based tool that features interactive application wizards and a dynamic product selector.	Solution Advisor
Product Brief	The Product Brief contains concise overview/summary information to enable quick evaluation of a device for design suitability.	KL1 Family Product Brief ¹
Reference Manual	The Reference Manual contains a comprehensive description of the structure and function (operation) of a device.	KL14P80M48SF0RM ¹
Data Sheet	The Data Sheet includes electrical characteristics and signal connections.	KL14P80M48SF0 ¹
Chip Errata	The chip mask set Errata provides additional or corrective information for a particular device mask set.	KINETIS_L_xN97F ²
Package	Package dimensions are provided in package drawings.	QFN 32-pin: 98ASA00473D ¹
drawing		QFN 48-pin: 98ASA00466D ¹
		LQFP 64-pin: 98ASS23234W ¹
		LQFP 80-pin: 98ASS23174W ¹

1. To find the associated resource, go to http://www.freescale.com and perform a search using this term.

To find the associated resource, go to http://www.freescale.com and perform a search using this term with the "x" replaced by the revision of the device you are using.

Figure 1 shows the functional modules in the chip.



1 Ratings

1.1 Thermal handling ratings

Table 1. Thermal handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
T _{STG}	Storage temperature	-55	150	°C	1
T _{SDR}	Solder temperature, lead-free	—	260	°C	2

1. Determined according to JEDEC Standard JESD22-A103, High Temperature Storage Life.

2. Determined according to IPC/JEDEC Standard J-STD-020, Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices.

1.2 Moisture handling ratings

Table 2. Moisture handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
MSL	Moisture sensitivity level	—	3		1

1. Determined according to IPC/JEDEC Standard J-STD-020, Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices.

1.3 ESD handling ratings

Table 3. ESD handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
V _{HBM}	Electrostatic discharge voltage, human body model	-2000	+2000	V	1
V _{CDM}	Electrostatic discharge voltage, charged-device model	-500	+500	V	2
I _{LAT}	Latch-up current at ambient temperature of 105 °C	-100	+100	mA	3

1. Determined according to JEDEC Standard JESD22-A114, *Electrostatic Discharge (ESD) Sensitivity Testing Human Body Model (HBM)*.

 Determined according to JEDEC Standard JESD22-C101, Field-Induced Charged-Device Model Test Method for Electrostatic-Discharge-Withstand Thresholds of Microelectronic Components.

3. Determined according to JEDEC Standard JESD78, IC Latch-Up Test.

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Symbol	Description	Min.	Max.	Unit	Notes
V _{DD}	Supply voltage	1.71	3.6	V	
V _{DDA}	Analog supply voltage	1.71	3.6	V	—
$V_{DD} - V_{DDA}$	V _{DD} -to-V _{DDA} differential voltage	-0.1	0.1	V	—
$V_{SS} - V_{SSA}$	V _{SS} -to-V _{SSA} differential voltage	-0.1	0.1	V	—
V _{IH}	Input high voltage				—
	• $2.7 \text{ V} \le \text{V}_{\text{DD}} \le 3.6 \text{ V}$	$0.7 \times V_{DD}$	—	V	
	• $1.7 \text{ V} \le \text{V}_{\text{DD}} \le 2.7 \text{ V}$	$0.75 \times V_{DD}$	_	V	
V _{IL}	Input low voltage				_
	• $2.7 \text{ V} \le \text{V}_{\text{DD}} \le 3.6 \text{ V}$	_	$0.35 \times V_{DD}$	V	
	• $1.7 \text{ V} \le \text{V}_{\text{DD}} \le 2.7 \text{ V}$		$0.3 \times V_{DD}$	V	
V _{HYS}	Input hysteresis	$0.06 \times V_{DD}$	_	V	_
I _{ICIO}	IO pin negative DC injection current—single pin • V _{IN} < V _{SS} –0.3V	-3	_	mA	1
I _{ICcont}	Contiguous pin DC injection current —regional limit, includes sum of negative injection currents of 16 contiguous pins • Negative current injection	-25		mA	_
V _{ODPU}	Open drain pullup voltage level	V _{DD}	V _{DD}	V	2
V _{RAM}	V _{DD} voltage required to retain RAM	1.2	_	V	—

2.2.1 Voltage and current operating requirements Table 5. Voltage and current operating requirements

2. Open drain outputs must be pulled to V_{DD} .

2.2.2 LVD and POR operating requirements T

able 6.	V _{DD} supply LVD and PO	R operating requirements
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Symbol	Description	Min.	Тур.	Max.	Unit	Notes
V _{POR}	Falling V _{DD} POR detect voltage	0.8	1.1	1.5	V	—
V _{LVDH}	Falling low-voltage detect threshold — high range (LVDV = 01)	2.48	2.56	2.64	V	—
	Low-voltage warning thresholds — high range					1

^{1.} All I/O pins are internally clamped to V_{SS} through a ESD protection diode. There is no diode connection to V_{DD} . If V_{IN} greater than V_{IO_MIN} (= V_{SS}-0.3 V) is observed, then there is no need to provide current limiting resistors at the pads. If this limit cannot be observed then a current limiting resistor is required. The negative DC injection current limiting resistor is calculated as $R = (V_{IO MIN} - V_{IN})/|I_{ICIO}|$.



Symbol	Description	Min.	Max.	Unit	Notes
V _{OL}	Output low voltage — High drive pad				1
	• 2.7 V \leq V _{DD} \leq 3.6 V, I _{OL} = 18 mA	_	0.5	V	
	• $1.71 \text{ V} \le \text{V}_{\text{DD}} \le 2.7 \text{ V}, \text{ I}_{\text{OL}} = 6 \text{ mA}$	_	0.5	V	
I _{OLT}	Output low current total for all ports	_	100	mA	—
I _{IN}	Input leakage current (per pin) for full temperature range	_	1	μA	3
I _{IN}	Input leakage current (per pin) at 25 °C	_	0.025	μA	3
I _{IN}	Input leakage current (total all pins) for full temperature range	_	65	μΑ	3
I _{OZ}	Hi-Z (off-state) leakage current (per pin)	_	1	μA	—
R _{PU}	Internal pullup resistors	20	50	kΩ	4
R _{PD}	Internal pulldown resistors	20	50	kΩ	5

Table 7. Voltage and current operating behaviors (continued)

- 1. PTB0, PTB1, PTD6, and PTD7 I/O have both high drive and normal drive capability selected by the associated PTx_PCRn[DSE] control bit. All other GPIOs are normal drive only.
- 2. The reset pin only contains an active pull down device when configured as the RESET signal or as a GPIO. When configured as a GPIO output, it acts as a pseudo open drain output.
- 3. Measured at $V_{DD} = 3.6 \text{ V}$
- 4. Measured at V_{DD} supply voltage = V_{DD} min and Vinput = V_{SS}
- 5. Measured at VDD supply voltage = VDD min and Vinput = VDD

2.2.4 Power mode transition operating behaviors

All specifications except t_{POR} and VLLSx \rightarrow RUN recovery times in the following table assume this clock configuration:

- CPU and system clocks = 48 MHz
- Bus and flash clock = 24 MHz
- FEI clock mode

POR and VLLSx \rightarrow RUN recovery use FEI clock mode at the default CPU and system frequency of 21 MHz, and a bus and flash clock frequency of 10.5 MHz.

Symbol	Description	Min.	Тур.	Max.	Unit	
t _{POR}	After a POR event, amount of time from the point V_{DD} reaches 1.8 V to execution of the first instruction across the operating temperature range of the chip.	_		300	μs	1
	• VLLS0 \rightarrow RUN	_	95	115	μs	

 Table 8. Power mode transition operating behaviors

Table continues on the next page...

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Symbol	Description	Min.	Тур.	Max.	Unit	
	 VLLS1 → RUN 					
		—	93	115	μs	
	 VLLS3 → RUN 					
		—	42	53	μs	
	• LLS → RUN					
		—	4	4.6	μs	
	VLPS → RUN					
		—	4	4.4	μs	
	• STOP → RUN					
		—	4	4.4	μs	

 Table 8. Power mode transition operating behaviors (continued)

1. Normal boot (FTFA_FOPT[LPBOOT]=11).

2.2.5 Power consumption operating behaviors

The maximum values stated in the following table represent characterized results equivalent to the mean plus three times the standard deviation (mean + 3 sigma).

Symbol	Description	Temp.	Тур.	Max	Unit	Note
I _{DDA}	Analog supply current	—	—	See note	mA	1
I _{DD_RUNCO_} CM	Run mode current in compute operation - 48 MHz core / 24 MHz flash/ bus disabled, LPTMR running using 4 MHz internal reference clock, CoreMark® benchmark code executing from flash, at 3.0 V	_	6.4		mA	2
I _{DD_RUNCO}	Run mode current in compute operation - 48 MHz core / 24 MHz flash / bus clock disabled, code of while(1) loop executing from flash, at 3.0 V	_	3.9	4.8	mA	3
I _{DD_RUN}	Run mode current - 48 MHz core / 24 MHz bus and flash, all peripheral clocks disabled, code executing from flash, at 3.0 V	_	5	5.9	mA	3
I _{DD_RUN}	Run mode current - 48 MHz core / 24	at 25 °C	6.2	6.5	mA	3, 4
	MHz bus and flash, all peripheral clocks enabled, code executing from flash, at 3.0 V	at 125 °C	6.8	7.1	mA	

Table 9. Power consumption operating behaviors





Symbol	Description				Tempera	ature (°0	C)		Unit
			-40	25	50	70	85	105	
I _{IREFSTEN32KHz}	32 kHz internal reference clock Measured by entering STOP n 32 kHz IRC enabled.	(IRC) adder. node with the	52	52	52	52	52	52	μA
I _{EREFSTEN4MHz}	External 4 MHz crystal clock a Measured by entering STOP o with the crystal enabled.	dder. r VLPS mode	206	228	237	245	251	258	μA
I _{EREFSTEN32KHz}	External 32 kHz crystal clock	VLLS1	440	490	540	560	570	580	nA
	OSC0 CRIEREFSTEN and	VLLS3	440	490	540	560	570	580	
	EREFSTEN] bits. Measured	LLS	490	490	540	560	570	680	
	by entering all modes with the crystal enabled.	VLPS	510	560	560	560	610	680	
		STOP	510	560	560	560	610	680	
I _{CMP}	CMP peripheral adder measur the device in VLLS1 mode with using the 6-bit DAC and a sing input for compare. Includes 6-b consumption.	ed by placing n CMP enabled le external bit DAC power	22	22	22	22	22	22	μA
I _{RTC}	RTC peripheral adder measure the device in VLLS1 mode with kHz crystal enabled by means RTC_CR[OSCE] bit and the R for 1 minute. Includes ERCLK3 external crystal) power consum	ed by placing n external 32 of the TC ALARM set 32K (32 kHz nption.	432	357	388	475	532	810	nA
I _{UART}	UART peripheral adder measured by placing the device in STOP or VLPS mode with selected clock source waiting for RX data at	MCGIRCLK (4 MHz internal reference clock)	66	66	66	66	66	66	μA
	115200 baud rate. Includes selected clock source power consumption.	OSCERCLK (4 MHz external crystal)	214	237	246	254	260	268	
I _{TPM}	TPM peripheral adder measured by placing the device in STOP or VLPS mode with selected clock source configured for output	MCGIRCLK (4 MHz internal reference clock)	86	86	86	86	86	86	μA
	compare generating 100 Hz clock signal. No load is placed on the I/O generating the clock signal. Includes selected clock source and I/O switching currents.	OSCERCLK (4 MHz external crystal)	235	256	265	274	280	287	
I _{BG}	Bandgap adder when BGEN b device is placed in VLPx, LLS, mode.	it is set and or VLLSx	45	45	45	45	45	45	μA
I _{ADC}	ADC peripheral adder combini measured values at V _{DD} and V	ng the / _{DDA} by placing	366	366	366	366	366	366	μA

Table 10.	Low power mode	peripheral adders —	• typical value (continued)
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Figure 4. VLPR mode current vs. core frequency

2.2.6 EMC radiated emissions operating behaviors

 Table 11. EMC radiated emissions operating behaviors for 64-pin LQFP package

Symbol	Description	Frequency band (MHz)	Тур.	Unit	Notes
V _{RE1}	Radiated emissions voltage, band 1	0.15–50	13	dBµV	1, 2
V _{RE2}	Radiated emissions voltage, band 2	50–150	15	dBµV	
V _{RE3}	Radiated emissions voltage, band 3	150–500	12	dBµV	
V _{RE4}	Radiated emissions voltage, band 4	500–1000	7	dBµV	
V _{RE_IEC}	IEC level	0.15–1000	М	_	2, 3

 Determined according to IEC Standard 61967-1, Integrated Circuits - Measurement of Electromagnetic Emissions, 150 kHz to 1 GHz Part 1: General Conditions and Definitions and IEC Standard 61967-2, Integrated Circuits -Measurement of Electromagnetic Emissions, 150 kHz to 1 GHz Part 2: Measurement of Radiated Emissions—TEM Cell and Wideband TEM Cell Method. Measurements were made while the microcontroller was running basic



application code. The reported emission level is the value of the maximum measured emission, rounded up to the next whole number, from among the measured orientations in each frequency range.

- 2. $V_{DD} = 3.3 \text{ V}$, $T_A = 25 \text{ °C}$, $f_{OSC} = 8 \text{ MHz}$ (crystal), $f_{SYS} = 48 \text{ MHz}$, $f_{BUS} = 48 \text{ MHz}$
- 3. Specified according to Annex D of IEC Standard 61967-2, Measurement of Radiated Emissions TEM Cell and Wideband TEM Cell Method

2.2.7 Designing with radiated emissions in mind

To find application notes that provide guidance on designing your system to minimize interference from radiated emissions:

- 1. Go to www.freescale.com.
- 2. Perform a keyword search for "EMC design."

2.2.8 Capacitance attributes

Table 12. Capacitance attributes

Symbol	Description	Min.	Max.	Unit
C _{IN}	Input capacitance		7	pF

2.3 Switching specifications

2.3.1 Device clock specifications

Table 13. Device clock specifications

Symbol	Description	Min.	Max.	Unit					
	Normal run mode								
f _{SYS}	System and core clock	—	48	MHz					
f _{BUS}	Bus clock		24	MHz					
f _{FLASH}	Flash clock	—	24	MHz					
f _{LPTMR}	LPTMR clock	—	24	MHz					
	VLPR and VLPS modes ¹								
f _{SYS}	System and core clock	—	4	MHz					
f _{BUS}	Bus clock	—	1	MHz					
f _{FLASH}	Flash clock	—	1	MHz					
f _{LPTMR}	LPTMR clock ²	_	24	MHz					
f _{ERCLK}	External reference clock	_	16	MHz					



Symbol	Description	Min.	Max.	Unit
f _{LPTMR_ERCLK}	LPTMR external reference clock	—	16	MHz
f _{osc_hi_2}	Oscillator crystal or resonator frequency — high frequency mode (high range) (MCG_C2[RANGE]=1x)		16	MHz
f _{TPM}	TPM asynchronous clock	—	8	MHz
f _{UART0}	UART0 asynchronous clock	—	8	MHz

Table 13. Device clock specifications (continued)

 The frequency limitations in VLPR and VLPS modes here override any frequency specification listed in the timing specification for any other module. These same frequency limits apply to VLPS, whether VLPS was entered from RUN or from VLPR.

2. The LPTMR can be clocked at this speed in VLPR or VLPS only when the source is an external pin.

2.3.2 General switching specifications

These general-purpose specifications apply to all signals configured for GPIO and UART signals.

Table 14. General switching specifications

Description	Min.	Max.	Unit	Notes
GPIO pin interrupt pulse width (digital glitch filter disabled) — Synchronous path	1.5	—	Bus clock cycles	1
External RESET and NMI pin interrupt pulse width — Asynchronous path	100		ns	2
GPIO pin interrupt pulse width — Asynchronous path	16	_	ns	2
Port rise and fall time	_	36	ns	3

1. The greater synchronous and asynchronous timing must be met.

2. This is the shortest pulse that is guaranteed to be recognized.

3. 75 pF load

2.4 Thermal specifications

2.4.1 Thermal operating requirements

Table 15. Thermal operating requirements

Symbol	Description	Min.	Max.	Unit
TJ	Die junction temperature	-40	125	°C
T _A	Ambient temperature	-40	105	°C



Peripheral operating requirements and behaviors

Symbol	Description	Min.	Тур.	Max.	Unit	Notes
J _{acc_pll}	PLL accumulated jitter over 1µs (RMS)					10
	• f _{vco} = 48 MHz	—	1350	—	ps	
	• f _{vco} = 100 MHz	_	600	_	ps	
D _{lock}	Lock entry frequency tolerance	± 1.49	—	± 2.98	%	
D _{unl}	Lock exit frequency tolerance	± 4.47	—	± 5.97	%	
t _{pll_lock}	Lock detector detection time	_		150 × 10 ⁻⁶ + 1075(1/ f _{pll_ref})	S	11

Table 18. MCG specifications (continued)

- 1. This parameter is measured with the internal reference (slow clock) being used as a reference to the FLL (FEI clock mode).
- 2. The deviation is relative to the factory trimmed frequency at nominal V_{DD} and 25 °C, $f_{ints_{ft}}$.
- 3. These typical values listed are with the slow internal reference clock (FEI) using factory trim and DMX32 = 0.
- The resulting system clock frequencies must not exceed their maximum specified values. The DCO frequency deviation (Δf_{dco_t}) over voltage and temperature must be considered.
- 5. These typical values listed are with the slow internal reference clock (FEI) using factory trim and DMX32 = 1.
- 6. The resulting clock frequency must not exceed the maximum specified clock frequency of the device.
- 7. This specification is based on standard deviation (RMS) of period or frequency.
- 8. This specification applies to any time the FLL reference source or reference divider is changed, trim value is changed, DMX32 bit is changed, DRS bits are changed, or changing from FLL disabled (BLPE, BLPI) to FLL enabled (FEI, FEE, FBE, FBI). If a crystal/resonator is being used as the reference, this specification assumes it is already running.
- 9. Excludes any oscillator currents that are also consuming power while PLL is in operation.
- 10. This specification was obtained using a Freescale developed PCB. PLL jitter is dependent on the noise characteristics of each PCB and results will vary.
- 11. This specification applies to any time the PLL VCO divider or reference divider is changed, or changing from PLL disabled (BLPE, BLPI) to PLL enabled (PBE, PEE). If a crystal/resonator is being used as the reference, this specification assumes it is already running.

3.3.2 Oscillator electrical specifications

3.3.2.1 Oscillator DC electrical specifications

Symbol	Description	Min.	Тур.	Max.	Unit	Notes
V _{DD}	Supply voltage	1.71	—	3.6	V	
IDDOSC	Supply current — low-power mode (HGO=0)					1
	• 32 kHz	_	500	—	nA	
	• 4 MHz	_	200	—	μA	
	• 8 MHz (RANGE=01)	_	300	—	μA	
	• 16 MHz	_	950	—	μA	
		_	1.2	_	mA	

Table 19. Oscillator DC electrical specifications



3.4.1.1 Flash timing specifications — program and erase

The following specifications represent the amount of time the internal charge pumps are active and do not include command overhead.

Symbol	Description	Min.	Тур.	Max.	Unit	Notes
t _{hvpgm4}	Longword Program high-voltage time	_	7.5	18	μs	
t _{hversscr}	Sector Erase high-voltage time	_	13	113	ms	1
t _{hversall}	Erase All high-voltage time	_	52	452	ms	1

Table 21. NVM program/erase timing specifications

1. Maximum time based on expectations at cycling end-of-life.

3.4.1.2 Flash timing specifications — commands Table 22. Flash command timing specifications

Symbol	Description	Min.	Тур.	Max.	Unit	Notes
t _{rd1sec1k}	Read 1s Section execution time (flash sector)	—	—	60	μs	1
t _{pgmchk}	Program Check execution time	—	—	45	μs	1
t _{rdrsrc}	Read Resource execution time	—	—	30	μs	1
t _{pgm4}	Program Longword execution time	—	65	145	μs	_
t _{ersscr}	Erase Flash Sector execution time	—	14	114	ms	2
t _{rd1all}	Read 1s All Blocks execution time	—	—	1.8	ms	_
t _{rdonce}	Read Once execution time	—	—	25	μs	1
t _{pgmonce}	Program Once execution time	—	65	—	μs	_
t _{ersall}	Erase All Blocks execution time	—	88	650	ms	2
t _{vfykey}	Verify Backdoor Access Key execution time	—	—	30	μs	1

1. Assumes 25 MHz flash clock frequency.

2. Maximum times for erase parameters based on expectations at cycling end-of-life.

3.4.1.3 Flash high voltage current behaviors Table 23. Flash high voltage current behaviors

Symbol	Description	Min.	Тур.	Max.	Unit
I _{DD_PGM}	Average current adder during high voltage flash programming operation	—	2.5	6.0	mA
I _{DD_ERS}	Average current adder during high voltage flash erase operation		1.5	4.0	mA



- The ADC supply current depends on the ADC conversion clock speed, conversion rate and ADC_CFG1[ADLPC] (low power). For lowest power operation, ADC_CFG1[ADLPC] must be set, the ADC_CFG2[ADHSC] bit must be clear with 1 MHz ADC conversion clock speed.
- 4. 1 LSB = $(V_{REFH} V_{REFL})/2^{N}$
- 5. ADC conversion clock < 16 MHz, Max hardware averaging (AVGE = %1, AVGS = %11)
- 6. ADC conversion clock < 3 MHz



Figure 8. Typical ENOB vs. ADC_CLK for 12-bit single-ended mode

3.6.2 CMP and 6-bit DAC electrical specifications

Symbol	Description	Min.	Тур.	Max.	Unit
V _{DD}	Supply voltage	1.71	—	3.6	V
I _{DDHS}	Supply current, high-speed mode (EN = 1, PMODE = 1)	—	—	200	μA
I _{DDLS}	Supply current, low-speed mode (EN = 1, PMODE = 0)	—	—	20	μA
V _{AIN}	Analog input voltage	V _{SS}	—	V _{DD}	V
V _{AIO}	Analog input offset voltage	_	_	20	mV
V _H	Analog comparator hysteresis ¹				
	 CR0[HYSTCTR] = 00 	—	5	_	mV
	 CR0[HYSTCTR] = 01 		10	_	mV
	 CR0[HYSTCTR] = 10 		20	_	mV
	 CR0[HYSTCTR] = 11 	_	30		mV
V _{CMPOh}	Output high	V _{DD} – 0.5	—	—	V





Figure 10. Typical hysteresis vs. Vin level (V_{DD} = 3.3 V, PMODE = 1)

3.7 Timers

See General switching specifications.

3.8 Communication interfaces

3.8.1 SPI switching specifications

The Serial Peripheral Interface (SPI) provides a synchronous serial bus with master and slave operations. Many of the transfer attributes are programmable. The following tables provide timing characteristics for classic SPI timing modes. See the SPI chapter of the chip's Reference Manual for information about the modified transfer formats used for communicating with slower peripheral devices.

All timing is shown with respect to $20\% V_{DD}$ and $80\% V_{DD}$ thresholds, unless noted, as well as input signal transitions of 3 ns and a 30 pF maximum load on all SPI pins.

Num.	Symbol	Description	Min.	Max.	Unit	Note
1	f _{op}	Frequency of operation	f _{periph} /2048	f _{periph} /2	Hz	1

Table 28. SPI master mode timing on slew rate disabled pads



Peripheral operating requirements and behaviors

Characteristic	Symbol	Standa	rd Mode	Fast	Mode	Unit
		Minimum	Maximum	Minimum	Maximum	
SCL Clock Frequency	f _{SCL}	0	100	0	400 ¹	kHz
Hold time (repeated) START condition. After this period, the first clock pulse is generated.	t _{HD} ; STA	4	—	0.6	—	μs
LOW period of the SCL clock	t _{LOW}	4.7	—	1.3	—	μs
HIGH period of the SCL clock	t _{HIGH}	4	—	0.6	—	μs
Set-up time for a repeated START condition	t _{SU} ; STA	4.7	_	0.6	—	μs
Data hold time for I ² C bus devices	t _{HD} ; DAT	0 ²	3.45 ³	04	0.9 ²	μs
Data set-up time	t _{SU} ; DAT	250 ⁵	—	100 ³ , ⁶	—	ns
Rise time of SDA and SCL signals	t _r	_	1000	20 +0.1C _b ⁷	300	ns
Fall time of SDA and SCL signals	t _f	_	300	20 +0.1C _b ⁶	300	ns
Set-up time for STOP condition	t _{SU} ; STO	4	—	0.6	—	μs
Bus free time between STOP and START condition	t _{BUF}	4.7	_	1.3	—	μs
Pulse width of spikes that must be suppressed by the input filter	t _{SP}	N/A	N/A	0	50	ns

3.8.2 Inter-Integrated Circuit Interface (I2C) timing Table 32. I2C timing

1. The maximum SCL Clock Frequency in Fast mode with maximum bus loading can only achieved when using the High drive pins (see Voltage and current operating behaviors) or when using the Normal drive pins and VDD ≥ 2.7 V

The master mode I²C deasserts ACK of an address byte simultaneously with the falling edge of SCL. If no slaves
acknowledge this address byte, then a negative hold time can result, depending on the edge rates of the SDA and SCL
lines.

- 3. The maximum tHD; DAT must be met only if the device does not stretch the LOW period (tLOW) of the SCL signal.
- 4. Input signal Slew = 10 ns and Output Load = 50 pF
- 5. Set-up time in slave-transmitter mode is 1 IPBus clock period, if the TX FIFO is empty.
- 6. A Fast mode I²C bus device can be used in a Standard mode I2C bus system, but the requirement $t_{SU; DAT} \ge 250$ ns must then be met. This is automatically the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, then it must output the next data bit to the SDA line $t_{rmax} + t_{SU; DAT} = 1000 + 250 = 1250$ ns (according to the Standard mode I²C bus specification) before the SCL line is released.
- 7. C_b = total capacitance of the one bus line in pF.



Figure 15. Timing definition for fast and standard mode devices on the I²C bus





Figure 18. KL14 48-pin QFN pinout diagram



7.1 Description

Part numbers for the chip have fields that identify the specific part. You can use the values of these fields to determine the specific part you have received.

7.2 Format

Part numbers for this device have the following format:

Q KL## A FFF R T PP CC N

7.3 Fields

This table lists the possible values for each field in the part number (not all combinations are valid):

Field	Description	Values
Q	Qualification status	 M = Fully qualified, general market flow P = Prequalification
KL##	Kinetis family	• KL14
A	Key attribute	• Z = Cortex-M0+
FFF	Program flash memory size	 32 = 32 KB 64 = 64 KB
R	Silicon revision	 (Blank) = Main A = Revision after main
Т	Temperature range (°C)	• V = -40 to 105
PP	Package identifier	 FM = 32 QFN (5 mm x 5 mm) FT = 48 QFN (7 mm x 7 mm) LH = 64 LQFP (10 mm x 10 mm) LK = 80 LQFP (12 mm x 12 mm)
CC	Maximum CPU frequency (MHz)	• 4 = 48 MHz
Ν	Packaging type	 R = Tape and reel (Blank) = Trays

Table 33. Part number fields descriptions

7.4 Example

This is an example part number:



MKL14Z64VFT4

8 Terminology and guidelines

8.1 Definition: Operating requirement

An *operating requirement* is a specified value or range of values for a technical characteristic that you must guarantee during operation to avoid incorrect operation and possibly decreasing the useful life of the chip.

8.1.1 Example

This is an example of an operating requirement:

Symbol	Description	Min.	Max.	Unit
V _{DD}	1.0 V core supply voltage	0.9	1.1	V

8.2 Definition: Operating behavior

Unless otherwise specified, an *operating behavior* is a specified value or range of values for a technical characteristic that are guaranteed during operation if you meet the operating requirements and any other specified conditions.

8.2.1 Example

This is an example of an operating behavior:

Symbol	Description	Min.	Max.	Unit
I _{WP}	Digital I/O weak pullup/ pulldown current	10	130	μA



8.8 Definition: Typical value

A *typical value* is a specified value for a technical characteristic that:

- Lies within the range of values specified by the operating behavior
- Given the typical manufacturing process, is representative of that characteristic during operation when you meet the typical-value conditions or other specified conditions

Typical values are provided as design guidelines and are neither tested nor guaranteed.

8.8.1 Example 1

This is an example of an operating behavior that includes a typical value:

Symbol	Description	Min.	Тур.	Max.	Unit
I _{WP}	Digital I/O weak pullup/pulldown current	10	70	130	μΑ

8.8.2 Example 2

This is an example of a chart that shows typical values for various voltage and temperature conditions:



Revision history



8.9 Typical value conditions

Typical values assume you meet the following conditions (or other conditions as specified):

 Table 34.
 Typical value conditions

Symbol	Description	Value	Unit
T _A	Ambient temperature	25	۵°C
V _{DD}	3.3 V supply voltage	3.3	V

9 Revision history

The following table provides a revision history for this document.

Rev. No.	Date	Substantial Changes		
2	9/2012	Completed all the TBDs, initial public release.		
3	9/2012	Updated Signal Multiplexing and Pin Assignments table to add UART2 signals.		
4	3/2014	Updated the front page and restructured the chapters		
Table continues on the next page				

Table 35. Revision history

Rev. No.	Date	Substantial Changes
		 Added a note to the I_{LAT} in the ESD handling ratings Updated Voltage and current operating ratings Updated Voltage and current operating requirements Updated the Voltage and current operating behaviors Updated Power mode transition operating behaviors Updated Capacitance attributes Updated footnote in the Device clock specifications Updated Voltage and voltage and voltage and added a note to them in the 12-bit ADC operating conditions Updated Temp sensor slope and voltage and added a note to them in the 12-bit ADC operating requirements Added Inter-Integrated Circuit Interface (I2C) timing
5	08/2014	 Updated related source and added block diagram in the front page Updated Power consumption operating behaviors