E·XFL



Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

Product Status	Active
Core Processor	ARM® Cortex®-M0+
Core Size	32-Bit Single-Core
Speed	48MHz
Connectivity	I²C, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, LVD, POR, PWM, WDT
Number of I/O	40
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 3.6V
Data Converters	A/D 15x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	48-VFQFN Exposed Pad
Supplier Device Package	48-QFN (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mkl14z64vft4r

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong



Ordering Information

Part Number	Mer	nory	Maximum number of I\O's
	Flash (KB)	SRAM (KB)	
MKL14Z32VFM4	32	4	28
MKL14Z64VFM4	64	8	28
MKL14Z32VFT4	32	4	40
MKL14Z64VFT4	64	8	40
MKL14Z32VLH4	32	4	54
MKL14Z64VLH4	64	8	54
MKL14Z32VLK4	32	4	70
MKL14Z64VLK4	64	8	70

Related Resources

Туре	Description	Resource
Selector Guide	The Freescale Solution Advisor is a web-based tool that features interactive application wizards and a dynamic product selector.	Solution Advisor
Product Brief	The Product Brief contains concise overview/summary information to enable quick evaluation of a device for design suitability.	KL1 Family Product Brief ¹
Reference Manual	The Reference Manual contains a comprehensive description of the structure and function (operation) of a device.	KL14P80M48SF0RM ¹
Data Sheet	The Data Sheet includes electrical characteristics and signal connections.	KL14P80M48SF0 ¹
Chip Errata	The chip mask set Errata provides additional or corrective information for a particular device mask set.	KINETIS_L_xN97F ²
Package	Package dimensions are provided in package drawings.	QFN 32-pin: 98ASA00473D ¹
drawing		QFN 48-pin: 98ASA00466D ¹
		LQFP 64-pin: 98ASS23234W ¹
		LQFP 80-pin: 98ASS23174W ¹

1. To find the associated resource, go to http://www.freescale.com and perform a search using this term.

To find the associated resource, go to http://www.freescale.com and perform a search using this term with the "x" replaced by the revision of the device you are using.

Figure 1 shows the functional modules in the chip.



1 Ratings

1.1 Thermal handling ratings

Table 1. Thermal handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
T _{STG}	Storage temperature	-55	150	°C	1
T _{SDR}	Solder temperature, lead-free	—	260	°C	2

1. Determined according to JEDEC Standard JESD22-A103, High Temperature Storage Life.

2. Determined according to IPC/JEDEC Standard J-STD-020, Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices.

1.2 Moisture handling ratings

Table 2. Moisture handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
MSL	Moisture sensitivity level	—	3		1

1. Determined according to IPC/JEDEC Standard J-STD-020, Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices.

1.3 ESD handling ratings

Table 3. ESD handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
V _{HBM}	Electrostatic discharge voltage, human body model	-2000	+2000	V	1
V _{CDM}	Electrostatic discharge voltage, charged-device model	-500	+500	V	2
I _{LAT}	Latch-up current at ambient temperature of 105 °C	-100	+100	mA	3

1. Determined according to JEDEC Standard JESD22-A114, *Electrostatic Discharge (ESD) Sensitivity Testing Human Body Model (HBM)*.

 Determined according to JEDEC Standard JESD22-C101, Field-Induced Charged-Device Model Test Method for Electrostatic-Discharge-Withstand Thresholds of Microelectronic Components.

3. Determined according to JEDEC Standard JESD78, IC Latch-Up Test.

5



Symbol	Description	Min.	Max.	Unit	Notes
V _{DD}	Supply voltage	1.71	3.6	V	
V _{DDA}	Analog supply voltage	1.71	3.6	V	—
$V_{DD} - V_{DDA}$	V _{DD} -to-V _{DDA} differential voltage	-0.1	0.1	V	—
$V_{SS} - V_{SSA}$	V _{SS} -to-V _{SSA} differential voltage	-0.1	0.1	V	—
V _{IH}	Input high voltage				—
	• $2.7 \text{ V} \le \text{V}_{\text{DD}} \le 3.6 \text{ V}$	$0.7 \times V_{DD}$	—	V	
	• $1.7 \text{ V} \le \text{V}_{\text{DD}} \le 2.7 \text{ V}$	$0.75 \times V_{DD}$	_	V	
V _{IL}	Input low voltage				_
	• $2.7 \text{ V} \le \text{V}_{\text{DD}} \le 3.6 \text{ V}$	_	$0.35 \times V_{DD}$	V	
	• $1.7 \text{ V} \le \text{V}_{\text{DD}} \le 2.7 \text{ V}$		$0.3 \times V_{DD}$	V	
V _{HYS}	Input hysteresis	$0.06 \times V_{DD}$	_	V	_
I _{ICIO}	IO pin negative DC injection current—single pin • V _{IN} < V _{SS} –0.3V	-3	_	mA	1
I _{ICcont}	Contiguous pin DC injection current —regional limit, includes sum of negative injection currents of 16 contiguous pins • Negative current injection	-25		mA	_
V _{ODPU}	Open drain pullup voltage level	V _{DD}	V _{DD}	V	2
V _{RAM}	V _{DD} voltage required to retain RAM	1.2	_	V	—

2.2.1 Voltage and current operating requirements Table 5. Voltage and current operating requirements

2. Open drain outputs must be pulled to V_{DD} .

2.2.2 LVD and POR operating requirements T

able 6.	V _{DD} supply LVD and PO	R operating requirements
---------	-----------------------------------	---------------------------------

Symbol	Description	Min.	Тур.	Max.	Unit	Notes
V _{POR}	Falling V _{DD} POR detect voltage	0.8	1.1	1.5	V	—
V _{LVDH}	Falling low-voltage detect threshold — high range (LVDV = 01)	2.48	2.56	2.64	V	—
	Low-voltage warning thresholds — high range					1

Table continues on the next page ...

^{1.} All I/O pins are internally clamped to V_{SS} through a ESD protection diode. There is no diode connection to V_{DD} . If V_{IN} greater than V_{IO_MIN} (= V_{SS}-0.3 V) is observed, then there is no need to provide current limiting resistors at the pads. If this limit cannot be observed then a current limiting resistor is required. The negative DC injection current limiting resistor is calculated as $R = (V_{IO MIN} - V_{IN})/|I_{ICIO}|$.



Symbol	Description	Min.	Max.	Unit	Notes
V _{OL}	Output low voltage — High drive pad				1
	• 2.7 V \leq V _{DD} \leq 3.6 V, I _{OL} = 18 mA	_	0.5	V	
	• $1.71 \text{ V} \le \text{V}_{\text{DD}} \le 2.7 \text{ V}, \text{ I}_{\text{OL}} = 6 \text{ mA}$	_	0.5	V	
I _{OLT}	Output low current total for all ports	_	100	mA	—
I _{IN}	Input leakage current (per pin) for full temperature range	_	1	μA	3
I _{IN}	Input leakage current (per pin) at 25 °C	_	0.025	μA	3
I _{IN}	Input leakage current (total all pins) for full temperature range	_	65	μΑ	3
I _{OZ}	Hi-Z (off-state) leakage current (per pin)	_	1	μA	—
R _{PU}	Internal pullup resistors	20	50	kΩ	4
R _{PD}	Internal pulldown resistors	20	50	kΩ	5

Table 7. Voltage and current operating behaviors (continued)

- 1. PTB0, PTB1, PTD6, and PTD7 I/O have both high drive and normal drive capability selected by the associated PTx_PCRn[DSE] control bit. All other GPIOs are normal drive only.
- 2. The reset pin only contains an active pull down device when configured as the RESET signal or as a GPIO. When configured as a GPIO output, it acts as a pseudo open drain output.
- 3. Measured at $V_{DD} = 3.6 \text{ V}$
- 4. Measured at V_{DD} supply voltage = V_{DD} min and Vinput = V_{SS}
- 5. Measured at VDD supply voltage = VDD min and Vinput = VDD

2.2.4 Power mode transition operating behaviors

All specifications except t_{POR} and VLLSx \rightarrow RUN recovery times in the following table assume this clock configuration:

- CPU and system clocks = 48 MHz
- Bus and flash clock = 24 MHz
- FEI clock mode

POR and VLLSx \rightarrow RUN recovery use FEI clock mode at the default CPU and system frequency of 21 MHz, and a bus and flash clock frequency of 10.5 MHz.

Symbol	Description	Min.	Тур.	Max.	Unit	
t _{POR}	After a POR event, amount of time from the point V_{DD} reaches 1.8 V to execution of the first instruction across the operating temperature range of the chip.	_		300	μs	1
	• VLLS0 \rightarrow RUN	_	95	115	μs	

 Table 8. Power mode transition operating behaviors

Table continues on the next page...

9



Symbol	Description	Min.	Тур.	Max.	Unit	
	 VLLS1 → RUN 					
		—	93	115	μs	
	 VLLS3 → RUN 					
		—	42	53	μs	
	• LLS → RUN					
		—	4	4.6	μs	
	VLPS → RUN					
		—	4	4.4	μs	
	• STOP → RUN					
		—	4	4.4	μs	

 Table 8. Power mode transition operating behaviors (continued)

1. Normal boot (FTFA_FOPT[LPBOOT]=11).

2.2.5 Power consumption operating behaviors

The maximum values stated in the following table represent characterized results equivalent to the mean plus three times the standard deviation (mean + 3 sigma).

Symbol	Description	Temp.	Тур.	Max	Unit	Note
I _{DDA}	Analog supply current	—	—	See note	mA	1
I _{DD_RUNCO_} CM	Run mode current in compute operation - 48 MHz core / 24 MHz flash/ bus disabled, LPTMR running using 4 MHz internal reference clock, CoreMark® benchmark code executing from flash, at 3.0 V	_	6.4		mA	2
I _{DD_RUNCO}	Run mode current in compute operation - 48 MHz core / 24 MHz flash / bus clock disabled, code of while(1) loop executing from flash, at 3.0 V	_	3.9	4.8	mA	3
I _{DD_RUN}	Run mode current - 48 MHz core / 24 MHz bus and flash, all peripheral clocks disabled, code executing from flash, at 3.0 V	_	5	5.9	mA	3
I _{DD_RUN}	Run mode current - 48 MHz core / 24	at 25 °C	6.2	6.5	mA	3, 4
	MHz bus and flash, all peripheral clocks enabled, code executing from flash, at 3.0 V	at 125 °C	6.8	7.1	mA	

Table 9. Power consumption operating behaviors

Table continues on the next page ...





Symbol	Description			٦	Tempera	ature (°0	C)		Unit
			-40	25	50	70	85	105	
I _{IREFSTEN32KHz}	32 kHz internal reference clock Measured by entering STOP n 32 kHz IRC enabled.	(IRC) adder. node with the	52	52	52	52	52	52	μA
I _{EREFSTEN4MHz}	External 4 MHz crystal clock a Measured by entering STOP o with the crystal enabled.	dder. r VLPS mode	206	228	237	245	251	258	μA
I _{EREFSTEN32KHz}	External 32 kHz crystal clock	VLLS1	440	490	540	560	570	580	nA
	adder by means of the OSC0_CR[EREFSTEN and	VLLS3	440	490	540	560	570	580	
	EREFSTEN] bits. Measured	LLS	490	490	540	560	570	680	
	by entering all modes with the	VLPS	510	560	560	560	610	680	
	crystal enabled.	STOP	510	560	560	560	610	680	
I _{CMP}	CMP peripheral adder measur the device in VLLS1 mode with using the 6-bit DAC and a sing input for compare. Includes 6-b consumption.	ed by placing n CMP enabled le external bit DAC power	22	22	22	22	22	22	μA
I _{RTC}	RTC peripheral adder measure the device in VLLS1 mode with kHz crystal enabled by means RTC_CR[OSCE] bit and the R for 1 minute. Includes ERCLK3 external crystal) power consum	ed by placing n external 32 of the TC ALARM set 32K (32 kHz nption.	432	357	388	475	532	810	nA
I _{UART}	UART peripheral adder measured by placing the device in STOP or VLPS mode with selected clock source waiting for RX data at	MCGIRCLK (4 MHz internal reference clock)	66	66	66	66	66	66	μA
	115200 baud rate. Includes selected clock source power consumption.	OSCERCLK (4 MHz external crystal)	214	237	246	254	260	268	
I _{TPM}	TPM peripheral adder measured by placing the device in STOP or VLPS mode with selected clock source configured for output	MCGIRCLK (4 MHz internal reference clock)	86	86	86	86	86	86	μA
	compare generating 100 Hz clock signal. No load is placed on the I/O generating the clock signal. Includes selected clock source and I/O switching currents.	OSCERCLK (4 MHz external crystal)	235	256	265	274	280	287	
I _{BG}	Bandgap adder when BGEN b device is placed in VLPx, LLS, mode.	it is set and or VLLSx	45	45	45	45	45	45	μA
I _{ADC}	ADC peripheral adder combini measured values at V _{DD} and V	ng the / _{DDA} by placing	366	366	366	366	366	366	μA

Table 10.	Low power mode	peripheral adders —	 typical value (continued)
-----------	----------------	---------------------	---



Symbol	Description	Temperature (°C)					Unit	
		-40	25	50	70	85	105	
	the device in STOP or VLPS mode. ADC is configured for low power mode using the internal clock and continuous conversions.							

Table 10. Low power mode peripheral adders — typical value

2.2.5.1 Diagram: Typical IDD_RUN operating behavior

The following data was measured under these conditions:

- MCG in FBE for run mode, and BLPE for VLPR mode
- No GPIOs toggled
- Code execution from flash with cache enabled
- For the ALLOFF curve, all peripheral clocks are disabled except FTFA







Symbol	Description	Min.	Max.	Unit
f _{LPTMR_ERCLK}	LPTMR external reference clock	—	16	MHz
f _{osc_hi_2}	Oscillator crystal or resonator frequency — high frequency mode (high range) (MCG_C2[RANGE]=1x)		16	MHz
f _{TPM}	TPM asynchronous clock	—	8	MHz
f _{UART0}	UART0 asynchronous clock	—	8	MHz

Table 13. Device clock specifications (continued)

 The frequency limitations in VLPR and VLPS modes here override any frequency specification listed in the timing specification for any other module. These same frequency limits apply to VLPS, whether VLPS was entered from RUN or from VLPR.

2. The LPTMR can be clocked at this speed in VLPR or VLPS only when the source is an external pin.

2.3.2 General switching specifications

These general-purpose specifications apply to all signals configured for GPIO and UART signals.

Table 14. General switching specifications

Description	Min.	Max.	Unit	Notes
GPIO pin interrupt pulse width (digital glitch filter disabled) — Synchronous path	1.5	—	Bus clock cycles	1
External RESET and NMI pin interrupt pulse width — Asynchronous path	100		ns	2
GPIO pin interrupt pulse width — Asynchronous path	16	_	ns	2
Port rise and fall time	_	36	ns	3

1. The greater synchronous and asynchronous timing must be met.

2. This is the shortest pulse that is guaranteed to be recognized.

3. 75 pF load

2.4 Thermal specifications

2.4.1 Thermal operating requirements

Table 15. Thermal operating requirements

Symbol	Description	Min.	Max.	Unit
TJ	Die junction temperature	-40	125	°C
T _A	Ambient temperature	-40	105	°C



2.4.2 Thermal attributes

Table 16. Thern	nal attributes
-----------------	----------------

Board type	Symbol	Description	80 LQFP	64 LQFP	48 QFN	32 QFN	Unit	Notes
Single-layer (1S)	R _{θJA}	Thermal resistance, junction to ambient (natural convection)	70	71	84	92	°C/W	1
Four-layer (2s2p)	R _{θJA}	Thermal resistance, junction to ambient (natural convection)	53	52	28	33	°C/W	
Single-layer (1S)	R _{θJMA}	Thermal resistance, junction to ambient (200 ft./min. air speed)	_	59	69	75	°C/W	
Four-layer (2s2p)	R _{θJMA}	Thermal resistance, junction to ambient (200 ft./min. air speed)	—	46	22	27	°C/W	
_	R _{θJB}	Thermal resistance, junction to board	34	34	10	12	°C/W	2
	R _{θJC}	Thermal resistance, junction to case	15	20	2.0	1.8	°C/W	3
_	Ψ_{JT}	Thermal characterization parameter, junction to package top outside center (natural convection)	0.6	5	5.0	8	°C/W	4

1. Determined according to JEDEC Standard JESD51-2, Integrated Circuits Thermal Test Method Environmental Conditions—Natural Convection (Still Air), or EIA/JEDEC Standard JESD51-6, Integrated Circuit Thermal Test Method Environmental Conditions—Forced Convection (Moving Air).

- 2. Determined according to JEDEC Standard JESD51-8, Integrated Circuit Thermal Test Method Environmental Conditions—Junction-to-Board.
- 3. Determined according to Method 1012.1 of MIL-STD 883, *Test Method Standard, Microcircuits*, with the cold plate temperature used for the case temperature. The value includes the thermal resistance of the interface material between the top of the package and the cold plate.
- 4. Determined according to JEDEC Standard JESD51-2, Integrated Circuits Thermal Test Method Environmental Conditions—Natural Convection (Still Air).

3 Peripheral operating requirements and behaviors

3.1 Core modules



3.4.1.1 Flash timing specifications — program and erase

The following specifications represent the amount of time the internal charge pumps are active and do not include command overhead.

Symbol	Description	Min.	Тур.	Max.	Unit	Notes
t _{hvpgm4}	Longword Program high-voltage time	_	7.5	18	μs	
t _{hversscr}	Sector Erase high-voltage time	_	13	113	ms	1
t _{hversall}	Erase All high-voltage time	_	52	452	ms	1

Table 21. NVM program/erase timing specifications

1. Maximum time based on expectations at cycling end-of-life.

3.4.1.2 Flash timing specifications — commands Table 22. Flash command timing specifications

Symbol	Description	Min.	Тур.	Max.	Unit	Notes
t _{rd1sec1k}	Read 1s Section execution time (flash sector)	—	—	60	μs	1
t _{pgmchk}	Program Check execution time	—	—	45	μs	1
t _{rdrsrc}	Read Resource execution time	—	—	30	μs	1
t _{pgm4}	Program Longword execution time	—	65	145	μs	_
t _{ersscr}	Erase Flash Sector execution time	—	14	114	ms	2
t _{rd1all}	Read 1s All Blocks execution time	_	—	1.8	ms	_
t _{rdonce}	Read Once execution time	—	—	25	μs	1
t _{pgmonce}	Program Once execution time	—	65	—	μs	_
t _{ersall}	Erase All Blocks execution time	—	88	650	ms	2
t _{vfykey}	Verify Backdoor Access Key execution time	—	—	30	μs	1

1. Assumes 25 MHz flash clock frequency.

2. Maximum times for erase parameters based on expectations at cycling end-of-life.

3.4.1.3 Flash high voltage current behaviors Table 23. Flash high voltage current behaviors

Symbol	Description	Min.	Тур.	Max.	Unit
I _{DD_PGM}	Average current adder during high voltage flash programming operation	—	2.5	6.0	mA
I _{DD_ERS}	Average current adder during high voltage flash erase operation		1.5	4.0	mA

Num.	Symbol	Description	Min.	Max.	Unit	Note
2	t _{SPSCK}	SPSCK period	2 x t _{periph}	2048 x	ns	2
				^I periph		
3	t _{Lead}	Enable lead time	1/2		t _{SPSCK}	—
4	t _{Lag}	Enable lag time	1/2		t _{SPSCK}	—
5	t _{WSPSCK}	Clock (SPSCK) high or low time	t _{periph} – 30	1024 x	ns	—
				t _{periph}		
6	t _{SU}	Data setup time (inputs)	16	—	ns	—
7	t _{HI}	Data hold time (inputs)	0	—	ns	
8	t _v	Data valid (after SPSCK edge)	—	10	ns	—
9	t _{HO}	Data hold time (outputs)	0	_	ns	—
10	t _{RI}	Rise time input	—	t _{periph} – 25	ns	_
	t _{FI}	Fall time input				
11	t _{RO}	Rise time output	—	25	ns	—
	t _{FO}	Fall time output]			

Table 28. SPI master mode timing on slew rate disabled pads (continued)

1. For SPI0, f_{periph} is the bus clock (f_{BUS}). For SPI1 f_{periph} is the system clock (f_{SYS}).

2. $t_{periph} = 1/f_{periph}$

Table 29. SPI master mode timing on slew rate enabled pads

Num.	Symbol	Description	Min.	Max.	Unit	Note
1	f _{op}	Frequency of operation	f _{periph} /2048	f _{periph} /2	Hz	1
2	t _{SPSCK}	SPSCK period	2 x t _{periph}	2048 x t _{periph}	ns	2
3	t _{Lead}	Enable lead time	1/2	—	t _{SPSCK}	—
4	t _{Lag}	Enable lag time	1/2	—	t _{SPSCK}	
5	t _{WSPSCK}	Clock (SPSCK) high or low time	t _{periph} – 30	1024 x t _{periph}	ns	_
6	t _{SU}	Data setup time (inputs)	96	—	ns	—
7	t _{HI}	Data hold time (inputs)	0	—	ns	—
8	t _v	Data valid (after SPSCK edge)	—	52	ns	—
9	t _{HO}	Data hold time (outputs)	0	—	ns	—
10	t _{RI}	Rise time input	—	t _{periph} – 25	ns	—
	t _{FI}	Fall time input				
11	t _{RO}	Rise time output	_	36	ns	_
	t _{FO}	Fall time output				

1. For SPI0, f_{periph} is the bus clock (f_{BUS}). For SPI1 f_{periph} is the system clock (f_{SYS}).

2. $t_{periph} = 1/f_{periph}$





1. If configured as an output.

2. LSBF = 0. For LSBF = 1, bit order is LSB, bit 1, ..., bit 6, MSB.





1.If configured as output

2. LSBF = 0. For LSBF = 1, bit order is LSB, bit 1, ..., bit 6, MSB.

Figure 12. SPI master mode timing (CPHA = 1)

Table 30.	SPI slave	mode	timing of	on slew	rate	disabled	pads
-----------	-----------	------	-----------	---------	------	----------	------

Num.	Symbol	Description	Min.	Max.	Unit	Note
1	f _{op}	Frequency of operation	0	f _{periph} /4	Hz	1
2	t _{SPSCK}	SPSCK period	4 x t _{periph}	_	ns	2
3	t _{Lead}	Enable lead time	1		t _{periph}	_

Table continues on the next page ...





3.8.3 UART

See General switching specifications.

4 Dimensions

4.1 Obtaining package dimensions

Package dimensions are provided in package drawings.

To find a package drawing, go to **freescale.com** and perform a keyword search for the drawing's document number:

If you want the drawing for this package	Then use this document number
32-pin QFN	98ASA00473D
48-pin QFN	98ASA00466D
64-pin LQFP	98ASS23234W
80-pin LQFP	98ASS23174W

5 Pinout

5.1 KL14 Signal Multiplexing and Pin Assignments

The following table shows the signals available on each pin and the locations of these pins on the devices supported by this document. The Port Control Module is responsible for selecting which ALT functionality is available on each pin.

80 LQFP	64 LQFP	48 QFN	32 QFN	Pin Name	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7
1	1	-	1	PTE0	DISABLED		PTE0		UART1_TX	RTC_ CLKOUT	CMP0_OUT	I2C1_SDA	
2	2	—	2	PTE1	DISABLED		PTE1	SPI1_MOSI	UART1_RX		SPI1_MISO	I2C1_SCL	
3	_	-	-	PTE2	DISABLED		PTE2	SPI1_SCK					
4	_	-	-	PTE3	DISABLED		PTE3	SPI1_MISO			SPI1_MOSI		
5	_	-	-	PTE4	DISABLED		PTE4	SPI1_PCS0					

80 LQFP	64 LQFP	48 QFN	32 QFN	Pin Name	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7
41	33	25	18	PTA19	XTAL0	XTAL0	PTA19		UART1_TX	TPM_ CLKIN1		LPTMR0_ ALT1	
42	34	26	19	RESET_b	RESET_b		PTA20						
43	35	27	20	PTB0/ LLWU_P5	ADC0_SE8	ADC0_SE8	PTB0/ LLWU_P5	I2C0_SCL	TPM1_CH0				
44	36	28	21	PTB1	ADC0_SE9	ADC0_SE9	PTB1	I2C0_SDA	TPM1_CH1				
45	37	29	-	PTB2	ADC0_SE12	ADC0_SE12	PTB2	I2C0_SCL	TPM2_CH0				
46	38	30	_	PTB3	ADC0_SE13	ADC0_SE13	PTB3	I2C0_SDA	TPM2_CH1				
47	_	_	_	PTB8	DISABLED		PTB8		EXTRG_IN				
48	_	-	_	PTB9	DISABLED		PTB9						
49	_	_	_	PTB10	DISABLED		PTB10	SPI1_PCS0					
50	_	-	-	PTB11	DISABLED		PTB11	SPI1_SCK					
51	39	31	_	PTB16	DISABLED		PTB16	SPI1_MOSI	UART0_RX	TPM_ CLKIN0	SPI1_MISO		
52	40	32	1	PTB17	DISABLED		PTB17	SPI1_MISO	UART0_TX	TPM_ CLKIN1	SPI1_MOSI		
53	41	—	—	PTB18	DISABLED		PTB18		TPM2_CH0				
54	42	-	-	PTB19	DISABLED		PTB19		TPM2_CH1				
55	43	33	-	PTC0	ADC0_SE14	ADC0_SE14	PTC0		EXTRG_IN		CMP0_OUT		
56	44	34	22	PTC1/ LLWU_P6/ RTC_CLKIN	ADC0_SE15	ADC0_SE15	PTC1/ LLWU_P6/ RTC_CLKIN	I2C1_SCL		TPM0_CH0			
57	45	35	23	PTC2	ADC0_SE11	ADC0_SE11	PTC2	I2C1_SDA		TPM0_CH1			
58	46	36	24	PTC3/ LLWU_P7	DISABLED		PTC3/ LLWU_P7		UART1_RX	TPM0_CH2	CLKOUT		
59	47	—	—	VSS	VSS	VSS							
60	48	-	_	VDD	VDD	VDD							
61	49	37	25	PTC4/ LLWU_P8	DISABLED		PTC4/ LLWU_P8	SPI0_PCS0	UART1_TX	TPM0_CH3			
62	50	38	26	PTC5/ LLWU_P9	DISABLED		PTC5/ LLWU_P9	SPI0_SCK	LPTMR0_ ALT2			CMP0_OUT	
63	51	39	27	PTC6/ LLWU_P10	CMP0_IN0	CMP0_IN0	PTC6/ LLWU_P10	SPI0_MOSI	EXTRG_IN		SPI0_MISO		
64	52	40	28	PTC7	CMP0_IN1	CMP0_IN1	PTC7	SPI0_MISO			SPI0_MOSI		
65	53	1	-	PTC8	CMP0_IN2	CMP0_IN2	PTC8	I2C0_SCL	TPM0_CH4				
66	54	-	_	PTC9	CMP0_IN3	CMP0_IN3	PTC9	I2C0_SDA	TPM0_CH5				
67	55	_	—	PTC10	DISABLED		PTC10	I2C1_SCL					
68	56	_	-	PTC11	DISABLED		PTC11	I2C1_SDA					
69	-	—	—	PTC12	DISABLED		PTC12			TPM_ CLKIN0			
70	-	-	-	PTC13	DISABLED		PTC13			TPM_ CLKIN1			
71	-	-	-	PTC16	DISABLED		PTC16						

Kinetis KL14 Sub-Family, Rev5 08/2014.

P



80 LQFP	64 LQFP	48 QFN	32 QFN	Pin Name	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7
72	-	_	-	PTC17	DISABLED		PTC17						
73	57	41	_	PTD0	DISABLED		PTD0	SPI0_PCS0		TPM0_CH0			
74	58	42	_	PTD1	ADC0_SE5b	ADC0_SE5b	PTD1	SPI0_SCK		TPM0_CH1			
75	59	43	_	PTD2	DISABLED		PTD2	SPI0_MOSI	UART2_RX	TPM0_CH2	SPI0_MISO		
76	60	44	-	PTD3	DISABLED		PTD3	SPI0_MISO	UART2_TX	TPM0_CH3	SPI0_MOSI		
77	61	45	29	PTD4/ LLWU_P14	DISABLED		PTD4/ LLWU_P14	SPI1_PCS0	UART2_RX	TPM0_CH4			
78	62	46	30	PTD5	ADC0_SE6b	ADC0_SE6b	PTD5	SPI1_SCK	UART2_TX	TPM0_CH5			
79	63	47	31	PTD6/ LLWU_P15	ADC0_SE7b	ADC0_SE7b	PTD6/ LLWU_P15	SPI1_MOSI	UART0_RX		SPI1_MISO		
80	64	48	32	PTD7	DISABLED		PTD7	SPI1_MISO	UART0_TX		SPI1_MOSI		

5.2 KL14 pinouts

The following figures show the pinout diagrams for the devices supported by this document. Many signals may be multiplexed onto a single pin. To determine what signals can be used on which pin, see KL14 Signal Multiplexing and Pin Assignments.





Figure 17. KL14 64-pin LQFP pinout diagram





Figure 19. KL14 32-pin QFN pinout diagram

6 Ordering parts

6.1 Determining valid orderable parts

Valid orderable part numbers are provided on the web. To determine the orderable part numbers for this device, go to **freescale.com** and perform a part number search for the following device numbers: PKL14 and MKL14

7 Part identification



7.1 Description

Part numbers for the chip have fields that identify the specific part. You can use the values of these fields to determine the specific part you have received.

7.2 Format

Part numbers for this device have the following format:

Q KL## A FFF R T PP CC N

7.3 Fields

This table lists the possible values for each field in the part number (not all combinations are valid):

Field	Description	Values
Q	Qualification status	 M = Fully qualified, general market flow P = Prequalification
KL##	Kinetis family	• KL14
A	Key attribute	• Z = Cortex-M0+
FFF	Program flash memory size	 32 = 32 KB 64 = 64 KB
R	Silicon revision	 (Blank) = Main A = Revision after main
Т	Temperature range (°C)	• V = -40 to 105
PP	Package identifier	 FM = 32 QFN (5 mm x 5 mm) FT = 48 QFN (7 mm x 7 mm) LH = 64 LQFP (10 mm x 10 mm) LK = 80 LQFP (12 mm x 12 mm)
CC	Maximum CPU frequency (MHz)	• 4 = 48 MHz
Ν	Packaging type	 R = Tape and reel (Blank) = Trays

Table 33. Part number fields descriptions

7.4 Example

This is an example part number:



8.8 Definition: Typical value

A *typical value* is a specified value for a technical characteristic that:

- Lies within the range of values specified by the operating behavior
- Given the typical manufacturing process, is representative of that characteristic during operation when you meet the typical-value conditions or other specified conditions

Typical values are provided as design guidelines and are neither tested nor guaranteed.

8.8.1 Example 1

This is an example of an operating behavior that includes a typical value:

Symbol	Description	Min.	Тур.	Max.	Unit
I _{WP}	Digital I/O weak pullup/pulldown current	10	70	130	μΑ

8.8.2 Example 2

This is an example of a chart that shows typical values for various voltage and temperature conditions:



Revision history



8.9 Typical value conditions

Typical values assume you meet the following conditions (or other conditions as specified):

 Table 34.
 Typical value conditions

Symbol	Description	Value	Unit
T _A	Ambient temperature	25	۵°C
V _{DD}	3.3 V supply voltage	3.3	V

9 Revision history

The following table provides a revision history for this document.

Rev. No.	Date	Substantial Changes				
2	9/2012	Completed all the TBDs, initial public release.				
3	9/2012	Updated Signal Multiplexing and Pin Assignments table to add UART2 signals.				
4	4 3/2014 • Updated the front page and restructured the chapters					
Table continues on the next page						

Table 35. Revision history