

Welcome to [E-XFL.COM](https://www.e-xfl.com)

Understanding [Embedded - CPLDs \(Complex Programmable Logic Devices\)](#)

Embedded - CPLDs, or Complex Programmable Logic Devices, are highly versatile digital logic devices used in electronic systems. These programmable components are designed to perform complex logical operations and can be customized for specific applications. Unlike fixed-function ICs, CPLDs offer the flexibility to reprogram their configuration, making them an ideal choice for various embedded systems. They consist of a set of logic gates and programmable interconnects, allowing designers to implement complex logic circuits without needing custom hardware.

Applications of Embedded - CPLDs

Details

Product Status	Obsolete
Programmable Type	In System Programmable
Delay Time tpd(1) Max	3.5 ns
Voltage Supply - Internal	2.375V ~ 2.625V
Number of Logic Elements/Blocks	2
Number of Macrocells	32
Number of Gates	600
Number of I/O	36
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	49-LFBGA
Supplier Device Package	49-UBGA (7x7)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=epm7032buc49-3

MAX 7000B devices provide programmable speed/power optimization. Speed-critical portions of a design can run at high speed/full power, while the remaining portions run at reduced speed/low power. This speed/power optimization feature enables the designer to configure one or more macrocells to operate up to 50% lower power while adding only a nominal timing delay. MAX 7000B devices also provide an option that reduces the slew rate of the output buffers, minimizing noise transients when non-speed-critical signals are switching. The output drivers of all MAX 7000B devices can be set for 3.3 V, 2.5 V, or 1.8 V and all input pins are 3.3-V, 2.5-V, and 1.8-V tolerant, allowing MAX 7000B devices to be used in mixed-voltage systems.

MAX 7000B devices are supported by Altera development systems, which are integrated packages that offer schematic, text—including VHDL, Verilog HDL, and the Altera Hardware Description Language (AHDL)—and waveform design entry, compilation and logic synthesis, simulation and timing analysis, and device programming. Altera software provides EDIF 2.0.0 and 3.0.0, LPM, VHDL, Verilog HDL, and other interfaces for additional design entry and simulation support from other industry-standard PC- and UNIX-workstation-based EDA tools. Altera software runs on Windows-based PCs, as well as Sun SPARCstation, and HP 9000 Series 700/800 workstations.



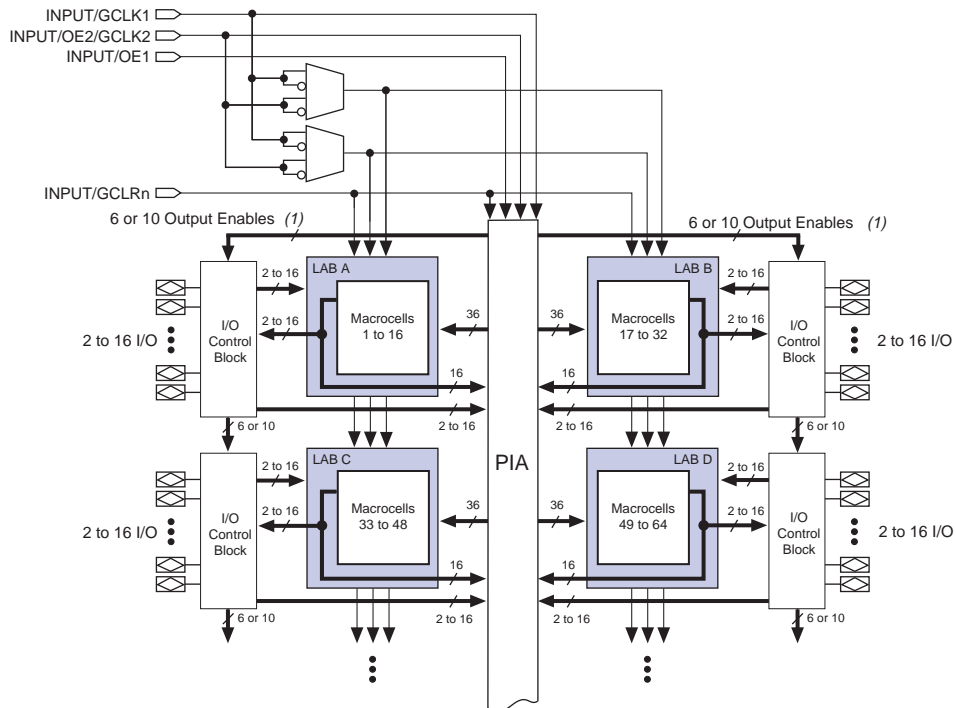
For more information on development tools, see the *MAX+PLUS II Programmable Logic Development System & Software Data Sheet* and the *Quartus Programmable Logic Development System & Software Data Sheet*.

Functional Description

The MAX 7000B architecture includes the following elements:

- LABs
- Macrocells
- Expander product terms (shareable and parallel)
- PIA
- I/O control blocks

The MAX 7000B architecture includes four dedicated inputs that can be used as general-purpose inputs or as high-speed, global control signals (clock, clear, and two output enable signals) for each macrocell and I/O pin. [Figure 1](#) shows the architecture of MAX 7000B devices.

Figure 1. MAX 7000B Device Block Diagram**Note:**

- (1) EPM7032B, EPM7064B, EPM7128B, and EPM7256B devices have six output enables. EPM7512B devices have ten output enables.

Logic Array Blocks

The MAX 7000B device architecture is based on the linking of high-performance LABs. LABs consist of 16 macrocell arrays, as shown in [Figure 1](#). Multiple LABs are linked together via the PIA, a global bus that is fed by all dedicated input pins, I/O pins, and macrocells.

Each LAB is fed by the following signals:

- 36 signals from the PIA that are used for general logic inputs
- Global controls that are used for secondary register functions
- Direct input paths from I/O pins to the registers that are used for fast setup times

Parallel Expanders

Parallel expanders are unused product terms that can be allocated to a neighboring macrocell to implement fast, complex logic functions. Parallel expanders allow up to 20 product terms to directly feed the macrocell OR logic, with five product terms provided by the macrocell and 15 parallel expanders provided by neighboring macrocells in the LAB.

The Altera Compiler can automatically allocate up to three sets of up to five parallel expanders to the macrocells that require additional product terms. Each set of five parallel expanders incurs a small, incremental timing delay (t_{PEXP}). For example, if a macrocell requires 14 product terms, the Compiler uses the five dedicated product terms within the macrocell and allocates two sets of parallel expanders; the first set includes five product terms and the second set includes four product terms, increasing the total delay by $2 \times t_{PEXP}$.

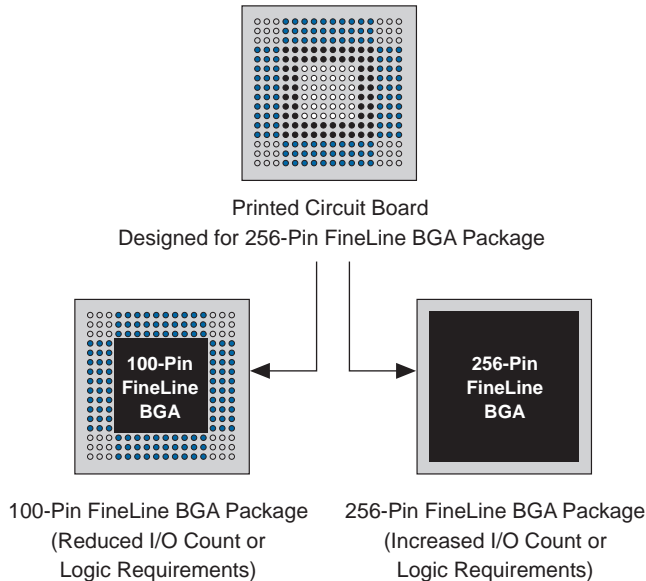
Two groups of eight macrocells within each LAB (e.g., macrocells 1 through 8, and 9 through 16) form two chains to lend or borrow parallel expanders. A macrocell borrows parallel expanders from lower-numbered macrocells. For example, macrocell 8 can borrow parallel expanders from macrocell 7, from macrocells 7 and 6, or from macrocells 7, 6, and 5. Within each group of eight, the lowest-numbered macrocell can only lend parallel expanders and the highest-numbered macrocell can only borrow them. [Figure 4](#) shows how parallel expanders can be borrowed from a neighboring macrocell.

SameFrame Pin-Outs

MAX 7000B devices support the SameFrame pin-out feature for FineLine BGA and 0.8-mm Ultra FineLine BGA packages. The SameFrame pin-out feature is the arrangement of balls on FineLine BGA and 0.8-mm Ultra FineLine BGA packages such that the lower-ball-count packages form a subset of the higher-ball-count packages. SameFrame pin-outs provide the flexibility to migrate not only from device to device within the same package, but also from one package to another. FineLine BGA packages are compatible with other FineLine BGA packages, and 0.8-mm Ultra FineLine BGA packages are compatible with other 0.8-mm Ultra FineLine BGA packages. A given printed circuit board (PCB) layout can support multiple device density / package combinations. For example, a single board layout can support a range of devices from an EPM7064B device in a 100-pin FineLine BGA package to an EPM7512B device in a 256-pin FineLine BGA package.

The Altera software provides support to design PCBs with SameFrame pin-out devices. Devices can be defined for present and future use. The Altera software generates pin-outs describing how to layout a board to take advantage of this migration (see [Figure 7](#)).

Figure 7. SameFrame Pin-Out Example



Programming with External Hardware



MAX 7000B devices can be programmed on Windows-based PCs with an Altera Logic Programmer card, the Master Programming Unit (MPU), and the appropriate device adapter. The MPU performs continuity checking to ensure adequate electrical contact between the adapter and the device.

For more information, see the [Altera Programming Hardware Data Sheet](#).

The Altera software can use text- or waveform-format test vectors created with the Altera Text Editor or Waveform Editor to test the programmed device. For added design verification, designers can perform functional testing to compare the functional device behavior with the results of simulation.

Data I/O, BP Microsystems, and other programming hardware manufacturers provide programming support for Altera devices. For more information, see [Programming Hardware Manufacturers](#).

IEEE Std. 1149.1 (JTAG) Boundary-Scan Support

MAX 7000B devices include the JTAG boundary-scan test circuitry defined by IEEE Std. 1149.1. [Table 6](#) describes the JTAG instructions supported by MAX 7000B devices. The pin-out tables starting on [page 59](#) of this data sheet show the location of the JTAG control pins for each device. If the JTAG interface is not required, the JTAG pins are available as user I/O pins.

Table 6. MAX 7000B JTAG Instructions

JTAG Instruction	Description
SAMPLE/PRELOAD	Allows a snapshot of signals at the device pins to be captured and examined during normal device operation, and permits an initial data pattern output at the device pins.
EXTEST	Allows the external circuitry and board-level interconnections to be tested by forcing a test pattern at the output pins and capturing test results at the input pins.
BYPASS	Places the 1-bit bypass register between the TDI and TDO pins, which allows the boundary-scan test data to pass synchronously through a selected device to adjacent devices during normal operation.
CLAMP	Allows the values in the boundary-scan register to determine pin states while placing the 1-bit bypass register between the TDI and TDO pins.
IDCODE	Selects the IDCODE register and places it between the TDI and TDO pins, allowing the IDCODE to be serially shifted out of TDO.
USERCODE	Selects the 32-bit USERCODE register and places it between the TDI and TDO pins, allowing the USERCODE value to be shifted out of TDO.
ISP Instructions	These instructions are used when programming MAX 7000B devices via the JTAG ports with the MasterBlaster or ByteBlasterMV download cable, or using a Jam File (.jam), Jam Byte-Code File (.jbc), or Serial Vector Format File (.svf) via an embedded processor or test equipment.

Programmable Speed/Power Control

MAX 7000B devices offer a power-saving mode that supports low-power operation across user-defined signal paths or the entire device. This feature allows total power dissipation to be reduced by 50% or more, because most logic applications require only a small fraction of all gates to operate at maximum frequency.

The designer can program each individual macrocell in a MAX 7000B device for either high-speed or low-power operation. As a result, speed-critical paths in the design can run at high speed, while the remaining paths can operate at reduced power. Macrocells that run at low power incur a nominal timing delay adder (t_{LPA}) for the t_{LAD} , t_{LAC} , t_{IC} , t_{ACL} , t_{CPW} , t_{EN} , and t_{SEXP} parameters.

Output Configuration

MAX 7000B device outputs can be programmed to meet a variety of system-level requirements.

MultiVolt I/O Interface

The MAX 7000B device architecture supports the MultiVolt I/O interface feature, which allows MAX 7000B devices to connect to systems with differing supply voltages. MAX 7000B devices in all packages can be set for 3.3-V, 2.5-V, or 1.8-V pin operation. These devices have one set of V_{CC} pins for internal operation and input buffers (V_{CCINT}), and another set for I/O output drivers (V_{CCIO}).

The V_{CCIO} pins can be connected to either a 3.3-V, 2.5-V, or 1.8-V power supply, depending on the output requirements. When the V_{CCIO} pins are connected to a 1.8-V power supply, the output levels are compatible with 1.8-V systems. When the V_{CCIO} pins are connected to a 2.5-V power supply, the output levels are compatible with 2.5-V systems. When the V_{CCIO} pins are connected to a 3.3-V power supply, the output high is at 3.3 V and is therefore compatible with 3.3-V or 5.0-V systems. Devices operating with V_{CCIO} levels of 2.5 V or 1.8 V incur a nominal timing delay adder.

Table 10 describes the MAX 7000B MultiVolt I/O support.

Table 10. MAX 7000B MultiVolt I/O Support

V_{CCIO} (V)	Input Signal (V)				Output Signal (V)			
	1.8	2.5	3.3	5.0	1.8	2.5	3.3	5.0
1.8	✓	✓	✓		✓			
2.5	✓	✓	✓			✓		
3.3	✓	✓	✓				✓	✓

Open-Drain Output Option

MAX 7000B devices provide an optional open-drain (equivalent to open-collector) output for each I/O pin. This open-drain output enables the device to provide system-level control signals (e.g., interrupt and write enable signals) that can be asserted by any of several devices. It can also provide an additional wired-OR plane.

Programmable Ground Pins

Each unused I/O pin on MAX 7000B devices may be used as an additional ground pin. This programmable ground feature does not require the use of the associated macrocell; therefore, the buried macrocell is still available for user logic.

Slew-Rate Control

The output buffer for each MAX 7000B I/O pin has an adjustable output slew rate that can be configured for low-noise or high-speed performance. A faster slew rate provides high-speed transitions for high-performance systems. However, these fast transitions may introduce noise transients into the system. A slow slew rate reduces system noise, but adds a nominal delay of 4 to 5 ns. When the configuration cell is turned off, the slew rate is set for low-noise performance. Each I/O pin has an individual EEPROM bit that controls the slew rate, allowing designers to specify the slew rate on a pin-by-pin basis. The slew rate control affects both the rising and falling edges of the output signal.

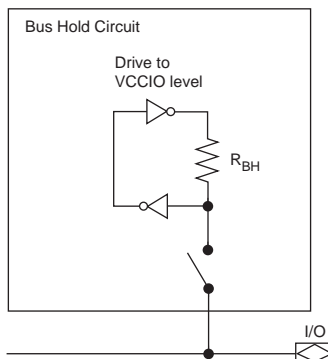
Advanced I/O Standard Support

The MAX 7000B I/O pins support the following I/O standards: LVTTTL, LVCMOS, 1.8-V I/O, 2.5-V I/O, GTL+, SSTL-3 Class I and II, and SSTL-2 Class I and II.

Two inverters implement the bus-hold circuitry in a loop that weakly drives back to the I/O pin in user mode.

Figure 10 shows a block diagram of the bus-hold circuit.

Figure 10. Bus-Hold Circuit



PCI Compatibility

MAX 7000B devices are compatible with PCI applications as well as all 3.3-V electrical specifications in the *PCI Local Bus Specification Revision 2.2* except for the clamp diode. While having multiple clamp diodes on a signal trace may be redundant, designers can add an external clamp diode to meet the specification. Table 13 shows the MAX 7000B device speed grades that meet the PCI timing specifications.

Table 13. MAX 7000B Device Speed Grades that Meet PCI Timing Specifications

Device	Specification	
	33-MHz PCI	66-MHz PCI
EPM7032B	All speed grades	-3
EPM7064B	All speed grades	-3
EPM7128B	All speed grades	-4
EPM7256B	All speed grades	-5 (1)
EPM7512B	All speed grades	-5 (1)

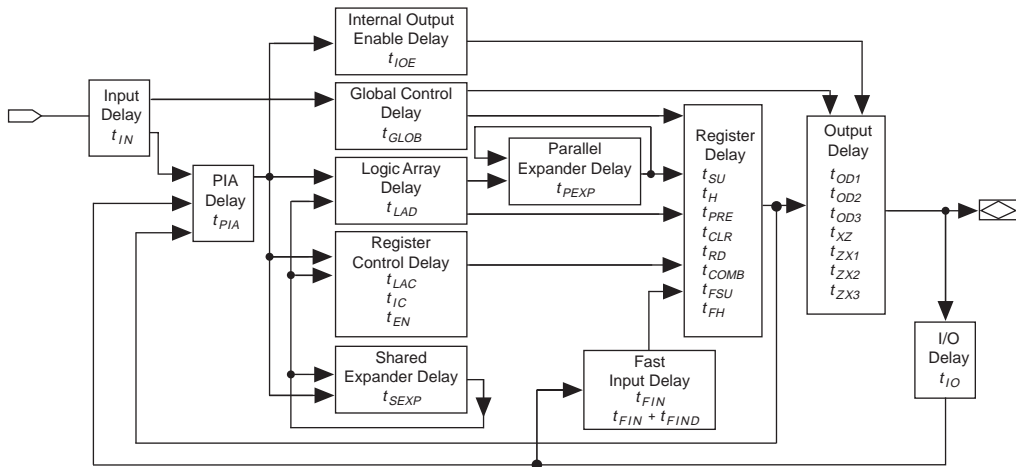
Note:

- (1) The EPM7256B and EPM7512B devices in a -5 speed grade meet all PCI timing specifications for 66-MHz operation except the Input Setup Time to CLK—Bused Signal parameter. However, these devices are within 1 ns of that parameter. EPM7256B and EPM7512B devices meet all other 66-MHz PCI timing specifications.

Timing Model

MAX 7000B device timing can be analyzed with the Altera software, with a variety of popular industry-standard EDA simulators and timing analyzers, or with the timing model shown in Figure 13. MAX 7000B devices have predictable internal delays that enable the designer to determine the worst-case timing of any design. The Altera software provides timing simulation, point-to-point delay prediction, and detailed timing analysis for device-wide performance evaluation.

Figure 13. MAX 7000B Timing Model



The timing characteristics of any signal path can be derived from the timing model and parameters of a particular device. External timing parameters, which represent pin-to-pin timing delays, can be calculated as the sum of internal parameters. Figure 14 shows the timing relationship between internal and external delay parameters.



See [Application Note 94 \(Understanding MAX 7000 Timing\)](#) for more information.

Table 19. EPM7032B Internal Timing Parameters *Notes (1)*

Symbol	Parameter	Conditions	Speed Grade						Unit
			-3.5		-5.0		-7.5		
			Min	Max	Min	Max	Min	Max	
t_{IN}	Input pad and buffer delay			0.3		0.5		0.7	ns
t_{IO}	I/O input pad and buffer delay			0.3		0.5		0.7	ns
t_{FIN}	Fast input delay			0.9		1.3		2.0	ns
t_{FIND}	Programmable delay adder for fast input			1.0		1.5		1.5	ns
t_{SEXP}	Shared expander delay			1.5		2.1		3.2	ns
t_{PEXP}	Parallel expander delay			0.4		0.6		0.9	ns
t_{LAD}	Logic array delay			1.4		2.0		3.1	ns
t_{LAC}	Logic control array delay			1.2		1.7		2.6	ns
t_{IOE}	Internal output enable delay			0.1		0.2		0.3	ns
t_{OD1}	Output buffer and pad delay slow slew rate = off $V_{CCIO} = 3.3\text{ V}$	$C1 = 35\text{ pF}$		0.9		1.2		1.8	ns
t_{OD3}	Output buffer and pad delay slow slew rate = on $V_{CCIO} = 2.5\text{ V}$ or 3.3 V	$C1 = 35\text{ pF}$		5.9		6.2		6.8	ns
t_{ZX1}	Output buffer enable delay slow slew rate = off $V_{CCIO} = 3.3\text{ V}$	$C1 = 35\text{ pF}$		1.6		2.2		3.4	ns
t_{ZX3}	Output buffer enable delay slow slew rate = on $V_{CCIO} = 2.5\text{ V}$ or 3.3 V	$C1 = 35\text{ pF}$		6.6		7.2		8.4	ns
t_{XZ}	Output buffer disable delay	$C1 = 5\text{ pF}$		1.6		2.2		3.4	ns
t_{SU}	Register setup time		0.7		1.1		1.6		ns
t_H	Register hold time		0.4		0.5		0.9		ns
t_{FSU}	Register setup time of fast input		0.8		0.8		1.1		ns
t_{FH}	Register hold time of fast input		1.2		1.2		1.4		ns
t_{RD}	Register delay			0.5		0.6		0.9	ns
t_{COMB}	Combinatorial delay			0.2		0.3		0.5	ns
t_{IC}	Array clock delay			1.2		1.8		2.8	ns
t_{EN}	Register enable time			1.2		1.7		2.6	ns
t_{GLOB}	Global control delay			0.7		1.1		1.6	ns
t_{PRE}	Register preset time			1.0		1.3		1.9	ns
t_{CLR}	Register clear time			1.0		1.3		1.9	ns
t_{PIA}	PIA delay	(2)		0.7		1.0		1.4	ns
t_{LPA}	Low-power adder	(4)		1.5		2.1		3.2	ns

Table 20. EPM7032B Selectable I/O Standard Timing Adder Delays *Notes (1)*

I/O Standard	Parameter	Speed Grade						Unit
		-3.5		-5.0		-7.5		
		Min	Max	Min	Max	Min	Max	
PCI	Input to PIA		0.0		0.0		0.0	ns
	Input to global clock and clear		0.0		0.0		0.0	ns
	Input to fast input register		0.0		0.0		0.0	ns
	All outputs		0.0		0.0		0.0	ns

Notes to tables:

- (1) These values are specified under the Recommended Operating Conditions in [Table 15 on page 29](#). See [Figure 14](#) for more information on switching waveforms.
- (2) These values are specified for a PIA fan-out of all LABs.
- (3) Measured with a 16-bit loadable, enabled, up/down counter programmed into each LAB.
- (4) The t_{LPA} parameter must be added to the t_{LAD} , t_{LAC} , t_{IC} , t_{ACL} , t_{CPW} , t_{EN} , and t_{SEXP} parameters for macrocells running in low-power mode.

Table 21. EPM7064B External Timing Parameters *Note (1)*

Symbol	Parameter	Conditions	Speed Grade						Unit
			-3		-5		-7		
			Min	Max	Min	Max	Min	Max	
t _{PD1}	Input to non-registered output	C1 = 35 pF (2)		3.5		5.0		7.5	ns
t _{PD2}	I/O input to non-registered output	C1 = 35 pF (2)		3.5		5.0		7.5	ns
t _{SU}	Global clock setup time	(2)	2.1		3.0		4.5		ns
t _H	Global clock hold time	(2)	0.0		0.0		0.0		ns
t _{FSU}	Global clock setup time of fast input		1.0		1.0		1.5		ns
t _{FH}	Global clock hold time of fast input		1.0		1.0		1.0		ns
t _{FZHSU}	Global clock setup time of fast input with zero hold time		2.0		2.5		3.0		ns
t _{FZHH}	Global clock hold time of fast input with zero hold time		0.0		0.0		0.0		ns
t _{CO1}	Global clock to output delay	C1 = 35 pF	1.0	2.4	1.0	3.4	1.0	5.0	ns
t _{CH}	Global clock high time		1.5		2.0		3.0		ns
t _{CL}	Global clock low time		1.5		2.0		3.0		ns
t _{ASU}	Array clock setup time	(2)	0.9		1.3		1.9		ns
t _{AH}	Array clock hold time	(2)	0.2		0.3		0.6		ns
t _{ACO1}	Array clock to output delay	C1 = 35 pF (2)	1.0	3.6	1.0	5.1	1.0	7.6	ns
t _{ACH}	Array clock high time		1.5		2.0		3.0		ns
t _{ACL}	Array clock low time		1.5		2.0		3.0		ns
t _{CPPW}	Minimum pulse width for clear and preset		1.5		2.0		3.0		ns
t _{CNT}	Minimum global clock period	(2)		3.3		4.7		7.0	ns
f _{CNT}	Maximum internal global clock frequency	(2), (3)	303.0		212.8		142.9		MHz
t _{ACNT}	Minimum array clock period	(2)		3.3		4.7		7.0	ns
f _{ACNT}	Maximum internal array clock frequency	(2), (3)	303.0		212.8		142.9		MHz

Table 23. EPM7064B Selectable I/O Standard Timing Adder Delays (Part 1 of 2) *Note (1)*

I/O Standard	Parameter	Speed Grade						Unit
		-3		-5		-7		
		Min	Max	Min	Max	Min	Max	
3.3 V TTL/CMOS	Input to PIA		0.0		0.0		0.0	ns
	Input to global clock and clear		0.0		0.0		0.0	ns
	Input to fast input register		0.0		0.0		0.0	ns
	All outputs		0.0		0.0		0.0	ns
2.5 V TTL/CMOS	Input to PIA		0.3		0.4		0.6	ns
	Input to global clock and clear		0.3		0.4		0.6	ns
	Input to fast input register		0.2		0.3		0.4	ns
	All outputs		0.2		0.3		0.4	ns
1.8 V TTL/CMOS	Input to PIA		0.5		0.7		1.1	ns
	Input to global clock and clear		0.5		0.7		1.1	ns
	Input to fast input register		0.4		0.6		0.9	ns
	All outputs		1.2		1.7		2.6	ns
SSTL-2 Class I	Input to PIA		1.3		1.9		2.8	ns
	Input to global clock and clear		1.2		1.7		2.6	ns
	Input to fast input register		0.9		1.3		1.9	ns
	All outputs		0.0		0.0		0.0	ns
SSTL-2 Class II	Input to PIA		1.3		1.9		2.8	ns
	Input to global clock and clear		1.2		1.7		2.6	ns
	Input to fast input register		0.9		1.3		1.9	ns
	All outputs		−0.1		−0.1		−0.2	ns
SSTL-3 Class I	Input to PIA		1.2		1.7		2.6	ns
	Input to global clock and clear		0.9		1.3		1.9	ns
	Input to fast input register		0.8		1.1		1.7	ns
	All outputs		0.0		0.0		0.0	ns
SSTL-3 Class II	Input to PIA		1.2		1.7		2.6	ns
	Input to global clock and clear		0.9		1.3		1.9	ns
	Input to fast input register		0.8		1.1		1.7	ns
	All outputs		0.0		0.0		0.0	ns
GTL+	Input to PIA		1.6		2.3		3.4	ns
	Input to global clock and clear		1.6		2.3		3.4	ns
	Input to fast input register		1.5		2.1		3.2	ns
	All outputs		0.0		0.0		0.0	ns

Table 23. EPM7064B Selectable I/O Standard Timing Adder Delays (Part 2 of 2) *Note (1)*

I/O Standard	Parameter	Speed Grade						Unit
		-3		-5		-7		
		Min	Max	Min	Max	Min	Max	
PCI	Input to PIA		0.0		0.0		0.0	ns
	Input to global clock and clear		0.0		0.0		0.0	ns
	Input to fast input register		0.0		0.0		0.0	ns
	All outputs		0.0		0.0		0.0	ns

Notes to tables:

- (1) These values are specified under the Recommended Operating Conditions in [Table 15 on page 29](#). See [Figure 14](#) for more information on switching waveforms.
- (2) These values are specified for a PIA fan-out of all LABs.
- (3) Measured with a 16-bit loadable, enabled, up/down counter programmed into each LAB.
- (4) The t_{LPA} parameter must be added to the t_{LAD} , t_{LAC} , t_{IC} , t_{ACL} , t_{CPPW} , t_{EN} , and t_{SEXP} parameters for macrocells running in low-power mode.

Table 27. EPM7256B External Timing Parameters *Note (1)*

Symbol	Parameter	Conditions	Speed Grade						Unit
			-5		-7		-10		
			Min	Max	Min	Max	Min	Max	
t _{PD1}	Input to non-registered output	C1 = 35 pF (2)		5.0		7.5		10.0	ns
t _{PD2}	I/O input to non-registered output	C1 = 35 pF (2)		5.0		7.5		10.0	ns
t _{SU}	Global clock setup time	(2)	3.3		4.8		6.6		ns
t _H	Global clock hold time	(2)	0.0		0.0		0.0		ns
t _{FSU}	Global clock setup time of fast input		1.0		1.5		1.5		ns
t _{FH}	Global clock hold time for fast input		1.0		1.0		1.0		ns
t _{FZHSU}	Global clock setup time of fast input with zero hold time		2.5		3.0		3.0		ns
t _{FZHH}	Global clock hold time of fast input with zero hold time		0.0		0.0		0.0		ns
t _{CO1}	Global clock to output delay	C1 = 35 pF	1.0	3.3	1.0	5.1	1.0	6.7	ns
t _{CH}	Global clock high time		2.0		3.0		4.0		ns
t _{CL}	Global clock low time		2.0		3.0		4.0		ns
t _{ASU}	Array clock setup time	(2)	1.4		2.0		2.8		ns
t _{AH}	Array clock hold time	(2)	0.4		0.8		1.0		ns
t _{ACO1}	Array clock to output delay	C1 = 35 pF (2)	1.0	5.2	1.0	7.9	1.0	10.5	ns
t _{ACH}	Array clock high time		2.0		3.0		4.0		ns
t _{ACL}	Array clock low time		2.0		3.0		4.0		ns
t _{CPPW}	Minimum pulse width for clear and preset		2.0		3.0		4.0		ns
t _{CNT}	Minimum global clock period	(2)		5.3		7.9		10.6	ns
f _{CNT}	Maximum internal global clock frequency	(2), (3)	188.7		126.6		94.3		MHz
t _{ACNT}	Minimum array clock period	(2)		5.3		7.9		10.6	ns
f _{ACNT}	Maximum internal array clock frequency	(2), (3)	188.7		126.6		94.3		MHz

Table 28. EPM7256B Internal Timing Parameters *Note (1)*

Symbol	Parameter	Conditions	Speed Grade						Unit
			-5		-7		-10		
			Min	Max	Min	Max	Min	Max	
t_{IN}	Input pad and buffer delay			0.4		0.6		0.8	ns
t_{IO}	I/O input pad and buffer delay			0.4		0.6		0.8	ns
t_{FIN}	Fast input delay			1.5		2.5		3.1	ns
t_{FIND}	Programmable delay adder for fast input			1.5		1.5		1.5	ns
t_{SEXP}	Shared expander delay			1.5		2.3		3.0	ns
t_{PEXP}	Parallel expander delay			0.4		0.6		0.8	ns
t_{LAD}	Logic array delay			1.7		2.5		3.3	ns
t_{LAC}	Logic control array delay			1.5		2.2		2.9	ns
t_{IOE}	Internal output enable delay			0.1		0.2		0.3	ns
t_{OD1}	Output buffer and pad delay slow slew rate = off $V_{CCIO} = 3.3\text{ V}$	$C1 = 35\text{ pF}$		0.9		1.4		1.9	ns
t_{OD3}	Output buffer and pad delay slow slew rate = on $V_{CCIO} = 2.5\text{ V}$ or 3.3 V	$C1 = 35\text{ pF}$		5.9		6.4		6.9	ns
t_{ZX1}	Output buffer enable delay slow slew rate = off $V_{CCIO} = 3.3\text{ V}$	$C1 = 35\text{ pF}$		2.2		3.3		4.5	ns
t_{ZX3}	Output buffer enable delay slow slew rate = on $V_{CCIO} = 2.5\text{ V}$ or 3.3 V	$C1 = 35\text{ pF}$		7.2		8.3		9.5	ns
t_{XZ}	Output buffer disable delay	$C1 = 5\text{ pF}$		2.2		3.3		4.5	ns
t_{SU}	Register setup time		1.2		1.8		2.5		ns
t_H	Register hold time		0.6		1.0		1.3		ns
t_{FSU}	Register setup time of fast input		0.8		1.1		1.1		ns
t_{FH}	Register hold time of fast input		1.2		1.4		1.4		ns
t_{RD}	Register delay			0.7		1.0		1.3	ns
t_{COMB}	Combinatorial delay			0.3		0.4		0.5	ns
t_{IC}	Array clock delay			1.5		2.3		3.0	ns
t_{EN}	Register enable time			1.5		2.2		2.9	ns
t_{GLOB}	Global control delay			1.3		2.1		2.7	ns
t_{PRE}	Register preset time			1.0		1.6		2.1	ns
t_{CLR}	Register clear time			1.0		1.6		2.1	ns
t_{PIA}	PIA delay	(2)		1.7		2.6		3.3	ns
t_{LPA}	Low-power adder	(4)		2.0		3.0		4.0	ns

Table 29. EPM7256B Selectable I/O Standard Timing Adder Delays (Part 2 of 2) *Note (1)*

I/O Standard	Parameter	Speed Grade						Unit
		-5		-7		-10		
		Min	Max	Min	Max	Min	Max	
PCI	Input to PIA		0.0		0.0		0.0	ns
	Input to global clock and clear		0.0		0.0		0.0	ns
	Input to fast input register		0.0		0.0		0.0	ns
	All outputs		0.0		0.0		0.0	ns

Notes to tables:

- (1) These values are specified under the Recommended Operating Conditions in Table 15 on page 29. See Figure 14 for more information on switching waveforms.
- (2) These values are specified for a PIA fan-out of one LAB (16 macrocells). For each additional LAB fan-out in these devices, add an additional 0.1 ns to the PIA timing value.
- (3) Measured with a 16-bit loadable, enabled, up/down counter programmed into each LAB.
- (4) The t_{LPA} parameter must be added to the t_{LAD} , t_{LAC} , t_{IC} , t_{ACL} , t_{CPW} , t_{EN} , and t_{SEXP} parameters for macrocells running in low-power mode.

Table 32. EPM7512B Selectable I/O Standard Timing Adder Delays (Part 2 of 2) *Note (1)*

I/O Standard	Parameter	Speed Grade						Unit
		-5		-7		-10		
		Min	Max	Min	Max	Min	Max	
PCI	Input to PIA		0.0		0.0		0.0	ns
	Input to global clock and clear		0.0		0.0		0.0	ns
	Input to fast input register		0.0		0.0		0.0	ns
	All outputs		0.0		0.0		0.0	ns

Notes to tables:

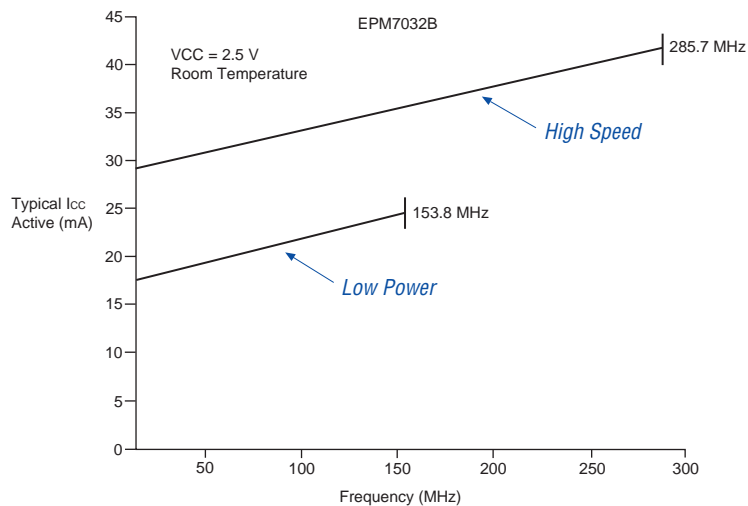
- (1) These values are specified under the Recommended Operating Conditions in Table 15 on page 29. See Figure 14 for more information on switching waveforms.
- (2) These values are specified for a PIA fan-out of one LAB (16 macrocells). For each additional LAB fan-out in these devices, add an additional 0.12 ns to the PIA timing value.
- (3) Measured with a 16-bit loadable, enabled, up/down counter programmed into each LAB.
- (4) The t_{LPA} parameter must be added to the t_{LAD} , t_{LAC} , t_{IC} , t_{ACL} , t_{CPPW} , t_{EN} , and t_{SEXP} parameters for macrocells running in low-power mode.

Power Consumption

Supply power (P) versus frequency (f_{MAX} , in MHz) for MAX 7000B devices is calculated with the following equation:

$$P = P_{INT} + P_{IO} = I_{CCINT} \times V_{CC} + P_{IO}$$

The P_{IO} value, which depends on the device output load characteristics and switching frequency, can be calculated using the guidelines given in Application Note 74 (*Evaluating Power for Altera Devices*).

Figure 15. I_{CC} vs. Frequency for EPM7032B Devices**Figure 16. I_{CC} vs. Frequency for EPM7064B Devices**