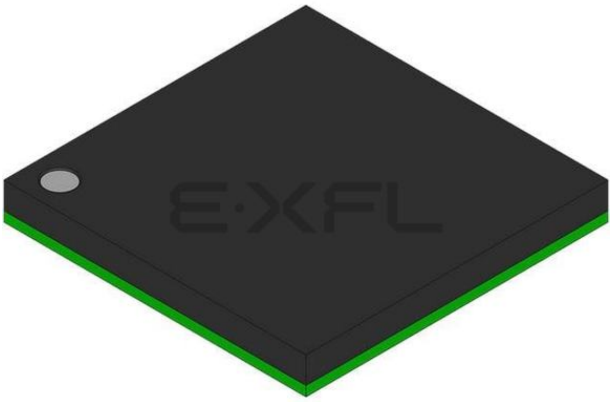

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Understanding Embedded - CPLDs (Complex Programmable Logic Devices)

Embedded - CPLDs, or Complex Programmable Logic Devices, are highly versatile digital logic devices used in electronic systems. These programmable components are designed to perform complex logical operations and can be customized for specific applications. Unlike fixed-function ICs, CPLDs offer the flexibility to reprogram their configuration, making them an ideal choice for various embedded systems. They consist of a set of logic gates and programmable interconnects, allowing designers to implement complex logic circuits without needing custom hardware.

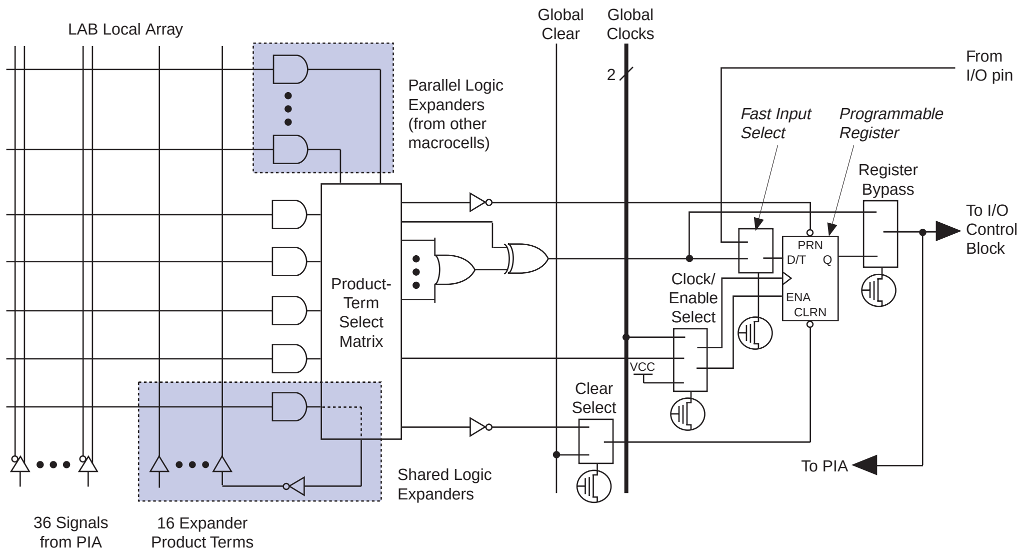
Applications of Embedded - CPLDs

Details	
Product Status	Active
Programmable Type	In System Programmable
Delay Time tpd(1) Max	3.5 ns
Voltage Supply - Internal	2.375V ~ 2.625V
Number of Logic Elements/Blocks	4
Number of Macrocells	64
Number of Gates	1250
Number of I/O	68
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LBGA
Supplier Device Package	100-FBGA (11x11)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=epm7064bfc100-3n

Macrocells

The MAX 7000B macrocell can be individually configured for either sequential or combinatorial logic operation. The macrocell consists of three functional blocks: the logic array, the product-term select matrix, and the programmable register. Figure 2 shows the MAX 7000B macrocell.

Figure 2. MAX 7000B Macrocell



Combinatorial logic is implemented in the logic array, which provides five product terms per macrocell. The product-term select matrix allocates these product terms for use as either primary logic inputs (to the OR and XOR gates) to implement combinatorial functions, or as secondary inputs to the macrocell's register preset, clock, and clock enable control functions.

Two kinds of expander product terms ("expanders") are available to supplement macrocell logic resources:

- Shareable expanders, which are inverted product terms that are fed back into the logic array
- Parallel expanders, which are product terms borrowed from adjacent macrocells

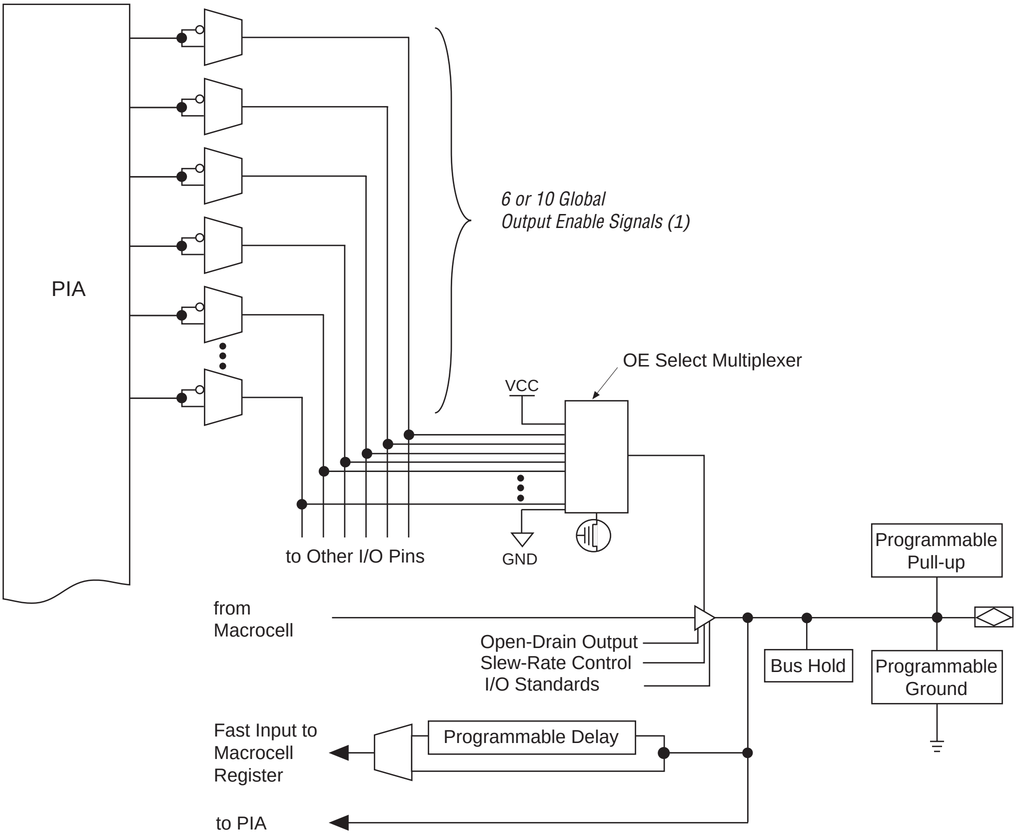
Parallel Expanders

Parallel expanders are unused product terms that can be allocated to a neighboring macrocell to implement fast, complex logic functions. Parallel expanders allow up to 20 product terms to directly feed the macrocell OR logic, with five product terms provided by the macrocell and 15 parallel expanders provided by neighboring macrocells in the LAB.

The Altera Compiler can automatically allocate up to three sets of up to five parallel expanders to the macrocells that require additional product terms. Each set of five parallel expanders incurs a small, incremental timing delay (t_{PEXP}). For example, if a macrocell requires 14 product terms, the Compiler uses the five dedicated product terms within the macrocell and allocates two sets of parallel expanders; the first set includes five product terms and the second set includes four product terms, increasing the total delay by $2 \times t_{PEXP}$.

Two groups of eight macrocells within each LAB (e.g., macrocells 1 through 8, and 9 through 16) form two chains to lend or borrow parallel expanders. A macrocell borrows parallel expanders from lower-numbered macrocells. For example, macrocell 8 can borrow parallel expanders from macrocell 7, from macrocells 7 and 6, or from macrocells 7, 6, and 5. Within each group of eight, the lowest-numbered macrocell can only lend parallel expanders and the highest-numbered macrocell can only borrow them. Figure 4 shows how parallel expanders can be borrowed from a neighboring macrocell.

Figure 6. I/O Control Block of MAX 7000B Devices



Note:

(1) EPM7032B, EPM7064B, EPM7128B, and EPM7256B devices have six output enable signals. EPM7512B devices have ten output enable signals.

When the tri-state buffer control is connected to ground, the output is tri-stated (high impedance) and the I/O pin can be used as a dedicated input. When the tri-state buffer control is connected to V_{CC}, the output is enabled.

The MAX 7000B architecture provides dual I/O feedback, in which macrocell and pin feedbacks are independent. When an I/O pin is configured as an input, the associated macrocell can be used for buried logic.

In-System Programmability (ISP)

MAX 7000B devices can be programmed in-system via an industry-standard 4-pin IEEE Std. 1149.1 (JTAG) interface. ISP offers quick, efficient iterations during design development and debugging cycles. The MAX 7000B architecture internally generates the high programming voltages required to program EEPROM cells, allowing in-system programming with only a single 2.5-V power supply. During in-system programming, the I/O pins are tri-stated and weakly pulled-up to eliminate board conflicts. The pull-up value is nominally 50 k¾.

MAX 7000B devices have an enhanced ISP algorithm for faster programming. These devices also offer an ISP_Done bit that provides safe operation when in-system programming is interrupted. This ISP_Done bit, which is the last bit programmed, prevents all I/O pins from driving until the bit is programmed.

ISP simplifies the manufacturing flow by allowing devices to be mounted on a PCB with standard pick-and-place equipment before they are programmed. MAX 7000B devices can be programmed by downloading the information via in-circuit testers, embedded processors, the Altera MasterBlaster communications cable, and the ByteBlasterMV parallel port download cable. Programming the devices after they are placed on the board eliminates lead damage on high-pin-count packages (e.g., QFP packages) due to device handling. MAX 7000B devices can be reprogrammed after a system has already shipped to the field. For example, product upgrades can be performed in the field via software or modem.

In-system programming can be accomplished with either an adaptive or constant algorithm. An adaptive algorithm reads information from the unit and adapts subsequent programming steps to achieve the fastest possible programming time for that unit. A constant algorithm uses a pre-defined (non-adaptive) programming sequence that does not take advantage of adaptive algorithm programming time improvements. Some in-circuit testers cannot program using an adaptive algorithm. Therefore, a constant algorithm must be used. MAX 7000B devices can be programmed with either an adaptive or constant (non-adaptive) algorithm.

The Jam Standard Test and Programming Language (STAPL), JEDEC standard JESD-71, can be used to program MAX 7000B devices with in-circuit testers, PCs, or embedded processors.

For more information on using the Jam language, see *Application Note 88 (Using the Jam Language for ISP & ICR via an Embedded Processor)* and *Application Note 122 (Using STAPL for ISP & ICR via an Embedded Processor)*.

The ISP circuitry in MAX 7000B devices is compliant with the IEEE Std. 1532 specification. The IEEE Std. 1532 is a standard developed to allow concurrent ISP between multiple PLD vendors.

The programming times described in Tables 4 through 6 are associated with the worst-case method using the enhanced ISP algorithm.

Table 4. MAX 7000B t_{PULSE} & $Cycle_{TCK}$ Values

Device	Programming		Stand-Alone Verification	
	t_{PPULSE} (s)	$Cycle_{PTCK}$	t_{VPULSE} (s)	$Cycle_{VTCK}$
EMP7032B	2.12	70,000	0.002	18,000
EMP7064B	2.12	120,000	0.002	35,000
EMP7128B	2.12	222,000	0.002	69,000
EMP7256B	2.12	466,000	0.002	151,000
EMP7512B	2.12	914,000	0.002	300,000

Tables 5 and 6 show the in-system programming and stand alone verification times for several common test clock frequencies.

Table 5. MAX 7000B In-System Programming Times for Different Test Clock Frequencies

Device	f_{TCK}								Units
	10 MHz	5 MHz	2 MHz	1 MHz	500 kHz	200 kHz	100 kHz	50 kHz	
EMP7032B	2.13	2.13	2.15	2.19	2.26	2.47	2.82	3.52	s
EMP7064B	2.13	2.14	2.18	2.24	2.36	2.72	3.32	4.52	s
EMP7128B	2.14	2.16	2.23	2.34	2.56	3.23	4.34	6.56	s
EMP7256B	2.17	2.21	2.35	2.58	3.05	4.45	6.78	11.44	s
EMP7512B	2.21	2.30	2.58	3.03	3.95	6.69	11.26	20.40	s

Table 1. MAX 7000B Stand-Alone Verification Times for Different Test Clock Frequencies

Device	f_{TCK}								Units
	10 MHz	5 MHz	2 MHz	1 MHz	500 kHz	200 kHz	100 kHz	50 kHz	
EMP7032B	0.00	0.01	0.01	0.02	0.04	0.09	0.18	0.36	s
EMP7064B	0.01	0.01	0.02	0.04	0.07	0.18	0.35	0.70	s
EMP7128B	0.01	0.02	0.04	0.07	0.14	0.35	0.69	1.38	s
EMP7256B	0.02	0.03	0.08	0.15	0.30	0.76	1.51	3.02	s
EMP7512B	0.03	0.06	0.15	0.30	0.60	1.50	3.00	6.00	s

Figure 8. MAX 7000B JTAG Waveforms

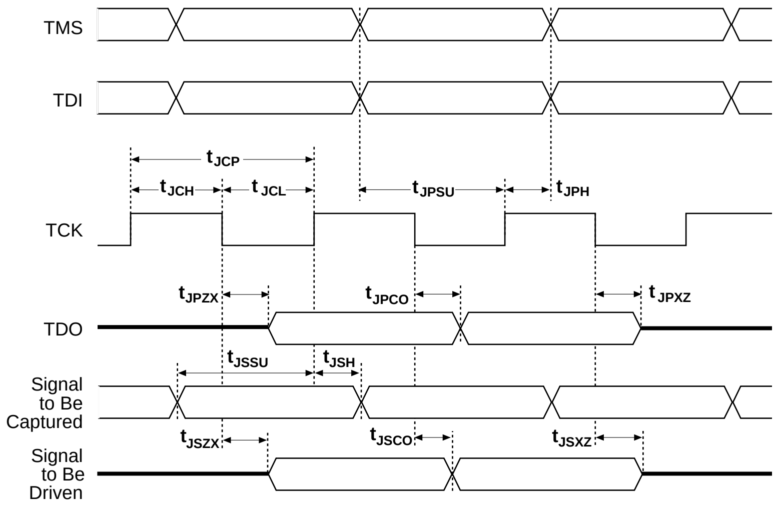


Table 9 shows the JTAG timing parameters and values for MAX 7000B devices.

Table 9. JTAG Timing Parameters & Values for MAX 7000B Devices *Note (1)*

Symbol	Parameter	Min	Max	Unit
t_{JCP}	TCK clock period	100		ns
t_{JCH}	TCK clock high time	50		ns
t_{JCL}	TCK clock low time	50		ns
t_{JPSU}	JTAG port setup time	20		ns
t_{JPH}	JTAG port hold time	45		ns
t_{JPCO}	JTAG port clock to output		25	ns
t_{JPZX}	JTAG port high impedance to valid output		25	ns
t_{JPXZ}	JTAG port valid output to high impedance		25	ns
t_{JSSU}	Capture register setup time	20		ns
t_{JSH}	Capture register hold time	45		ns
t_{JSCO}	Update register clock to output		25	ns
t_{JSZX}	Update register high impedance to valid output		25	ns
t_{JSXZ}	Update register valid output to high impedance		25	ns

Note:

(1) Timing parameters in this table apply to all V_{CCIO} levels.

Table 10. MAX 7000B MultiVolt I/O Support

V_{CCIO} (V)	Input Signal (V)				Output Signal (V)			
	1.8	2.5	3.3	5.0	1.8	2.5	3.3	5.0
1.8	✓	✓	✓		✓			
2.5	✓	✓	✓			✓		
3.3	✓	✓	✓				✓	✓

Open-Drain Output Option

MAX 7000B devices provide an optional open-drain (equivalent to open-collector) output for each I/O pin. This open-drain output enables the device to provide system-level control signals (e.g., interrupt and write enable signals) that can be asserted by any of several devices. It can also provide an additional wired-OR plane.

Programmable Ground Pins

Each unused I/O pin on MAX 7000B devices may be used as an additional ground pin. This programmable ground feature does not require the use of the associated macrocell; therefore, the buried macrocell is still available for user logic.

Slew-Rate Control

The output buffer for each MAX 7000B I/O pin has an adjustable output slew rate that can be configured for low-noise or high-speed performance. A faster slew rate provides high-speed transitions for high-performance systems. However, these fast transitions may introduce noise transients into the system. A slow slew rate reduces system noise, but adds a nominal delay of 4 to 5 ns. When the configuration cell is turned off, the slew rate is set for low-noise performance. Each I/O pin has an individual EEPROM bit that controls the slew rate, allowing designers to specify the slew rate on a pin-by-pin basis. The slew rate control affects both the rising and falling edges of the output signal.

Advanced I/O Standard Support

The MAX 7000B I/O pins support the following I/O standards: LVTTL, LVCMOS, 1.8-V I/O, 2.5-V I/O, GTL+, SSTL-3 Class I and II, and SSTL-2 Class I and II.

Programmable Pull-Up Resistor

Each MAX 7000B device I/O pin provides an optional programmable pull-up resistor during user mode. When this feature is enabled for an I/O pin, the pull-up resistor (typically 50 k¾) weakly holds the output to V_{CCIO} level.

Bus Hold

Each MAX 7000B device I/O pin provides an optional bus-hold feature. When this feature is enabled for an I/O pin, the bus-hold circuitry weakly holds the signal at its last driven state. By holding the last driven state of the pin until the next input signals is present, the bus-hold feature can eliminate the need to add external pull-up or pull-down resistors to hold a signal level when the bus is tri-stated. The bus-hold circuitry also pulls undriven pins away from the input threshold voltage where noise can cause unintended high-frequency switching. This feature can be selected individually for each I/O pin. The bus-hold output will drive no higher than V_{CCIO} to prevent overdriving signals. The propagation delays through the input and output buffers in MAX 7000B devices are not affected by whether the bus-hold feature is enabled or disabled.

The bus-hold circuitry weakly pulls the signal level to the last driven state through a resistor with a nominal resistance (R_{BH}) of approximately 8.5 k¾. Table 12 gives specific sustaining current that will be driven through this resistor and overdrive current that will identify the next driven input level. This information is provided for each VCCIO voltage level.

Table 12. Bus Hold Parameters

Parameter	Conditions	VCCIO Level						Units
		1.8 V		2.5 V		3.3 V		
		Min	Max	Min	Max	Min	Max	
Low sustaining current	$V_{IN} > V_{IL}$ (max)	30		50		70		µA
High sustaining current	$V_{IN} < V_{IH}$ (min)	–30		–50		–70		µA
Low overdrive current	$0 V < V_{IN} < V_{CCIO}$		200		300		500	µA
High overdrive current	$0 V < V_{IN} < V_{CCIO}$		–295		–435		–680	µA

The bus-hold circuitry is active only during user operation. At power-up, the bus-hold circuit initializes its initial hold value as V_{CC} approaches the recommended operation conditions. When transitioning from ISP to User Mode with bus hold enabled, the bus-hold circuit captures the value present on the pin at the end of programming.

Power Sequencing & Hot-Socketing

Because MAX 7000B devices can be used in a mixed-voltage environment, they have been designed specifically to tolerate any possible power-up sequence. The V_{CCIO} and V_{CCINT} power planes can be powered in any order.

Signals can be driven into MAX 7000B devices before and during power-up (and power-down) without damaging the device. Additionally, MAX 7000B devices do not drive out during power-up. Once operating conditions are reached, MAX 7000B devices operate as specified by the user.

MAX 7000B device I/O pins will not source or sink more than 300 µA of DC current during power-up. All pins can be driven up to 4.1 V during hot-socketing.

Design Security

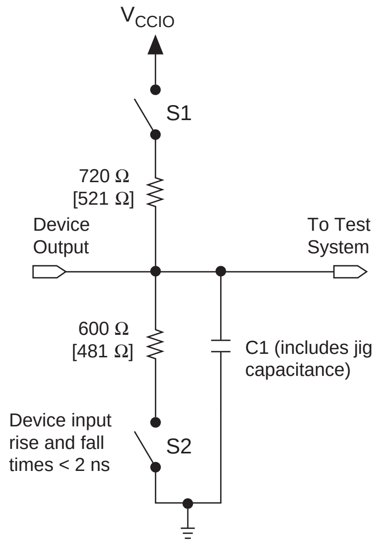
All MAX 7000B devices contain a programmable security bit that controls access to the data programmed into the device. When this bit is programmed, a design implemented in the device cannot be copied or retrieved. This feature provides a high level of design security, because programmed data within EEPROM cells is invisible. The security bit that controls this function, as well as all other programmed data, is reset only when the device is reprogrammed.

Generic Testing

MAX 7000B devices are fully functionally tested. Complete testing of each programmable EEPROM bit and all internal logic elements ensures 100% programming yield. AC test measurements are taken under conditions equivalent to those shown in Figure 11. Test patterns can be used and then erased during early stages of the production flow.

Figure 11. MAX 7000B AC Test Conditions

Power supply transients can affect AC measurements. Simultaneous transitions of multiple outputs should be avoided for accurate measurement. Threshold tests must not be performed under AC conditions. Large-amplitude, fast-ground-current transients normally occur as the device outputs discharge the load capacitances. When these transients flow through the parasitic inductance between the device ground pin and the test system ground, significant reductions in observable noise immunity can result. Numbers in brackets are for 2.5-V outputs. Numbers without brackets are for 3.3-V outputs. Switches S1 and S2 are open for all tests except output disable timing parameters.



Operating Conditions

Tables 14 through 17 provide information on absolute maximum ratings, recommended operating conditions, operating conditions, and capacitance for MAX 7000B devices.

Table 14. MAX 7000B Device Absolute Maximum Ratings *Note (1)*

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CCINT}	Supply voltage		–0.5	3.6	V
V_{CCIO}	Supply voltage		–0.5	3.6	V
V_I	DC input voltage	*(2)*	–2.0	4.6	V
I_{OUT}	DC output current, per pin		–33	50	mA
T_{STG}	Storage temperature	No bias	–65	150	° C
T_A	Ambient temperature	Under bias	–65	135	° C
T_J	Junction temperature	Under bias	–65	135	° C

Table 17. MAX 7000B Device Capacitance *Note (9)*					
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Unit**
C_{IN}	Input pin capacitance	V_{IN} = 0 V, f = 1.0 MHz		8	pF
$C_{I/O}$	I/O pin capacitance	V_{OUT} = 0 V, f = 1.0 MHz		8	pF

Notes to tables:

(1) See the *Operating Requirements for Altera Devices Data Sheet*.

(2) Minimum DC input voltage is –0.5 V. During transitions, the inputs may undershoot to –2.0 V or overshoot to 4.6 V for input currents less than 100 mA and periods shorter than 20 ns.

(3) All pins, including dedicated inputs, I/O pins, and JTAG pins, may be driven before V_{CCINT} and V_{CCIO} are powered.

(4) These values are specified under the Recommended Operating Conditions in Table 15 on page 29.

(5) The parameter is measured with 50% of the outputs each sourcing the specified current. The I_{OH} parameter refers to high-level TTL or CMOS output current.

(6) The parameter is measured with 50% of the outputs each sinking the specified current. The I_{OL} parameter refers to low-level TTL or CMOS output current.

(7) This value is specified for normal device operation. During power-up, the maximum leakage current is ±300 µA.

(8) This pull-up exists while devices are being programmed in-system and in unprogrammed devices during power-up. The pull-up resistor is from the pins to V_{CCIO}.

(9) Capacitance is measured at 25° C and is sample-tested only. Two of the dedicated input pins (`OE1` and `GCLRN`) have a maximum capacitance of 15 pF.

(10) The POR time for all 7000B devices does not exceed 100 µs. The sufficient V_{CCINT} voltage level for POR is 2.375 V. The device is fully initialized within the POR time after V_{CCINT} reaches the sufficient POR voltage level.

(11) These devices support in-system programming for –40° to 100° C. For in-system programming support between –40° and 0° C, contact Altera Applications.

Table 25. EPM7128B Internal Timing Parameters *Note (1)*									
Symbol	**Parameter**	**Conditions**	**Speed Grade**						**Unit**
			-4		**-7**		**-10**		
			Min	**Max**	**Min**	**Max**	**Min**	**Max**	
t_{IN}	Input pad and buffer delay			0.3		0.6		0.8	ns
t_{IO}	I/O input pad and buffer delay			0.3		0.6		0.8	ns
t_{FIN}	Fast input delay			1.3		2.9		3.7	ns
t_{FIND}	Programmable delay adder for fast input			1.0		1.5		1.5	ns
t_{SEXP}	Shared expander delay			1.5		2.8		3.8	ns
t_{PEXP}	Parallel expander delay			0.4		0.8		1.0	ns
t_{LAD}	Logic array delay			1.6		2.9		3.8	ns
t_{LAC}	Logic control array delay			1.4		2.6		3.4	ns
t_{IOE}	Internal output enable delay			0.1		0.3		0.4	ns
t_{OD1}	Output buffer and pad delay slow slew rate = off V_{CCIO} = 3.3 V	C1 = 35 pF		0.9		1.7		2.2	ns
t_{OD3}	Output buffer and pad delay slow slew rate = on V_{CCIO} = 2.5 V or 3.3 V	C1 = 35 pF		5.9		6.7		7.2	ns
t_{ZX1}	Output buffer enable delay slow slew rate = off V_{CCIO} = 3.3 V	C1 = 35 pF		1.8		3.3		4.4	ns
t_{ZX3}	Output buffer enable delay slow slew rate = on V_{CCIO} = 2.5 V or 3.3 V	C1 = 35 pF		6.8		8.3		9.4	ns
t_{XZ}	Output buffer disable delay	C1 = 5 pF		1.8		3.3		4.4	ns
t_{SU}	Register setup time		1.0		1.9		2.6		ns
t_{H}	Register hold time		0.4		0.8		1.1		ns
t_{FSU}	Register setup time of fast input		0.8		0.9		0.9		ns
t_{FH}	Register hold time of fast input		1.2		1.6		1.6		ns
t_{RD}	Register delay			0.5		1.1		1.4	ns
t_{COMB}	Combinatorial delay			0.2		0.3		0.4	ns
t_{IC}	Array clock delay			1.4		2.8		3.6	ns
t_{EN}	Register enable time			1.4		2.6		3.4	ns
t_{GLOB}	Global control delay			1.1		2.3		3.1	ns
t_{PRE}	Register preset time			1.0		1.9		2.6	ns
t_{CLR}	Register clear time			1.0		1.9		2.6	ns
t_{PIA}	PIA delay	*(2)*		1.0		2.0		2.8	ns
t_{LPA}	Low-power adder	*(4)*		1.5		2.8		3.8	ns

Table 27. EPM7256B External Timing Parameters *Note (1)*

Symbol	Parameter	Conditions	Speed Grade						Unit
			-5		-7		-10		
			Min	Max	Min	Max	Min	Max	
t_{PD1}	Input to non-registered output	C1 = 35 pF *(2)*		5.0		7.5		10.0	ns
t_{PD2}	I/O input to non-registered output	C1 = 35 pF *(2)*		5.0		7.5		10.0	ns
t_{SU}	Global clock setup time	*(2)*	3.3		4.8		6.6		ns
t_{H}	Global clock hold time	*(2)*	0.0		0.0		0.0		ns
t_{FSU}	Global clock setup time of fast input		1.0		1.5		1.5		ns
t_{FH}	Global clock hold time for fast input		1.0		1.0		1.0		ns
t_{FZHSU}	Global clock setup time of fast input with zero hold time		2.5		3.0		3.0		ns
t_{FZHH}	Global clock hold time of fast input with zero hold time		0.0		0.0		0.0		ns
t_{CO1}	Global clock to output delay	C1 = 35 pF	1.0	3.3	1.0	5.1	1.0	6.7	ns
t_{CH}	Global clock high time		2.0		3.0		4.0		ns
t_{CL}	Global clock low time		2.0		3.0		4.0		ns
t_{ASU}	Array clock setup time	*(2)*	1.4		2.0		2.8		ns
t_{AH}	Array clock hold time	*(2)*	0.4		0.8		1.0		ns
t_{ACO1}	Array clock to output delay	C1 = 35 pF *(2)*	1.0	5.2	1.0	7.9	1.0	10.5	ns
t_{ACH}	Array clock high time		2.0		3.0		4.0		ns
t_{ACL}	Array clock low time		2.0		3.0		4.0		ns
t_{CPPW}	Minimum pulse width for clear and preset		2.0		3.0		4.0		ns
t_{CNT}	Minimum global clock period	*(2)*		5.3		7.9		10.6	ns
f_{CNT}	Maximum internal global clock frequency	*(2)*, *(3)*	188.7		126.6		94.3		MHz
t_{ACNT}	Minimum array clock period	*(2)*		5.3		7.9		10.6	ns
f_{ACNT}	Maximum internal array clock frequency	*(2)*, *(3)*	188.7		126.6		94.3		MHz

Table 29. EPM7256B Selectable I/O Standard Timing Adder Delays (Part 1 of 2) Note (1)

I/O Standard	Parameter	Speed Grade						Unit
		-5		-7		-10		
		Min	Max	Min	Max	Min	Max	
3.3 V TTL/CMOS	Input to PIA		0.0		0.0		0.0	ns
	Input to global clock and clear		0.0		0.0		0.0	ns
	Input to fast input register		0.0		0.0		0.0	ns
	All outputs		0.0		0.0		0.0	ns
2.5 V TTL/CMOS	Input to PIA		0.4		0.6		0.8	ns
	Input to global clock and clear		0.3		0.5		0.6	ns
	Input to fast input register		0.2		0.3		0.4	ns
	All outputs		0.2		0.3		0.4	ns
1.8 V TTL/CMOS	Input to PIA		0.6		0.9		1.2	ns
	Input to global clock and clear		0.6		0.9		1.2	ns
	Input to fast input register		0.5		0.8		1.0	ns
	All outputs		1.3		2.0		2.6	ns
SSTL-2 Class I	Input to PIA		1.5		2.3		3.0	ns
	Input to global clock and clear		1.3		2.0		2.6	ns
	Input to fast input register		1.1		1.7		2.2	ns
	All outputs		0.0		0.0		0.0	ns
SSTL-2 Class II	Input to PIA		1.5		2.3		3.0	ns
	Input to global clock and clear		1.3		2.0		2.6	ns
	Input to fast input register		1.1		1.7		2.2	ns
	All outputs		–0.1		–0.2		–0.2	ns
SSTL-3 Class I	Input to PIA		1.4		2.1		2.8	ns
	Input to global clock and clear		1.1		1.7		2.2	ns
	Input to fast input register		1.0		1.5		2.0	ns
	All outputs		0.0		0.0		0.0	ns
SSTL-3 Class II	Input to PIA		1.4		2.1		2.8	ns
	Input to global clock and clear		1.1		1.7		2.2	ns
	Input to fast input register		1.0		1.5		2.0	ns
	All outputs		0.0		0.0		0.0	ns
GTL+	Input to PIA		1.8		2.7		3.6	ns
	Input to global clock and clear		1.8		2.7		3.6	ns
	Input to fast input register		1.7		2.6		3.4	ns
	All outputs		0.0		0.0		0.0	ns

Table 29. EPM7256B Selectable I/O Standard Timing Adder Delays (Part 2 of 2) Note (1)								
I/O Standard	Parameter	Speed Grade						Unit
		-5		-7		-10		
		Min	Max	Min	Max	Min	Max	
PCI	Input to PIA		0.0		0.0		0.0	ns
	Input to global clock and clear		0.0		0.0		0.0	ns
	Input to fast input register		0.0		0.0		0.0	ns
	All outputs		0.0		0.0		0.0	ns

Notes to tables:

(1) These values are specified under the Recommended Operating Conditions in Table 15 on page 29. See Figure 14 for more information on switching waveforms.

(2) These values are specified for a PIA fan-out of one LAB (16 macrocells). For each additional LAB fan-out in these devices, add an additional 0.1 ns to the PIA timing value.

(3) Measured with a 16-bit loadable, enabled, up/down counter programmed into each LAB.

(4) The t_{LPA} parameter must be added to the t_{LAD}, t_{LAC}, t_{IC}, t_{ACL}, t_{CPPW}, t_{EN}, and t_{SEXP} parameters for macrocells running in low-power mode.

Table 32. EPM7512B Selectable I/O Standard Timing Adder Delays (Part 2 of 2) Note (1)

I/O Standard	Parameter	Speed Grade						Unit
		-5		-7		-10		
		Min	Max	Min	Max	Min	Max	
PCI	Input to PIA		0.0		0.0		0.0	ns
	Input to global clock and clear		0.0		0.0		0.0	ns
	Input to fast input register		0.0		0.0		0.0	ns
	All outputs		0.0		0.0		0.0	ns

Notes to tables:

(1) These values are specified under the Recommended Operating Conditions in Table 15 on page 29. See Figure 14 for more information on switching waveforms.
(2) These values are specified for a PIA fan-out of one LAB (16 macrocells). For each additional LAB fan-out in these devices, add an additional 0.12 ns to the PIA timing value.
(3) Measured with a 16-bit loadable, enabled, up/down counter programmed into each LAB.
(4) The t_{LPA} parameter must be added to the t_{LAD}, t_{LAC}, t_{IC}, t_{ACL}, t_{CPPW}, t_{EN}, and t_{SEXP} parameters for macrocells running in low-power mode.

Power Consumption

Supply power (P) versus frequency ($\mathbf{f_{MAX}}$, in MHz) for MAX 7000B devices is calculated with the following equation:

$$P = P_{INT} + P_{IO} = I_{CCINT} \times V_{CC} + P_{IO}$$

The P_{IO} value, which depends on the device output load characteristics and switching frequency, can be calculated using the guidelines given in *Application Note 74 (Evaluating Power for Altera Devices)*.

The I_{CCINT} value depends on the switching frequency and the application logic. The I_{CCINT} value is calculated with the following equation:

I_{CCINT} =

$$(A \times MC_{TON}) + [B \times (MC_{DEV} - MC_{TON})] + (C \times MC_{USED} \times \mathbf{f_{MAX}} \times \mathbf{tog_{LC}})$$

The parameters in this equation are:

MC_{TON} = Number of macrocells with the Turbo Bit™ option turned on, as reported in the MAX+PLUS II Report File (**.rpt**)
MC_{DEV} = Number of macrocells in the device
MC_{USED} = Total number of macrocells in the design, as reported in the Report File
$\mathbf{f_{MAX}}$ = Highest clock frequency to the device
$\mathbf{tog_{LC}}$ = Average percentage of logic cells toggling at each clock (typically 12.5%)
A, B, C = Constants, shown in Table 33

Table 33. MAX 7000B I_{CC} Equation Constants

Device	A	B	C
EPM7032B	0.91	0.54	0.010
EPM7064B	0.91	0.54	0.012
EPM7128B	0.91	0.54	0.016
EPM7256B	0.91	0.54	0.017
EPM7512B	0.91	0.54	0.019

This calculation provides an I_{CC} estimate based on typical conditions using a pattern of a 16-bit, loadable, enabled, up/down counter in each LAB with no output load. Actual I_{CC} should be verified during operation because this measurement is sensitive to the actual pattern in the device and the environmental operating conditions.

Figure 17. I_{CC} vs. Frequency for EPM7128B Devices

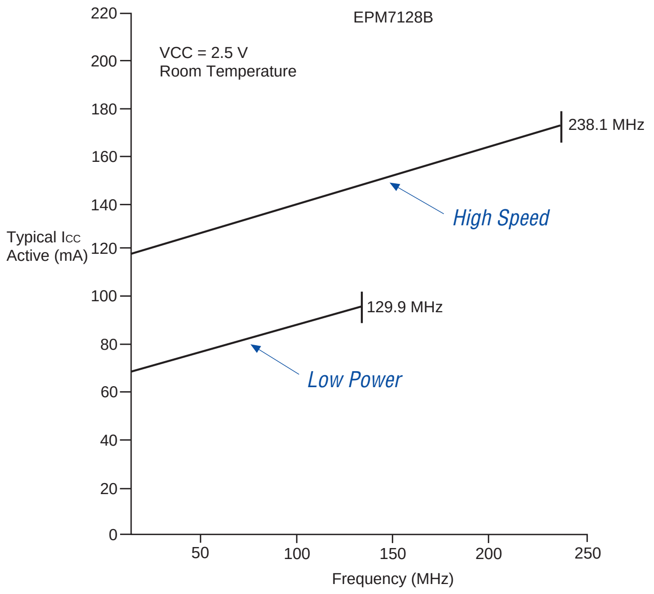


Figure 18. I_{CC} vs. Frequency for EPM7256B Devices

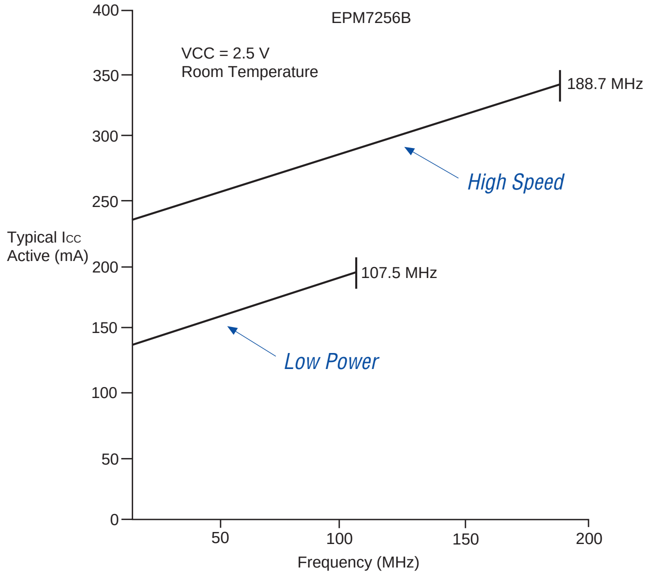


Figure 19. I_{CC} vs. Frequency for EPM7512B Devices

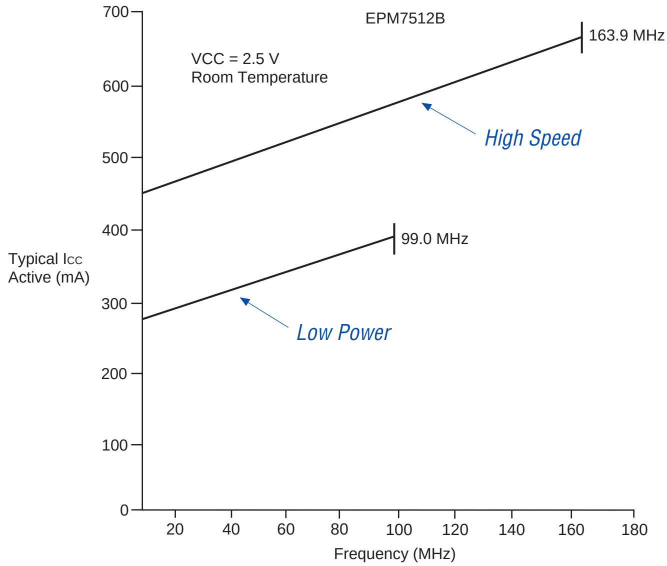


Figure 23. 100-Pin TQFP Package Pin-Out Diagram

Package outline not drawn to scale.

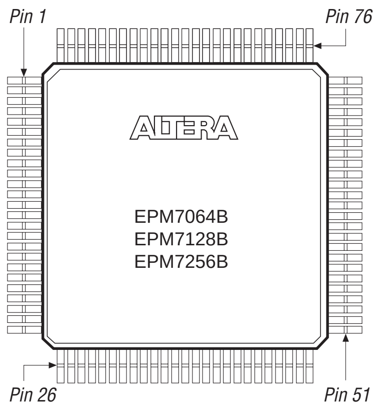


Figure 24. 100-Pin FineLine BGA Package Pin-Out Diagram

Package outline not drawn to scale.