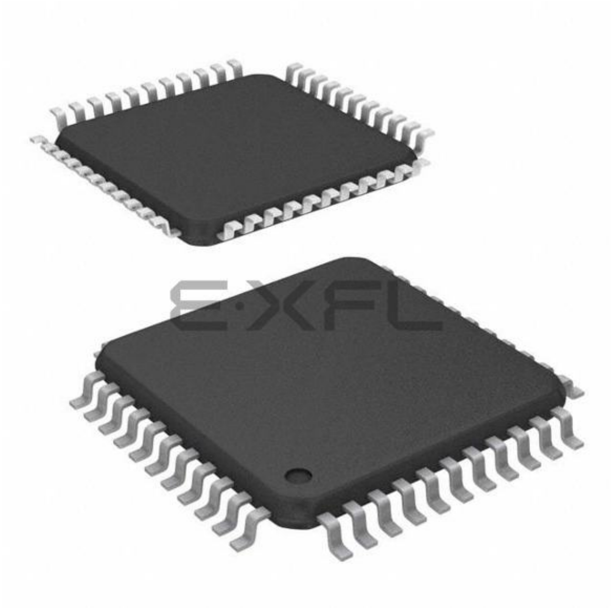


Welcome to E-XFL.COM

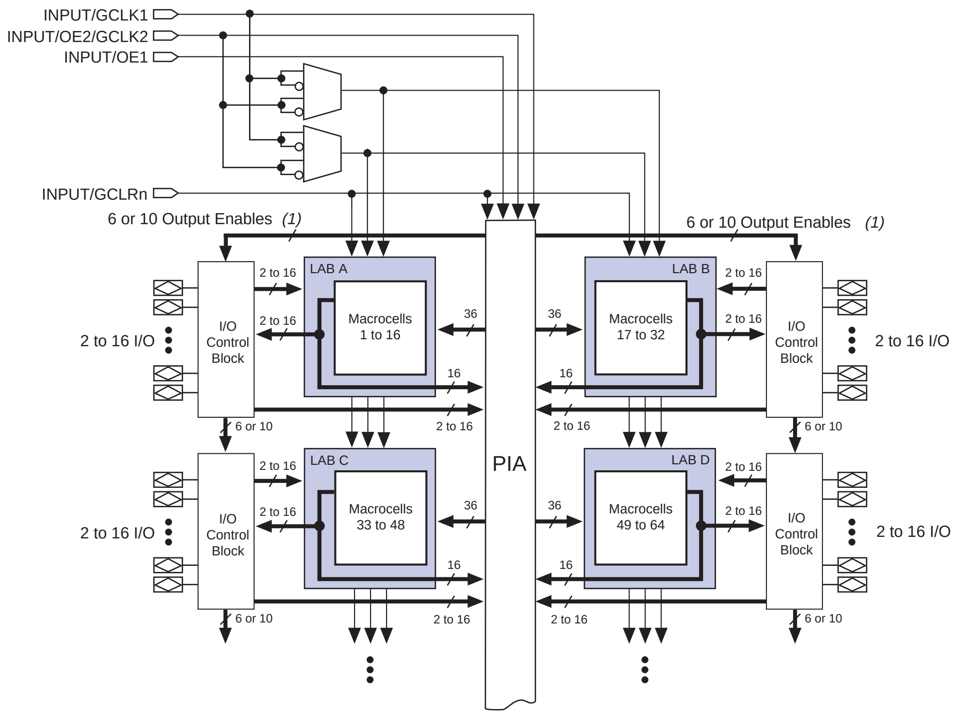
Understanding Embedded - CPLDs (Complex Programmable Logic Devices)

Embedded - CPLDs, or Complex Programmable Logic Devices, are highly versatile digital logic devices used in electronic systems. These programmable components are designed to perform complex logical operations and can be customized for specific applications. Unlike fixed-function ICs, CPLDs offer the flexibility to reprogram their configuration, making them an ideal choice for various embedded systems. They consist of a set of logic gates and programmable interconnects, allowing designers to implement complex logic circuits without needing custom hardware.

Applications of Embedded - CPLDs

Details	
Product Status	Obsolete
Programmable Type	In System Programmable
Delay Time tpd(1) Max	7.5 ns
Voltage Supply - Internal	2.375V ~ 2.625V
Number of Logic Elements/Blocks	4
Number of Macrocells	64
Number of Gates	1250
Number of I/O	36
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	44-TQFP
Supplier Device Package	44-TQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/intel/epm7064btc44-7n

Figure 1. MAX 7000B Device Block Diagram



Note:

(1) EPM7032B, EPM7064B, EPM7128B, and EPM7256B devices have six output enables. EPM7512B devices have ten output enables.

Logic Array Blocks

The MAX 7000B device architecture is based on the linking of high-performance LABs. LABs consist of 16 macrocell arrays, as shown in Figure 1. Multiple LABs are linked together via the PIA, a global bus that is fed by all dedicated input pins, I/O pins, and macrocells.

Each LAB is fed by the following signals:

- 36 signals from the PIA that are used for general logic inputs
- Global controls that are used for secondary register functions
- Direct input paths from I/O pins to the registers that are used for fast setup times

The Altera development system automatically optimizes product-term allocation according to the logic requirements of the design.

For registered functions, each macrocell flipflop can be individually programmed to implement D, T, JK, or SR operation with programmable clock control. The flipflop can be bypassed for combinatorial operation. During design entry, the designer specifies the desired flipflop type; the MAX+PLUS II software then selects the most efficient flipflop operation for each registered function to optimize resource utilization.

Each programmable register can be clocked in three different modes:

- Global clock signal. This mode achieves the fastest clock-to-output performance.
- Global clock signal enabled by an active-high clock enable. A clock enable is generated by a product term. This mode provides an enable on each flipflop while still achieving the fast clock-to-output performance of the global clock.
- Array clock implemented with a product term. In this mode, the flipflop can be clocked by signals from buried macrocells or I/O pins.

Two global clock signals are available in MAX 7000B devices. As shown in Figure 1, these global clock signals can be the true or the complement of either of the global clock pins, `GCLK1` or `GCLK2`.

Each register also supports asynchronous preset and clear functions. As shown in Figure 2, the product-term select matrix allocates product terms to control these operations. Although the product-term-driven preset and clear from the register are active high, active-low control can be obtained by inverting the signal within the logic array. In addition, each register clear function can be individually driven by the active-low dedicated global clear pin (`GCLRn`). Upon power-up, each register in a MAX 7000B device may be set to either a high or low state. This power-up state is specified at design entry.

All MAX 7000B I/O pins have a fast input path to a macrocell register. This dedicated path allows a signal to bypass the PIA and combinatorial logic and be clocked to an input D flipflop with an extremely fast input setup time. The input path from the I/O pin to the register has a programmable delay element that can be selected to either guarantee zero hold time or to get the fastest possible set-up time (as fast as 1.0 ns).

Programming Sequence

During in-system programming, instructions, addresses, and data are shifted into the MAX 7000B device through the `TDI` input pin. Data is shifted out through the `TDO` output pin and compared against the expected data.

Programming a pattern into the device requires the following six ISP stages. A stand-alone verification of a programmed pattern involves only stages 1, 2, 5, and 6.

1. *Enter ISP*. The enter ISP stage ensures that the I/O pins transition smoothly from user mode to ISP mode. The enter ISP stage requires 1 ms.

2. *Check ID*. Before any program or verify process, the silicon ID is checked. The time required to read this silicon ID is relatively small compared to the overall programming time.

3. *Bulk Erase*. Erasing the device in-system involves shifting in the instructions to erase the device and applying one erase pulse of 100 ms.

4. *Program*. Programming the device in-system involves shifting in the address and data and then applying the programming pulse to program the EEPROM cells. This process is repeated for each EEPROM address.

5. *Verify*. Verifying an Altera device in-system involves shifting in addresses, applying the read pulse to verify the EEPROM cells, and shifting out the data for comparison. This process is repeated for each EEPROM address.

6. *Exit ISP*. An exit ISP stage ensures that the I/O pins transition smoothly from ISP mode to user mode. The exit ISP stage requires 1 ms.

Programming Times

The time required to implement each of the six programming stages can be broken into the following two elements:

- A pulse time to erase, program, or read the EEPROM cells.
- A shifting time based on the test clock (`TCK`) frequency and the number of `TCK` cycles to shift instructions, address, and data into the device.

Programmable Speed/Power Control

MAX 7000B devices offer a power-saving mode that supports low-power operation across user-defined signal paths or the entire device. This feature allows total power dissipation to be reduced by 50% or more, because most logic applications require only a small fraction of all gates to operate at maximum frequency.

The designer can program each individual macrocell in a MAX 7000B device for either high-speed or low-power operation. As a result, speed-critical paths in the design can run at high speed, while the remaining paths can operate at reduced power. Macrocells that run at low power incur a nominal timing delay adder (t_{LPA}) for the t_{LAD}, t_{LAC}, t_{IC}, t_{ACL}, t_{CPPW}, t_{EN}, and t_{SEXP} parameters.

Output Configuration

MAX 7000B device outputs can be programmed to meet a variety of system-level requirements.

MultiVolt I/O Interface

The MAX 7000B device architecture supports the MultiVolt I/O interface feature, which allows MAX 7000B devices to connect to systems with differing supply voltages. MAX 7000B devices in all packages can be set for 3.3-V, 2.5-V, or 1.8-V pin operation. These devices have one set of V_{CC} pins for internal operation and input buffers (`VCCINT`), and another set for I/O output drivers (`VCCIO`).

The `VCCIO` pins can be connected to either a 3.3-V, 2.5-V, or 1.8-V power supply, depending on the output requirements. When the `VCCIO` pins are connected to a 1.8-V power supply, the output levels are compatible with 1.8-V systems. When the `VCCIO` pins are connected to a 2.5-V power supply, the output levels are compatible with 2.5-V systems. When the `VCCIO` pins are connected to a 3.3-V power supply, the output high is at 3.3 V and is therefore compatible with 3.3-V or 5.0-V systems. Devices operating with V_{CCIO} levels of 2.5 V or 1.8 V incur a nominal timing delay adder.

Table 10 describes the MAX 7000B MultiVolt I/O support.

Table 10. MAX 7000B MultiVolt I/O Support

V_{CCIO} (V)	Input Signal (V)				Output Signal (V)			
	1.8	2.5	3.3	5.0	1.8	2.5	3.3	5.0
1.8	✓	✓	✓		✓			
2.5	✓	✓	✓			✓		
3.3	✓	✓	✓				✓	✓

Open-Drain Output Option

MAX 7000B devices provide an optional open-drain (equivalent to open-collector) output for each I/O pin. This open-drain output enables the device to provide system-level control signals (e.g., interrupt and write enable signals) that can be asserted by any of several devices. It can also provide an additional wired-OR plane.

Programmable Ground Pins

Each unused I/O pin on MAX 7000B devices may be used as an additional ground pin. This programmable ground feature does not require the use of the associated macrocell; therefore, the buried macrocell is still available for user logic.

Slew-Rate Control

The output buffer for each MAX 7000B I/O pin has an adjustable output slew rate that can be configured for low-noise or high-speed performance. A faster slew rate provides high-speed transitions for high-performance systems. However, these fast transitions may introduce noise transients into the system. A slow slew rate reduces system noise, but adds a nominal delay of 4 to 5 ns. When the configuration cell is turned off, the slew rate is set for low-noise performance. Each I/O pin has an individual EEPROM bit that controls the slew rate, allowing designers to specify the slew rate on a pin-by-pin basis. The slew rate control affects both the rising and falling edges of the output signal.

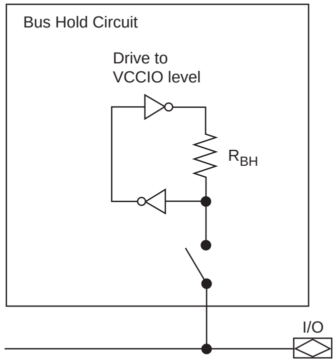
Advanced I/O Standard Support

The MAX 7000B I/O pins support the following I/O standards: LVTTL, LVCMOS, 1.8-V I/O, 2.5-V I/O, GTL+, SSTL-3 Class I and II, and SSTL-2 Class I and II.

Two inverters implement the bus-hold circuitry in a loop that weakly drives back to the I/O pin in user mode.

Figure 10 shows a block diagram of the bus-hold circuit.

Figure 10. Bus-Hold Circuit



PCI Compatibility

MAX 7000B devices are compatible with PCI applications as well as all 3.3-V electrical specifications in the ***PCI Local Bus Specification Revision 2.2*** except for the clamp diode. While having multiple clamp diodes on a signal trace may be redundant, designers can add an external clamp diode to meet the specification. Table 13 shows the MAX 7000B device speed grades that meet the PCI timing specifications.

Table 13. MAX 7000B Device Speed Grades that Meet PCI Timing Specifications

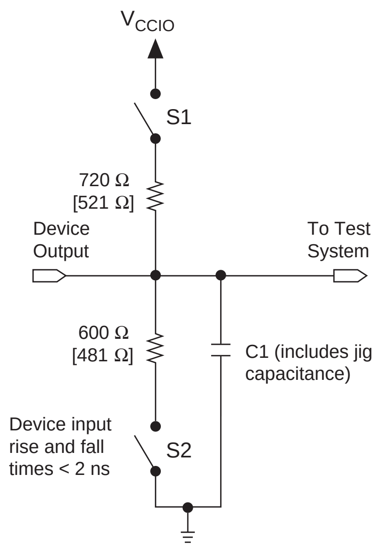
Device	Specification	
	33-MHz PCI	66-MHz PCI
EPM7032B	All speed grades	-3
EPM7064B	All speed grades	-3
EPM7128B	All speed grades	-4
EPM7256B	All speed grades	-5 *(1)*
EPM7512B	All speed grades	-5 *(1)*

Note:

(1) The EPM7256B and EPM7512B devices in a -5 speed grade meet all PCI timing specifications for 66-MHz operation except the Input Setup Time to CLK—Bused Signal parameter. However, these devices are within 1 ns of that parameter. EPM7256B and EPM7512B devices meet all other 66-MHz PCI timing specifications.

Figure 11. MAX 7000B AC Test Conditions

Power supply transients can affect AC measurements. Simultaneous transitions of multiple outputs should be avoided for accurate measurement. Threshold tests must not be performed under AC conditions. Large-amplitude, fast-ground-current transients normally occur as the device outputs discharge the load capacitances. When these transients flow through the parasitic inductance between the device ground pin and the test system ground, significant reductions in observable noise immunity can result. Numbers in brackets are for 2.5-V outputs. Numbers without brackets are for 3.3-V outputs. Switches S1 and S2 are open for all tests except output disable timing parameters.



Operating Conditions

Tables 14 through 17 provide information on absolute maximum ratings, recommended operating conditions, operating conditions, and capacitance for MAX 7000B devices.

Table 14. MAX 7000B Device Absolute Maximum Ratings Note (1)

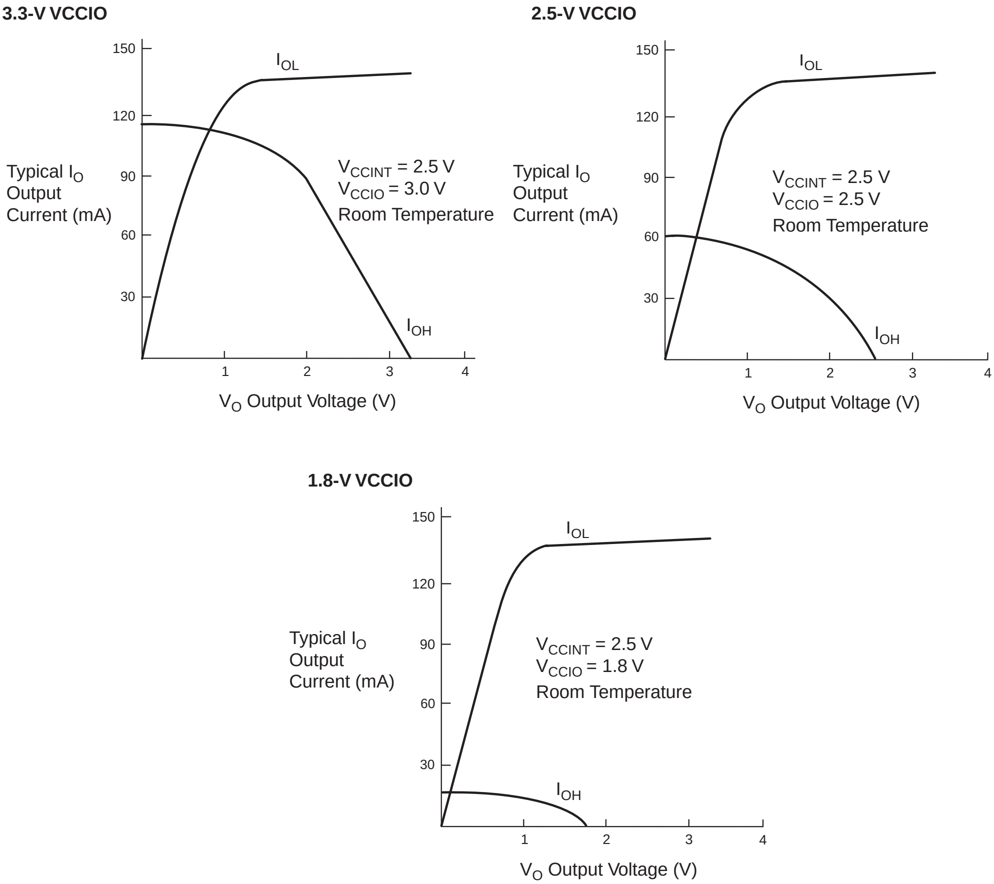
Symbol	Parameter	Conditions	Min	Max	Unit
V_{CCINT}	Supply voltage		–0.5	3.6	V
V_{CCIO}	Supply voltage		–0.5	3.6	V
V_I	DC input voltage	(2)	–2.0	4.6	V
I_{OUT}	DC output current, per pin		–33	50	mA
T_{STG}	Storage temperature	No bias	–65	150	° C
T_A	Ambient temperature	Under bias	–65	135	° C
T_J	Junction temperature	Under bias	–65	135	° C

Table 15. MAX 7000B Device Recommended Operating Conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CCINT}	Supply voltage for internal logic and input buffers	*(10)*	2.375	2.625	V
V_{CCIO}	Supply voltage for output drivers, 3.3-V operation		3.0	3.6	V
	Supply voltage for output drivers, 2.5-V operation		2.375	2.625	V
	Supply voltage for output drivers, 1.8-V operation		1.71	1.89	V
V_{CCISP}	Supply voltage during in-system programming		2.375	2.625	V
V_I	Input voltage	*(3)*	–0.5	3.9	V
V_O	Output voltage		0	V_{CCIO}	V
T_A	Ambient temperature	For commercial use	0	70	° C
		For industrial use *(11)*	–40	85	° C
T_J	Junction temperature	For commercial use	0	90	° C
		For industrial use *(11)*	–40	105	° C
t_R	Input rise time			40	ns
t_F	Input fall time			40	ns

Figure 12 shows the typical output drive characteristics of MAX 7000B devices.

Figure 12. Output Drive Characteristics of MAX 7000B Devices



Tables 18 through 32 show MAX 7000B device timing parameters.

Table 18. EPM7032B External Timing Parameters *Notes (1)*

Symbol	Parameter	Conditions	Speed Grade						Unit
			-3.5		-5.0		-7.5		
			Min	Max	Min	Max	Min	Max	
t_{PD1}	Input to non-registered output	C1 = 35 pF *(2)*		3.5		5.0		7.5	ns
t_{PD2}	I/O input to non-registered output	C1 = 35 pF *(2)*		3.5		5.0		7.5	ns
t_{SU}	Global clock setup time	*(2)*	2.1		3.0		4.5		ns
t_{H}	Global clock hold time	*(2)*	0.0		0.0		0.0		ns
t_{FSU}	Global clock setup time of fast input		1.0		1.0		1.5		ns
t_{FH}	Global clock hold time of fast input		1.0		1.0		1.0		ns
t_{FZHSU}	Global clock setup time of fast input with zero hold time		2.0		2.5		3.0		ns
t_{FZHH}	Global clock hold time of fast input with zero hold time		0.0		0.0		0.0		ns
t_{CO1}	Global clock to output delay	C1 = 35 pF	1.0	2.4	1.0	3.4	1.0	5.0	ns
t_{CH}	Global clock high time		1.5		2.0		3.0		ns
t_{CL}	Global clock low time		1.5		2.0		3.0		ns
t_{ASU}	Array clock setup time	*(2)*	0.9		1.3		1.9		ns
t_{AH}	Array clock hold time	*(2)*	0.2		0.3		0.6		ns
t_{ACO1}	Array clock to output delay	C1 = 35 pF *(2)*	1.0	3.6	1.0	5.1	1.0	7.6	ns
t_{ACH}	Array clock high time		1.5		2.0		3.0		ns
t_{ACL}	Array clock low time		1.5		2.0		3.0		ns
t_{CPPW}	Minimum pulse width for clear and preset		1.5		2.0		3.0		ns
t_{CNT}	Minimum global clock period	*(2)*		3.3		4.7		7.0	ns
f_{CNT}	Maximum internal global clock frequency	*(2)*, *(3)*	303.0		212.8		142.9		MHz
t_{ACNT}	Minimum array clock period	*(2)*		3.3		4.7		7.0	ns
f_{ACNT}	Maximum internal array clock frequency	*(2)*, *(3)*	303.0		212.8		142.9		MHz

Table 19. EPM7032B Internal Timing Parameters *Notes (1)*									
Symbol	**Parameter**	**Conditions**	**Speed Grade**						**Unit**
			-3.5		**-5.0**		**-7.5**		
			Min	**Max**	**Min**	**Max**	**Min**	**Max**	
t_{IN}	Input pad and buffer delay			0.3		0.5		0.7	ns
t_{IO}	I/O input pad and buffer delay			0.3		0.5		0.7	ns
t_{FIN}	Fast input delay			0.9		1.3		2.0	ns
t_{FIND}	Programmable delay adder for fast input			1.0		1.5		1.5	ns
t_{SEXP}	Shared expander delay			1.5		2.1		3.2	ns
t_{PEXP}	Parallel expander delay			0.4		0.6		0.9	ns
t_{LAD}	Logic array delay			1.4		2.0		3.1	ns
t_{LAC}	Logic control array delay			1.2		1.7		2.6	ns
t_{IOE}	Internal output enable delay			0.1		0.2		0.3	ns
t_{OD1}	Output buffer and pad delay slow slew rate = off V_{CCIO} = 3.3 V	C1 = 35 pF		0.9		1.2		1.8	ns
t_{OD3}	Output buffer and pad delay slow slew rate = on V_{CCIO} = 2.5 V or 3.3 V	C1 = 35 pF		5.9		6.2		6.8	ns
t_{ZX1}	Output buffer enable delay slow slew rate = off V_{CCIO} = 3.3 V	C1 = 35 pF		1.6		2.2		3.4	ns
t_{ZX3}	Output buffer enable delay slow slew rate = on V_{CCIO} = 2.5 V or 3.3 V	C1 = 35 pF		6.6		7.2		8.4	ns
t_{XZ}	Output buffer disable delay	C1 = 5 pF		1.6		2.2		3.4	ns
t_{SU}	Register setup time		0.7		1.1		1.6		ns
t_{H}	Register hold time		0.4		0.5		0.9		ns
t_{FSU}	Register setup time of fast input		0.8		0.8		1.1		ns
t_{FH}	Register hold time of fast input		1.2		1.2		1.4		ns
t_{RD}	Register delay			0.5		0.6		0.9	ns
t_{COMB}	Combinatorial delay			0.2		0.3		0.5	ns
t_{IC}	Array clock delay			1.2		1.8		2.8	ns
t_{EN}	Register enable time			1.2		1.7		2.6	ns
t_{GLOB}	Global control delay			0.7		1.1		1.6	ns
t_{PRE}	Register preset time			1.0		1.3		1.9	ns
t_{CLR}	Register clear time			1.0		1.3		1.9	ns
t_{PIA}	PIA delay	*(2)*		0.7		1.0		1.4	ns
t_{LPA}	Low-power adder	*(4)*		1.5		2.1		3.2	ns

Table 21. EPM7064B External Timing Parameters *Note (1)*

Symbol	Parameter	Conditions	Speed Grade						Unit
			-3		-5		-7		
			Min	Max	Min	Max	Min	Max	
t_{PD1}	Input to non-registered output	C1 = 35 pF *(2)*		3.5		5.0		7.5	ns
t_{PD2}	I/O input to non-registered output	C1 = 35 pF *(2)*		3.5		5.0		7.5	ns
t_{SU}	Global clock setup time	*(2)*	2.1		3.0		4.5		ns
t_{H}	Global clock hold time	*(2)*	0.0		0.0		0.0		ns
t_{FSU}	Global clock setup time of fast input		1.0		1.0		1.5		ns
t_{FH}	Global clock hold time of fast input		1.0		1.0		1.0		ns
t_{FZHSU}	Global clock setup time of fast input with zero hold time		2.0		2.5		3.0		ns
t_{FZHH}	Global clock hold time of fast input with zero hold time		0.0		0.0		0.0		ns
t_{CO1}	Global clock to output delay	C1 = 35 pF	1.0	2.4	1.0	3.4	1.0	5.0	ns
t_{CH}	Global clock high time		1.5		2.0		3.0		ns
t_{CL}	Global clock low time		1.5		2.0		3.0		ns
t_{ASU}	Array clock setup time	*(2)*	0.9		1.3		1.9		ns
t_{AH}	Array clock hold time	*(2)*	0.2		0.3		0.6		ns
t_{ACO1}	Array clock to output delay	C1 = 35 pF *(2)*	1.0	3.6	1.0	5.1	1.0	7.6	ns
t_{ACH}	Array clock high time		1.5		2.0		3.0		ns
t_{ACL}	Array clock low time		1.5		2.0		3.0		ns
t_{CPPW}	Minimum pulse width for clear and preset		1.5		2.0		3.0		ns
t_{CNT}	Minimum global clock period	*(2)*		3.3		4.7		7.0	ns
f_{CNT}	Maximum internal global clock frequency	*(2)*, *(3)*	303.0		212.8		142.9		MHz
t_{ACNT}	Minimum array clock period	*(2)*		3.3		4.7		7.0	ns
f_{ACNT}	Maximum internal array clock frequency	*(2)*, *(3)*	303.0		212.8		142.9		MHz

Table 25. EPM7128B Internal Timing Parameters *Note (1)*

Symbol	Parameter	Conditions	Speed Grade						Unit
			-4		-7		-10		
			Min	Max	Min	Max	Min	Max	
t_{IN}	Input pad and buffer delay			0.3		0.6		0.8	ns
t_{IO}	I/O input pad and buffer delay			0.3		0.6		0.8	ns
t_{FIN}	Fast input delay			1.3		2.9		3.7	ns
t_{FIND}	Programmable delay adder for fast input			1.0		1.5		1.5	ns
t_{SEXP}	Shared expander delay			1.5		2.8		3.8	ns
t_{PEXP}	Parallel expander delay			0.4		0.8		1.0	ns
t_{LAD}	Logic array delay			1.6		2.9		3.8	ns
t_{LAC}	Logic control array delay			1.4		2.6		3.4	ns
t_{IOE}	Internal output enable delay			0.1		0.3		0.4	ns
t_{OD1}	Output buffer and pad delay slow slew rate = off V_{CCIO} = 3.3 V	C1 = 35 pF		0.9		1.7		2.2	ns
t_{OD3}	Output buffer and pad delay slow slew rate = on V_{CCIO} = 2.5 V or 3.3 V	C1 = 35 pF		5.9		6.7		7.2	ns
t_{ZX1}	Output buffer enable delay slow slew rate = off V_{CCIO} = 3.3 V	C1 = 35 pF		1.8		3.3		4.4	ns
t_{ZX3}	Output buffer enable delay slow slew rate = on V_{CCIO} = 2.5 V or 3.3 V	C1 = 35 pF		6.8		8.3		9.4	ns
t_{XZ}	Output buffer disable delay	C1 = 5 pF		1.8		3.3		4.4	ns
t_{SU}	Register setup time		1.0		1.9		2.6		ns
t_{H}	Register hold time		0.4		0.8		1.1		ns
t_{FSU}	Register setup time of fast input		0.8		0.9		0.9		ns
t_{FH}	Register hold time of fast input		1.2		1.6		1.6		ns
t_{RD}	Register delay			0.5		1.1		1.4	ns
t_{COMB}	Combinatorial delay			0.2		0.3		0.4	ns
t_{IC}	Array clock delay			1.4		2.8		3.6	ns
t_{EN}	Register enable time			1.4		2.6		3.4	ns
t_{GLOB}	Global control delay			1.1		2.3		3.1	ns
t_{PRE}	Register preset time			1.0		1.9		2.6	ns
t_{CLR}	Register clear time			1.0		1.9		2.6	ns
t_{PIA}	PIA delay	*(2)*		1.0		2.0		2.8	ns
t_{LPA}	Low-power adder	*(4)*		1.5		2.8		3.8	ns

Table 28. EPM7256B Internal Timing Parameters *Note (1)*									
Symbol	**Parameter**	**Conditions**	**Speed Grade**						**Unit**
			-5		**-7**		**-10**		
			Min	**Max**	**Min**	**Max**	**Min**	**Max**	
t_{IN}	Input pad and buffer delay			0.4		0.6		0.8	ns
t_{IO}	I/O input pad and buffer delay			0.4		0.6		0.8	ns
t_{FIN}	Fast input delay			1.5		2.5		3.1	ns
t_{FIND}	Programmable delay adder for fast input			1.5		1.5		1.5	ns
t_{SEXP}	Shared expander delay			1.5		2.3		3.0	ns
t_{PEXP}	Parallel expander delay			0.4		0.6		0.8	ns
t_{LAD}	Logic array delay			1.7		2.5		3.3	ns
t_{LAC}	Logic control array delay			1.5		2.2		2.9	ns
t_{IOE}	Internal output enable delay			0.1		0.2		0.3	ns
t_{OD1}	Output buffer and pad delay slow slew rate = off V_{CCIO} = 3.3 V	C1 = 35 pF		0.9		1.4		1.9	ns
t_{OD3}	Output buffer and pad delay slow slew rate = on V_{CCIO} = 2.5 V or 3.3 V	C1 = 35 pF		5.9		6.4		6.9	ns
t_{ZX1}	Output buffer enable delay slow slew rate = off V_{CCIO} = 3.3 V	C1 = 35 pF		2.2		3.3		4.5	ns
t_{ZX3}	Output buffer enable delay slow slew rate = on V_{CCIO} = 2.5 V or 3.3 V	C1 = 35 pF		7.2		8.3		9.5	ns
t_{XZ}	Output buffer disable delay	C1 = 5 pF		2.2		3.3		4.5	ns
t_{SU}	Register setup time		1.2		1.8		2.5		ns
t_{H}	Register hold time		0.6		1.0		1.3		ns
t_{FSU}	Register setup time of fast input		0.8		1.1		1.1		ns
t_{FH}	Register hold time of fast input		1.2		1.4		1.4		ns
t_{RD}	Register delay			0.7		1.0		1.3	ns
t_{COMB}	Combinatorial delay			0.3		0.4		0.5	ns
t_{IC}	Array clock delay			1.5		2.3		3.0	ns
t_{EN}	Register enable time			1.5		2.2		2.9	ns
t_{GLOB}	Global control delay			1.3		2.1		2.7	ns
t_{PRE}	Register preset time			1.0		1.6		2.1	ns
t_{CLR}	Register clear time			1.0		1.6		2.1	ns
t_{PIA}	PIA delay	*(2)*		1.7		2.6		3.3	ns
t_{LPA}	Low-power adder	*(4)*		2.0		3.0		4.0	ns

Table 29. EPM7256B Selectable I/O Standard Timing Adder Delays (Part 1 of 2) Note (1)

I/O Standard	Parameter	Speed Grade						Unit
		-5		-7		-10		
		Min	Max	Min	Max	Min	Max	
3.3 V TTL/CMOS	Input to PIA		0.0		0.0		0.0	ns
	Input to global clock and clear		0.0		0.0		0.0	ns
	Input to fast input register		0.0		0.0		0.0	ns
	All outputs		0.0		0.0		0.0	ns
2.5 V TTL/CMOS	Input to PIA		0.4		0.6		0.8	ns
	Input to global clock and clear		0.3		0.5		0.6	ns
	Input to fast input register		0.2		0.3		0.4	ns
	All outputs		0.2		0.3		0.4	ns
1.8 V TTL/CMOS	Input to PIA		0.6		0.9		1.2	ns
	Input to global clock and clear		0.6		0.9		1.2	ns
	Input to fast input register		0.5		0.8		1.0	ns
	All outputs		1.3		2.0		2.6	ns
SSTL-2 Class I	Input to PIA		1.5		2.3		3.0	ns
	Input to global clock and clear		1.3		2.0		2.6	ns
	Input to fast input register		1.1		1.7		2.2	ns
	All outputs		0.0		0.0		0.0	ns
SSTL-2 Class II	Input to PIA		1.5		2.3		3.0	ns
	Input to global clock and clear		1.3		2.0		2.6	ns
	Input to fast input register		1.1		1.7		2.2	ns
	All outputs		–0.1		–0.2		–0.2	ns
SSTL-3 Class I	Input to PIA		1.4		2.1		2.8	ns
	Input to global clock and clear		1.1		1.7		2.2	ns
	Input to fast input register		1.0		1.5		2.0	ns
	All outputs		0.0		0.0		0.0	ns
SSTL-3 Class II	Input to PIA		1.4		2.1		2.8	ns
	Input to global clock and clear		1.1		1.7		2.2	ns
	Input to fast input register		1.0		1.5		2.0	ns
	All outputs		0.0		0.0		0.0	ns
GTL+	Input to PIA		1.8		2.7		3.6	ns
	Input to global clock and clear		1.8		2.7		3.6	ns
	Input to fast input register		1.7		2.6		3.4	ns
	All outputs		0.0		0.0		0.0	ns

Table 29. EPM7256B Selectable I/O Standard Timing Adder Delays (Part 2 of 2) Note (1)

I/O Standard	Parameter	Speed Grade						Unit
		-5		-7		-10		
		Min	Max	Min	Max	Min	Max	
PCI	Input to PIA		0.0		0.0		0.0	ns
	Input to global clock and clear		0.0		0.0		0.0	ns
	Input to fast input register		0.0		0.0		0.0	ns
	All outputs		0.0		0.0		0.0	ns

Notes to tables:

(1) These values are specified under the Recommended Operating Conditions in Table 15 on page 29. See Figure 14 for more information on switching waveforms.

(2) These values are specified for a PIA fan-out of one LAB (16 macrocells). For each additional LAB fan-out in these devices, add an additional 0.1 ns to the PIA timing value.

(3) Measured with a 16-bit loadable, enabled, up/down counter programmed into each LAB.

(4) The t_{LPA} parameter must be added to the t_{LAD}, t_{LAC}, t_{IC}, t_{ACL}, t_{CPPW}, t_{EN}, and t_{SEXP} parameters for macrocells running in low-power mode.

Table 32. EPM7512B Selectable I/O Standard Timing Adder Delays (Part 1 of 2) Note (1)

I/O Standard	Parameter	Speed Grade						Unit
		-5		-7		-10		
		Min	Max	Min	Max	Min	Max	
3.3 V TTL/CMOS	Input to PIA		0.0		0.0		0.0	ns
	Input to global clock and clear		0.0		0.0		0.0	ns
	Input to fast input register		0.0		0.0		0.0	ns
	All outputs		0.0		0.0		0.0	ns
2.5 V TTL/CMOS	Input to PIA		0.4		0.5		0.7	ns
	Input to global clock and clear		0.3		0.4		0.5	ns
	Input to fast input register		0.2		0.3		0.3	ns
	All outputs		0.2		0.3		0.3	ns
1.8 V TTL/CMOS	Input to PIA		0.7		1.0		1.3	ns
	Input to global clock and clear		0.6		0.8		1.0	ns
	Input to fast input register		0.5		0.6		0.8	ns
	All outputs		1.3		1.8		2.3	ns
SSTL-2 Class I	Input to PIA		1.5		2.0		2.7	ns
	Input to global clock and clear		1.4		1.9		2.5	ns
	Input to fast input register		1.1		1.5		2.0	ns
	All outputs		0.0		0.0		0.0	ns
SSTL-2 Class II	Input to PIA		1.5		2.0		2.7	ns
	Input to global clock and clear		1.4		1.9		2.5	ns
	Input to fast input register		1.1		1.5		2.0	ns
	All outputs		–0.1		–0.1		–0.2	ns
SSTL-3 Class I	Input to PIA		1.4		1.9		2.5	ns
	Input to global clock and clear		1.2		1.6		2.2	ns
	Input to fast input register		1.0		1.4		1.8	ns
	All outputs		0.0		0.0		0.0	ns
SSTL-3 Class II	Input to PIA		1.4		1.9		2.5	ns
	Input to global clock and clear		1.2		1.6		2.2	ns
	Input to fast input register		1.0		1.4		1.8	ns
	All outputs		0.0		0.0		0.0	ns
GTL+	Input to PIA		1.8		2.5		3.3	ns
	Input to global clock and clear		1.9		2.6		3.5	ns
	Input to fast input register		1.8		2.5		3.3	ns
	All outputs		0.0		0.0		0.0	ns

Table 32. EPM7512B Selectable I/O Standard Timing Adder Delays (Part 2 of 2) *Note (1)*

I/O Standard	Parameter	Speed Grade						Unit
		-5		-7		-10		
		Min	Max	Min	Max	Min	Max	
PCI	Input to PIA		0.0		0.0		0.0	ns
	Input to global clock and clear		0.0		0.0		0.0	ns
	Input to fast input register		0.0		0.0		0.0	ns
	All outputs		0.0		0.0		0.0	ns

Notes to tables:

(1) These values are specified under the Recommended Operating Conditions in Table 15 on page 29. See Figure 14 for more information on switching waveforms.

(2) These values are specified for a PIA fan-out of one LAB (16 macrocells). For each additional LAB fan-out in these devices, add an additional 0.12 ns to the PIA timing value.

(3) Measured with a 16-bit loadable, enabled, up/down counter programmed into each LAB.

(4) The t_{LPA} parameter must be added to the t_{LAD}, t_{LAC}, t_{IC}, t_{ACL}, t_{CPPW}, t_{EN}, and t_{SEXP} parameters for macrocells running in low-power mode.

Power Consumption

Supply power (P) versus frequency ($\mathbf{f_{MAX}}$, in MHz) for MAX 7000B devices is calculated with the following equation:

$$P = P_{INT} + P_{IO} = I_{CCINT} \times V_{CC} + P_{IO}$$

The P_{IO} value, which depends on the device output load characteristics and switching frequency, can be calculated using the guidelines given in *Application Note 74 (Evaluating Power for Altera Devices)*.

Figure 15. I_{CC} vs. Frequency for EPM7032B Devices

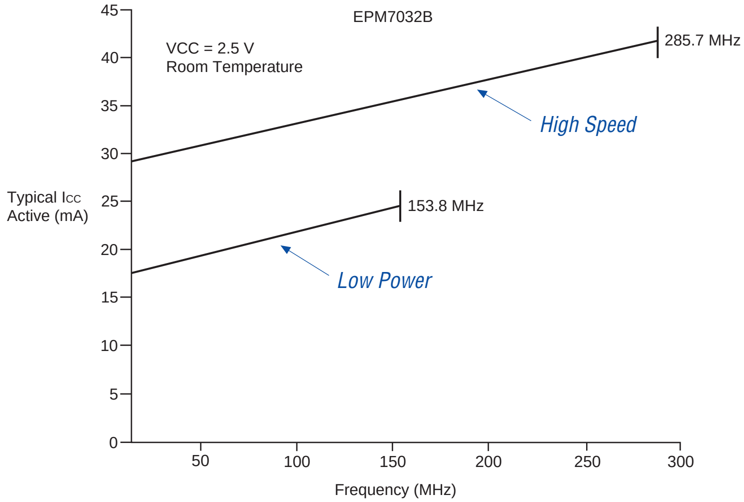


Figure 16. I_{CC} vs. Frequency for EPM7064B Devices

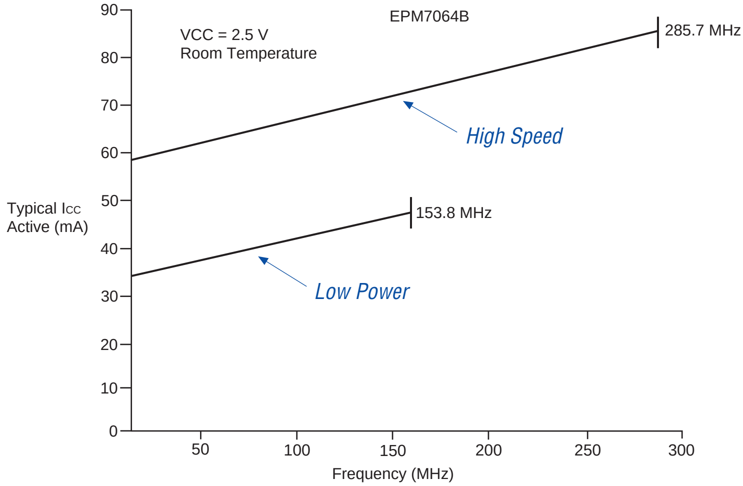


Figure 27. 208-Pin PQFP Package Pin-Out Diagram

Package outline not drawn to scale.